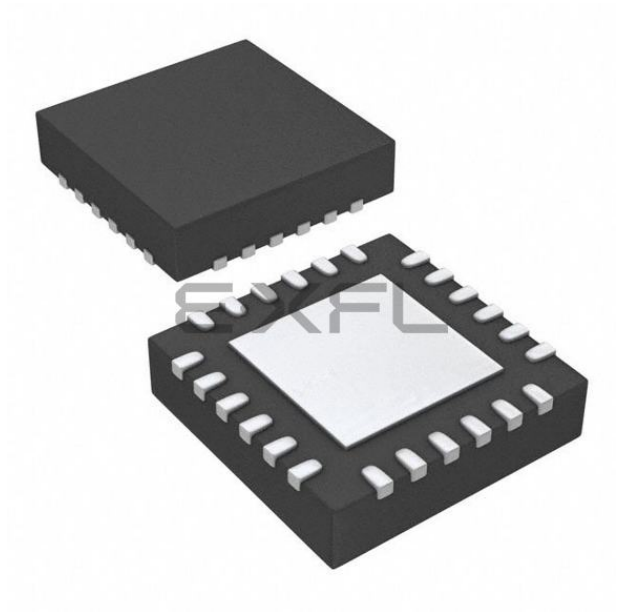

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	20
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-HVQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1114lvfhn24-103

- UART with fractional baud rate generation and internal FIFO.
- One SPI controller with SSP features and with FIFO and multi-protocol capabilities.
- I^2C-bus interface supporting full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.

- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 2.5 % accuracy for T_{amb} = -20 °C to +85 °C and to 5 % accuracy for T_{amb} = -40 °C to -20 °C. The IRC can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
  - Clock output function with divider that can reflect the system oscillator clock, IRC clock, CPU clock, and the Watchdog clock.
- Power control:
  - Two reduced power modes: Sleep and Deep-sleep mode.
  - Ultra-low power consumption in Deep-sleep mode ($\leq$ 1.6 μA).
  - 5 μs wake-up time from Deep-sleep mode.
  - Processor wake-up from Deep-sleep mode via a dedicated start logic using up to 13 of the functional pins.
  - Power-On Reset (POR).
  - Brown-Out Detection (BOD) causing a forced reset.
- Unique device serial number for identification.
- Single power supply (1.65 V to 1.95 V)
- Available as WLCSP25, HVQFN24, and HVQFN33 package. Other package options are available for high-volume customers.

3. Applications

- Mobile phones
- Mobile accessories
- Cameras
- Tablets/Ultra books
- Active cables
- Portable medical electronics

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1101LVUK	WLCSP25	wafer level chip-size package; 25 bumps; 2.17 × 2.32 × 0.56 mm	-
LPC1102LVUK	WLCSP25	wafer level chip-size package; 25 bumps; 2.17 × 2.32 × 0.56 mm	-
LPC1112LVFHN24/003	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm	SOT616-3
LPC1114LVFHN24/103	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm	SOT616-3

6.2 Pin description

Table 3. LPC110xLVUK/LPC111xLV pin description table

Symbol	WLCSP25	HVQFN24	HVQFN33		Start logic input	Type	Reset state [1]	Description
$\overline{\text{RESET}}$/PIO0_0	D1	2	2	[2]	yes	I	I; PU	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
						I/O	-	**PIO0_0 —** General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	C3	3	3	[3]	yes	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
						O	-	**CLKOUT —** Clockout pin.
						O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	B2	7	8	[3]	yes	I/O	I; PU	**PIO0_2 —** General purpose digital input/output pin.
						I/O	-	**SSEL0 —** Slave Select for SPI0.
						I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3	-	-	9	[3]	yes	I/O	I;PU	**PIO0_3 —** General purpose digital input/output pin.
PIO0_4/SCL	A2	8	10	[4]	yes	I/O	I; IA	**PIO0_4 —** General purpose digital input/output pin (open-drain).
						I/O	-	**SCL —** I^2C-bus, open-drain clock input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	A3	9	11	[4]	yes	I/O	I; IA	**PIO0_5 —** General purpose digital input/output pin (open-drain).
						I/O	-	**SDA —** I^2C-bus, open-drain data input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	A4	10	15	[3]	yes	I/O	I; PU	**PIO0_6 —** General purpose digital input/output pin.
						I/O	-	**SCK0 —** Serial clock for SPI0.
PIO0_7/$\overline{\text{CTS}}$	-	11	16	[3]	yes	I/O	I; PU	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
						I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	A5	12	17	[3]	yes	I/O	I; PU	**PIO0_8 —** General purpose digital input/output pin.
						I/O	-	**MISO0 —** Master In Slave Out for SPI0.
						O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	B5	13	18	[3]	yes	I/O	I; PU	**PIO0_9 —** General purpose digital input/output pin.
						I/O	-	**MOSI0 —** Master Out Slave In for SPI0.
						O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.

Table 3. LPC110xLVUK/LPC111xLV pin description table

Symbol	WLCSP25	HVQFN24	HVQFN33		Start logic input	Type	Reset state [1]	Description
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	B4	14	19	[3]	yes	I	I; PU	**SWCLK —** Serial wire clock.
						I/O	-	**PIO0_10 —** General purpose digital input/output pin.
						I/O	-	**SCK0 —** Serial clock for SPI0.
						O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	C5	15	21	[5]	yes	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCON block.
						I/O	-	**PIO0_11 —** General purpose digital input/output pin.
						I	-	**AD0 —** A/D converter, input 0.
						O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
R/PIO1_0/ AD1/CT32B1_CAP0	C4	16	22	[5]	yes	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCON block.
						I/O	-	**PIO1_0 —** General purpose digital input/output pin.
						I	-	**AD1 —** A/D converter, input 1.
						I	-	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	D5	17	23	[5]	no	O	I; PU	**R —** Reserved. Configure for an alternate function in the IOCON block.
						I/O	-	**PIO1_1 —** General purpose digital input/output pin.
						I	-	**AD2 —** A/D converter, input 2.
						O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	D4	18	24	[5]	no	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCON block.
						I/O	-	**PIO1_2 —** General purpose digital input/output pin.
						I	-	**AD3 —** A/D converter, input 3.
						O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	E5	19	25	[5]	no	I/O	I; PU	**SWDIO —** Serial wire debug input/output.
						I/O	-	**PIO1_3 —** General purpose digital input/output pin.
						I	-	**AD4 —** A/D converter, input 4.
						O	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3	D3	20	26	[5]	no	I/O	I; PU	**PIO1_4 —** General purpose digital input/output pin with 10 ns glitch filter.
						I	-	**AD5 —** A/D converter, input 5.
						O	-	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
PIO1_5/$\overline{\text{RTS}}$/ CT32B0_CAP0	E2	23	30	[3]	no	I/O	I; PU	**PIO1_5 —** General purpose digital input/output pin.
						O	-	**$\overline{\text{RTS}}$ —** Request To Send output for UART.
						I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	D2	24	31	[3]	no	I/O	I; PU	**PIO1_6 —** General purpose digital input/output pin.
						I	-	**RXD —** Receiver input for UART.
						O	-	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.

Table 3. LPC110xLVUK/LPC111xLV pin description table

Symbol	WLCSP25	HVQFN24	HVQFN33		Start logic input	Type	Reset state [1]	Description
PIO1_7/TXD/ CT32B0_MAT1	E1	1	32	[3]	no	I/O	I; PU	**PIO1_7 —** General purpose digital input/output pin.
						O	-	**TXD —** Transmitter output for UART.
						O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	B1	6	7	[3]	no	I/O	I; PU	**PIO1_8 —** General purpose digital input/output pin.
						I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO1_9/ CT16B1_MAT0	B3	-	12	[3]	no	I/O	I; PU	**PIO1_9 —** General purpose digital input/output pin.
						O	-	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO1_10/AD6/ CT16B1_MAT1	-	-	20	[5]	no	I/O	I;PU	**PIO1_10 —** General purpose digital input/output pin.
						I	-	**AD6 —** A/D converter, input 6.
						O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO1_11/AD7/ CT32B0_MAT3	-	-	27	[5]	no	I/O	I;PU	**PIO1_11 —** General purpose digital input/output pin.
						I	-	**AD7 —** A/D converter, input 7.
						O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
PIO2_0/$\overline{\text{DTR}}$	-	-	1	[3]	no	I/O	I;PU	**PIO2_0 —** General purpose digital input/output pin.
						O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART.
PIO2_1/$\overline{\text{DSR}}$	A1	-	-	[3]	no	I/O	I; PU	**PIO2_1 —** General purpose digital input/output pin.
						I	-	**$\overline{\text{DSR}}$ —** Data Set Ready input for UART.
PIO3_4/ CT16B0_CAP1/RXD	-	-	13	[3]	no	I/O	I;PU	**PIO3_4 —** General purpose digital input/output pin.
						I	-	**CT16B0_CAP1 —** Capture input 1 for 16-bit timer 0.
						I	-	**RXD —** Receiver input for UART.
PIO3_5/ CT16B1_CAP1/TXD	-	-	14	[3]	no	I/O	I;PU	**PIO3_5 —** General purpose digital input/output pin.
						I	-	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
						O	-	**TXD —** Transmitter output for UART.
V_{DD}	E3	22	29; 6; 28		-	-	-	1.8 V supply voltage to the core, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	C1	4	4	[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	C2	5	5	[6]	-	O	-	Output from the oscillator amplifier.
V_{SS}	E4	21	33		-	-	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level 0; IA = inactive, no pull-up/down enabled.

[2] See Figure 28 for the reset pad configuration.

[3] Pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 27).

[4] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus.

[5] Pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as an ADC input, digital section of the pad is disabled (see Figure 27).

[6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.10.1 Features

- The I^2C-interface is a standard I^2C-bus compliant interface with open-drain pins. The I^2C-bus interface also supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- The I^2C-bus controller supports multiple address recognition and a bus monitor mode.

7.11 ADC

The LPC111xLV/LPC11xxLVUK contains one ADC. It is a single 8-bit successive approximation ADC with up to eight channels.

Remark: ADC specifications are valid for T_{amb} = -40 °C to +85 °C on HVQFN33 and WLCSP25 packages. ADC specifications are valid for T_{amb} = -10 °C to 85 °C on the HVQFN24 package.

7.11.1 Features

- 8-bit successive approximation ADC.
- Input multiplexing among 6 pins (WLCSP25 and HVQFN24 packages).
- Input multiplexing among 8 pins (HVQFN33 packages).
- Power-down mode.
- Measurement range 0 V to V_{DD}.
- 8-bit sampling rate of up to 10 kSamples/s.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

7.12 General purpose external event counter/timers

The LPC111xLV/LPC11xxLVUK includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.12.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- Up to two capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

7.13 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.14 Windowed WatchDog Timer

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.14.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.

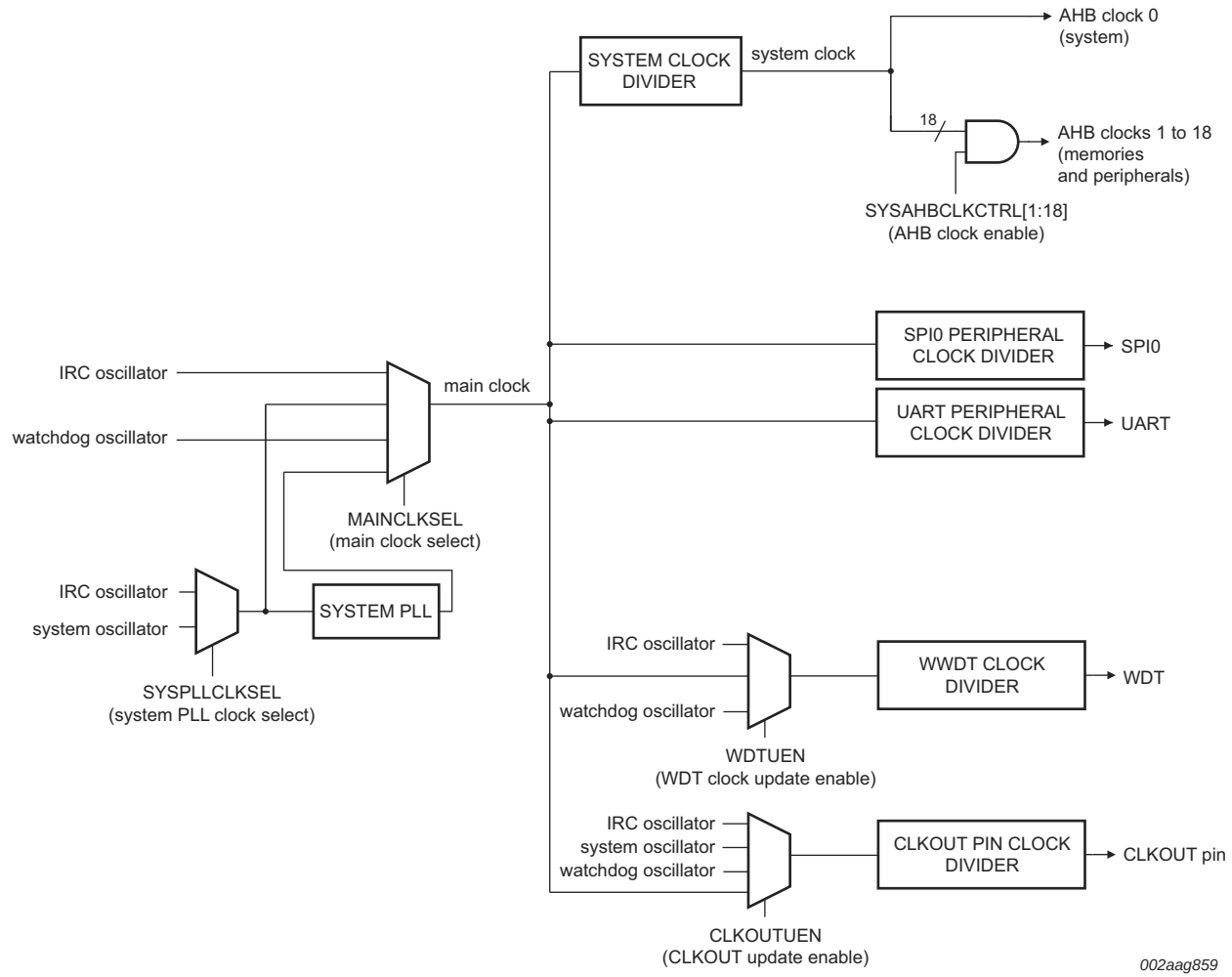


Fig 6. LPC111xLV/LPC11xxLVUK clock generation block diagram

7.15.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 2.5 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC111xLV/LPC11xxLVUK use the IRC as the clock source. Software may later switch to one of the other available clock sources.

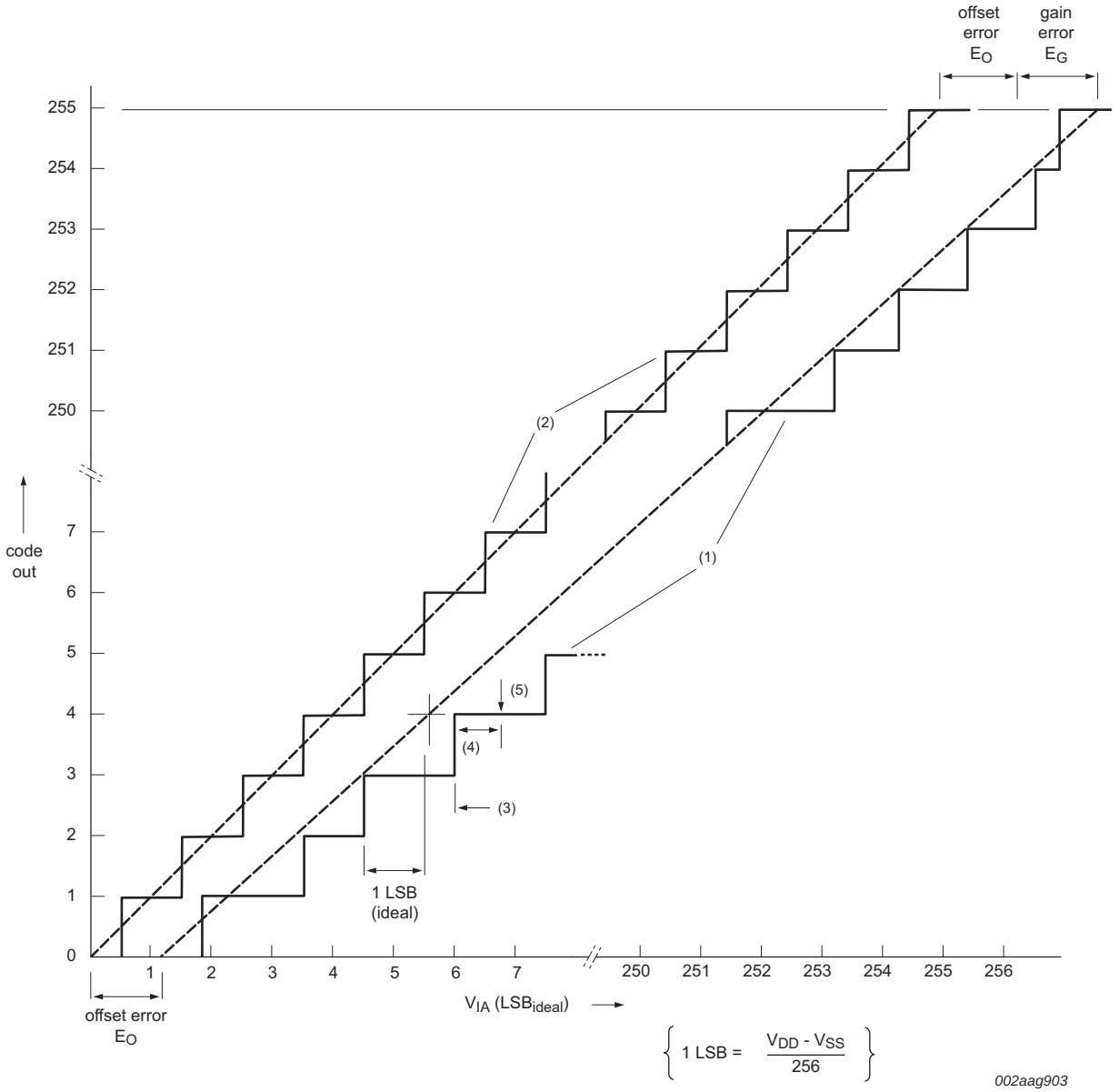
7.15.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

Table 5. Static characteristics (single power supply *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[10]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[10]	-	-	50	mA
I_{pd}	pull-down current	V_I = 1.8 V (V_{DD} = 1.8 V)		10	29	90	μA
I_{pu}	pull-up current	V_I = 0 V; 1.65 V ≤ V_{DD} ≤ 1.95 V		−3	−13	−85	μA
		$V_{DD} < V_I < 3.0$ V		0	0	0	μA
High-drive output pin (PIO0_7)							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function;	[8][9]				
		V_{DD} = 1.8 V		0	-	3.0	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	1.65 V ≤ V_{DD} ≤ 1.95 V; I_{OH} = 10 mA		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	1.65 V ≤ V_{DD} ≤ 1.95 V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD}$ − 0.4 V; 1.65 V ≤ V_{DD} ≤ 1.95 V		10	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 1.65 V ≤ V_{DD} ≤ 1.95 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[10]	-	-	50	mA
I_{pd}	pull-down current	V_I = 1.8 V		10	29	90	μA
I_{pu}	pull-up current	V_I = 0 V; 1.65 V ≤ V_{DD} ≤ 1.95 V		−3	−13	−85	μA
		$V_{DD} < V_I < 3.0$ V		0	0	0	μA



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

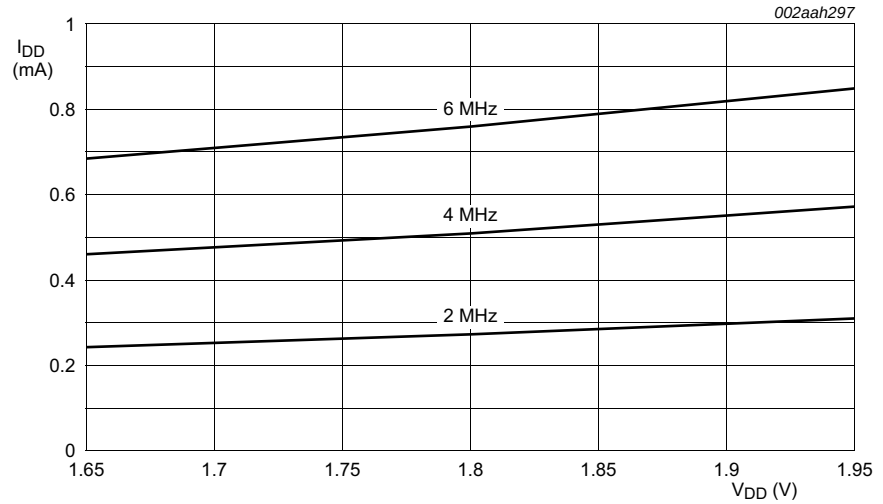
(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

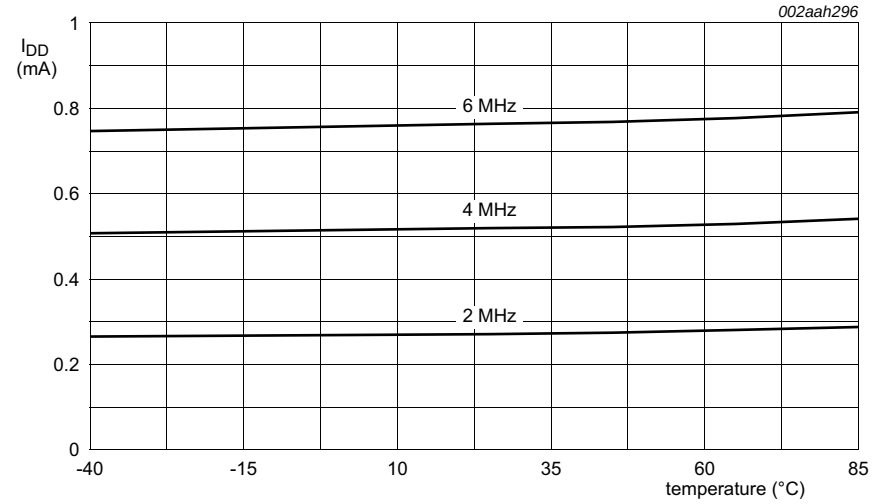
Fig 7. ADC characteristics

9.3 Power consumption



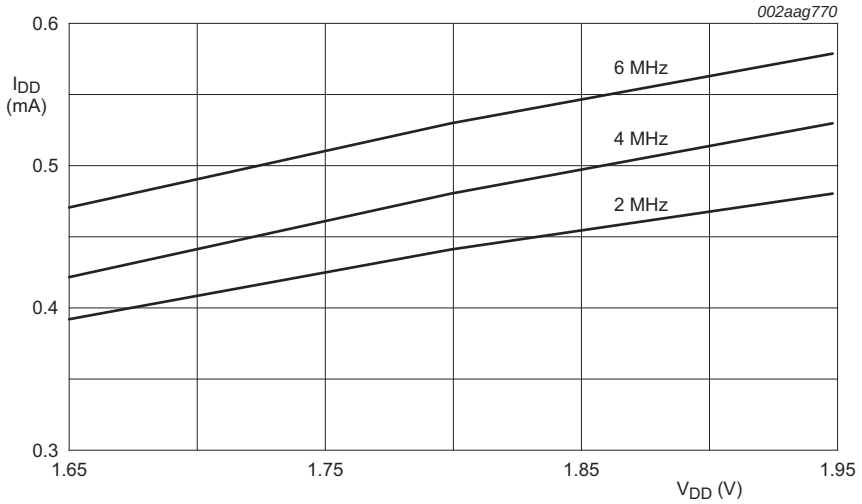
Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; System oscillator, system PLL, IRC, BOD disabled; system clock provided by external clock.

Fig 14. Active mode (2 MHz to 6 MHz): Typical supply current I_{DD} versus supply voltage V_{DD} for different clock frequencies



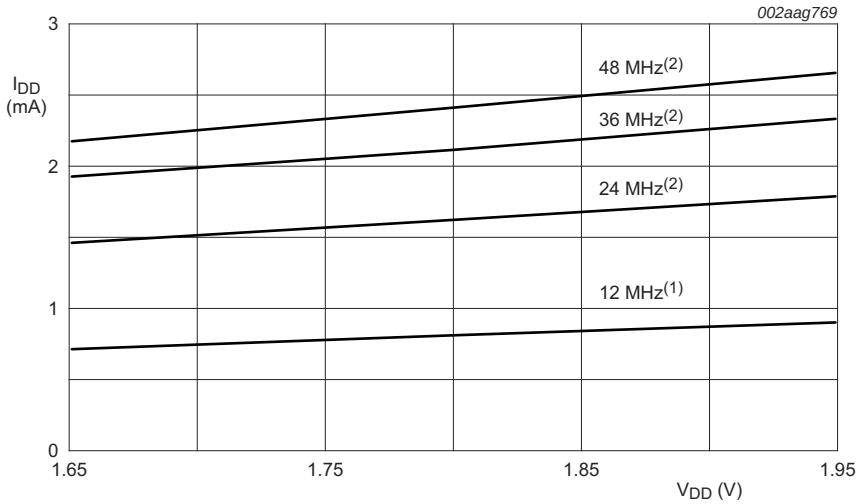
Conditions: V_{DD} = 1.8 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; System oscillator, system PLL, IRC, BOD disabled; system clock provided by external clock.

Fig 15. Active mode (2 MHz to 6 MHz): Typical supply current I_{DD} versus temperature for different clock frequencies



Conditions: T_{amb} = 25 °C; Sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; System oscillator and system PLL disabled; IRC disabled; system clock provided by external clock.

Fig 18. Sleep mode (2 MHz to 6 MHz): Typical supply current I_{DD} versus supply voltage V_{DD} for different clock frequencies



Conditions: T_{amb} = 25 °C; Sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 19. Sleep mode (12 MHz to 48 MHz): Typical supply current I_{DD} versus supply voltage V_{DD} for different clock frequencies

9.4 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

Table 7. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.26	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.18	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	0.004	-	-	System oscillator running; PLL off; independent of main clock frequency.
Main PLL	-	0.061	-	
ADC	-	0.08	0.29	
CLKOUT	-	0.18	0.45	Main clock divided by 4 in the CLKOUTDIV register.
CT16B0	-	0.02	0.06	
CT16B1	-	0.02	0.06	
CT32B0	-	0.02	0.07	
CT32B1	-	0.02	0.06	
GPIO	-	0.23	0.88	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCON	-	0.03	0.10	
I2C	-	0.04	0.13	
ROM	-	0.04	0.15	
SPI0	-	0.12	0.45	
UART	-	0.22	0.82	
WWDT	-	0.02	0.06	Main clock selected as clock source for the WWDT.

9.5 BOD static characteristics

Table 8. BOD static characteristics

T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	reset level 0				
		assertion	-	1.46	-	V
		de-assertion	-	1.63	-	V

10.3 Internal oscillators

Table 11. Dynamic characteristic: internal oscillators
V_{DD} = 1.65V to 1.95 V.

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	*-20 °C ≤ T_{amb} ≤ +85 °C*	12 - 2.5 %	12	12 + 2.5 %	MHz
		-40 °C ≤ T_{amb} < -20 °C	12 - 5 %	12	12 + 5 %	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

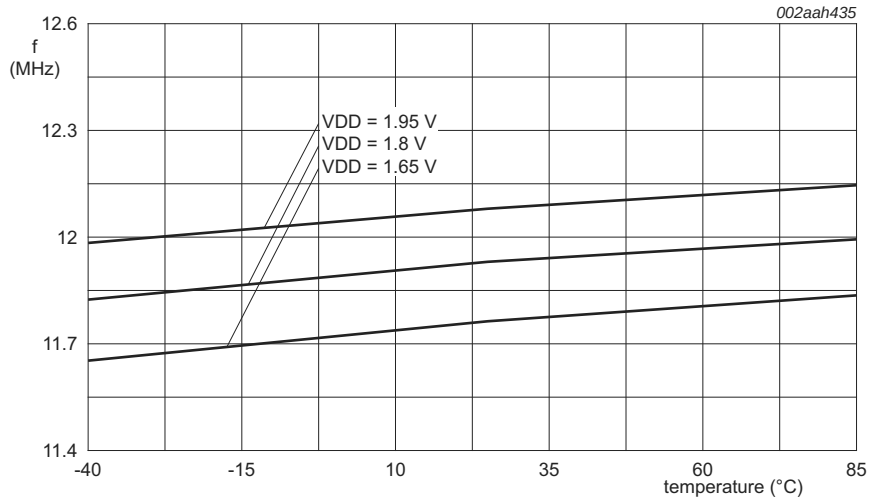


Fig 23. Typical internal RC oscillator frequency for different supply voltages V_{DD}

Table 12. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +85 °C) is ±40 %.

[3] See the *LPC111xLV user manual*.

10.4 I²C-bus

Table 13. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	Standard-mode	0	100	kHz
		Fast-mode	0	400	kHz
		Fast-mode Plus	0	1	MHz

Table 13. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals	-	300	ns
			Standard-mode			
			Fast-mode	$20 + 0.1 \times C_b$	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

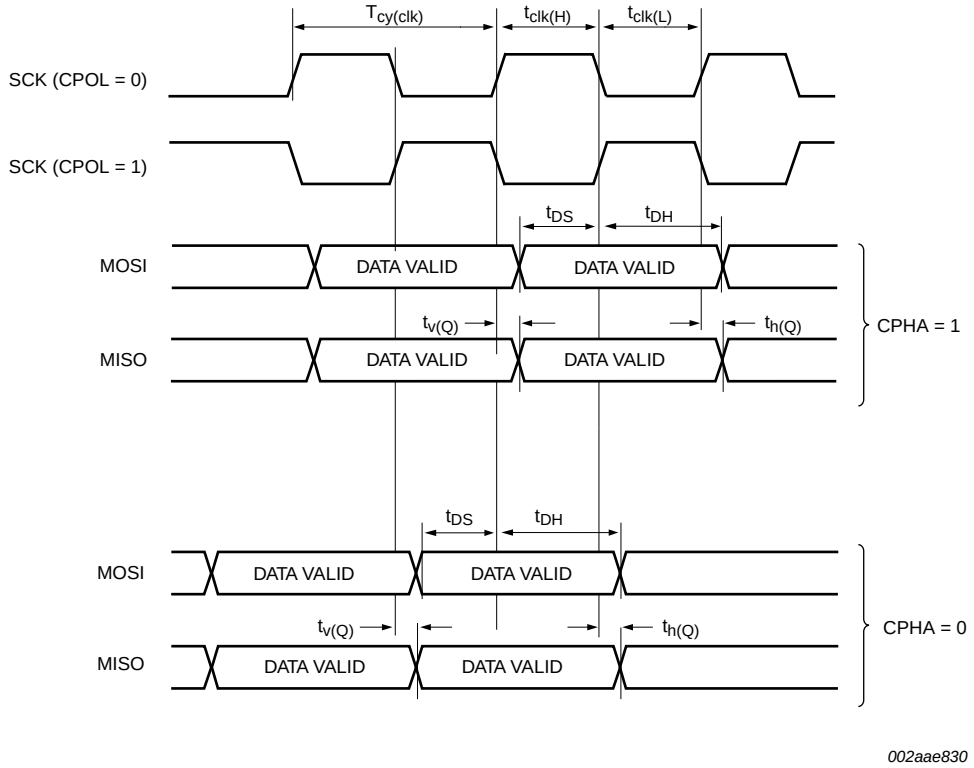
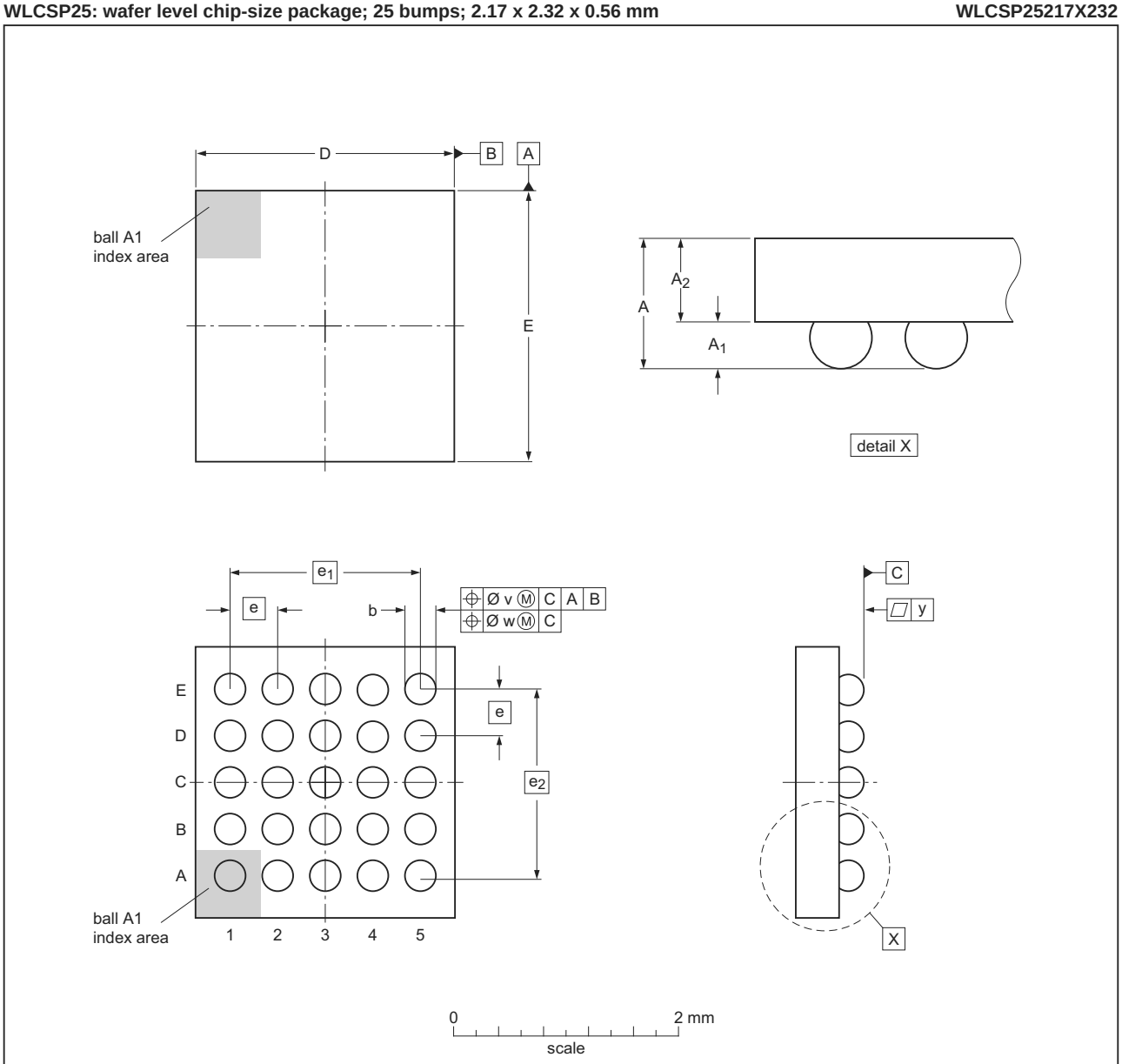


Fig 26. SPI slave timing in SPI mode

12. Package outline

WLCSP25: wafer level chip-size package; 25 bumps; 2.17 x 2.32 x 0.56 mm **WLCSP25217X232**



Dimensions (mm are the original dimensions)

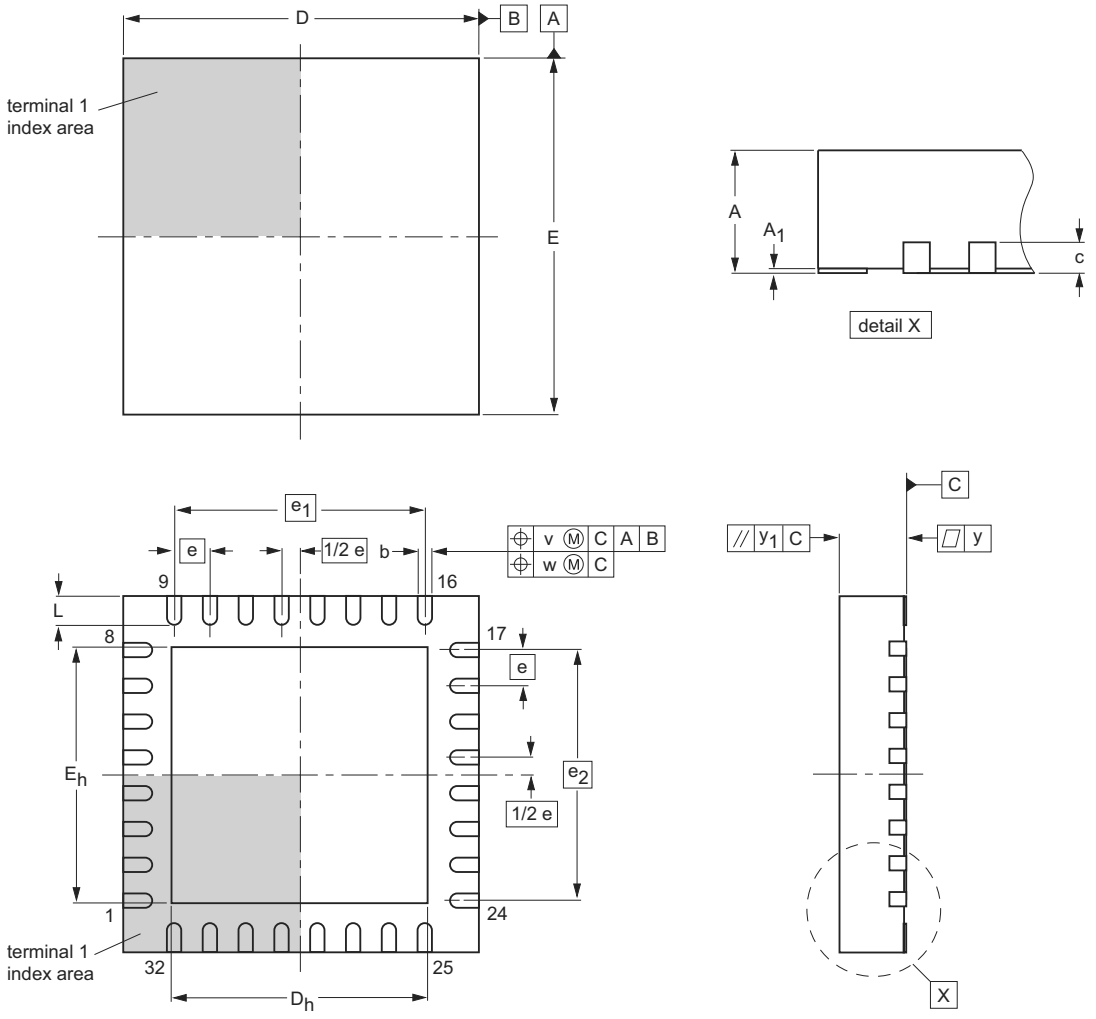
Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
	max	0.615	0.23	0.385	0.29	2.21	2.36						
mm	nom	0.560	0.20	0.360	0.26	2.17	2.32	0.4	1.6	1.6	0.15	0.05	0.05
	min	0.505	0.17	0.335	0.23	2.13	2.28						

wlcsp25_217x232_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
WLCSP25217X232						~~11-05-04~~ 12-02-13

Fig 29. Package outline (WLCSP25)

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm



Dimensions (mm are the original dimensions)

Unit[1]		A[1]	A_1	b	c	D[1]	D_h	E[1]	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	0.85	0.05	0.30	0.2	5.1	3.75	5.1	3.75	0.5	3.5	3.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

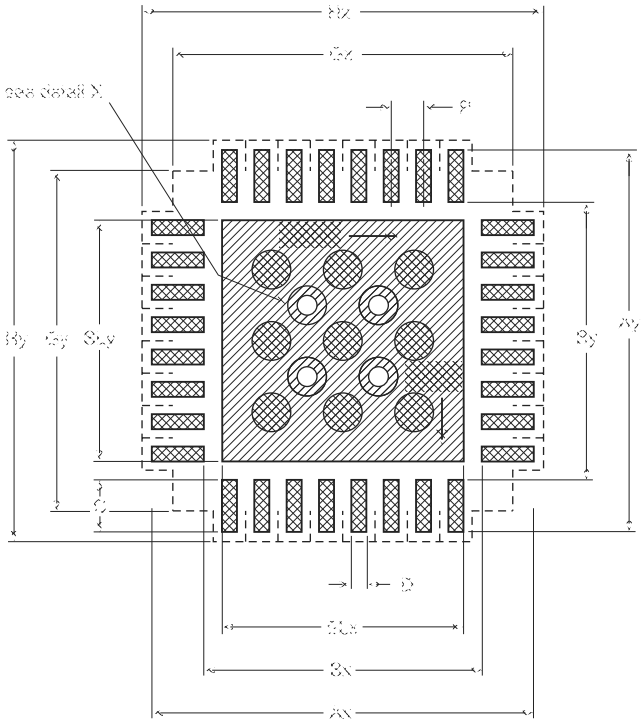
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

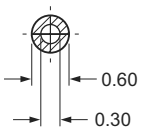
hvqfn33f_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		MO-220				~~11-10-11~~ 11-10-17

Fig 31. Package outline (HVQFN33)

Footprint information for reflow soldering of HVQFN33 package





detail X

solder land

solder paste

occupied area

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	nSPx	nSPy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	5.25	5.25	6.2	6.2	3.75	3.75	3	3

Issue date ~~11-11-15~~ 11-11-20

002aag766

Fig 33. Reflow soldering for the HVQFN33 (5x5) package

14. Abbreviations

Table 15. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	Brown-Out Detect
GPIO	General-Purpose Input/Output
JEDEC	Joint Electron Devices Engineering Council
NVM	Non-Volatile Memory
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
TTL	Transistor-Transistor Logic
USART	Universal Synchronous Asynchronous Receiver/Transmitter

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