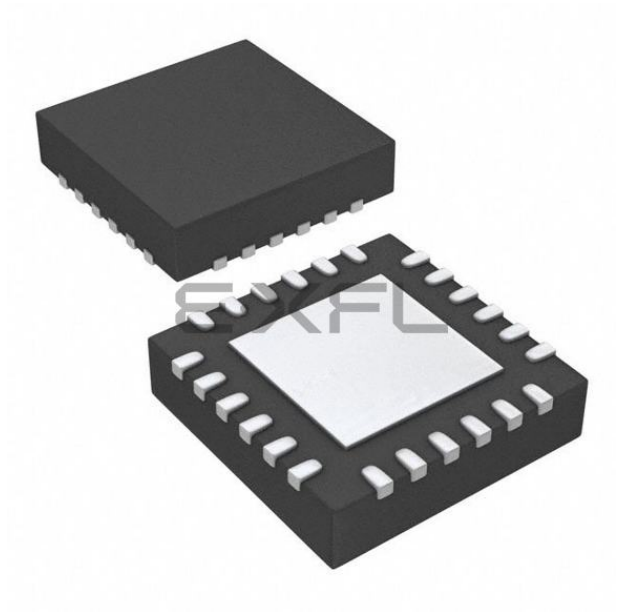


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, WDT |
| Number of I/O | 20 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 1.95V |
| Data Converters | A/D 8x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 24-VFQFN Exposed Pad |
| Supplier Device Package | 24-HVQFN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1114lvfhn24-303 |

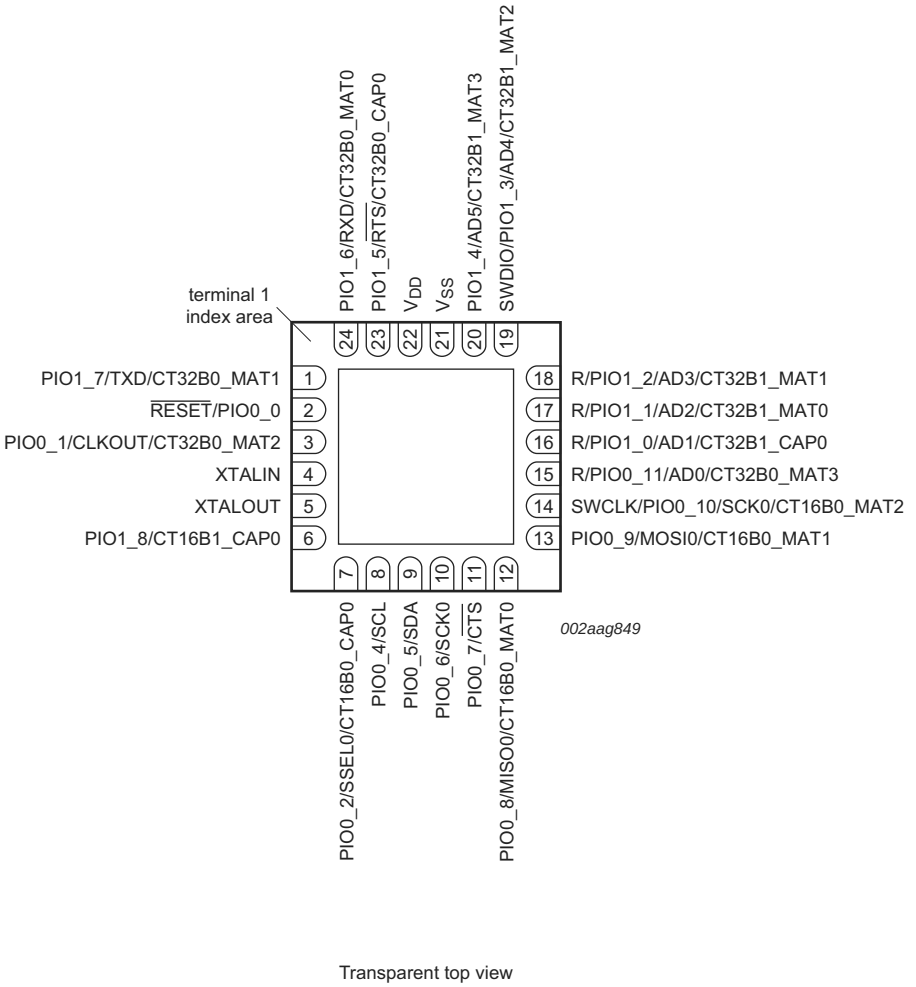
**Table 1. Ordering information** *…continued*

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| LPC1114LVFHN24/303 | HVQFN24 | plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm | SOT616-3 |
| LPC1112LVFHI33/103 | HVQFN33 | plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm | n/a |
| LPC1114LVFHI33/303 | HVQFN33 | plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm | n/a |

## 4.1 Ordering options

**Table 2. Ordering options**

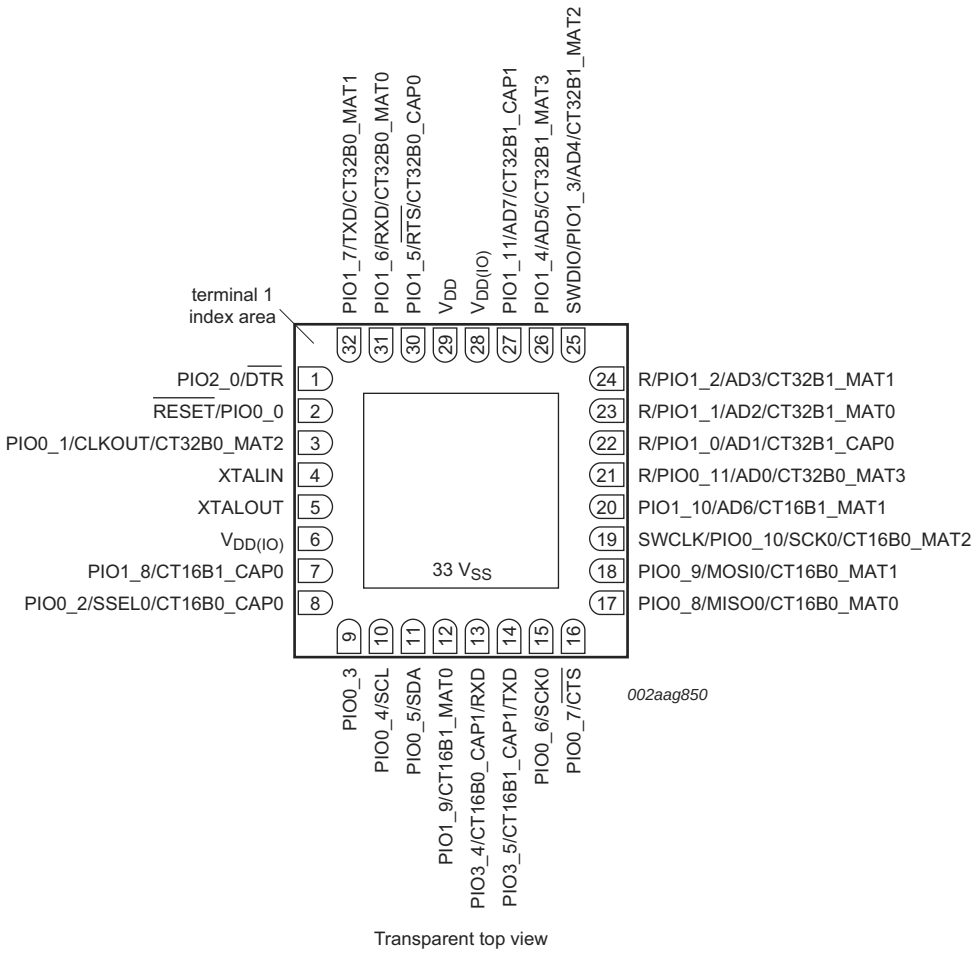
| Type number | Flash in kB | Total SRAM in kB | SPI/ SSP | I2C | UART | ADC | GPIO pins | Package |
|---|---|---|---|---|---|---|---|---|
| LPC1101LVUK | 32 | 2 | 1 | 1 | 1 | 6-channel | 21 | WLCSP25 |
| LPC1102LVUK | 32 | 8 | 1 | 1 | 1 | 6-channel | 21 | WLCSP25 |
| LPC1112LVFHN24/003 | 16 | 2 | 1 | 1 | 1 | 6-channel | 20 | HVQFN24 |
| LPC1114LVFHN24/103 | 32 | 4 | 1 | 1 | 1 | 6-channel | 20 | HVQFN24 |
| LPC1114LVFHN24/303 | 32 | 8 | 1 | 1 | 1 | 6-channel | 20 | HVQFN24 |
| LPC1112LVFHI33/103 | 16 | 4 | 1 | 1 | 1 | 8-channel | 27 | HVQFN33 |
| LPC1114LVFHI33/303 | 32 | 8 | 1 | 1 | 1 | 8-channel | 27 | HVQFN33 |




Transparent top view

For parts LPC1112LVFHN24/003, LPC1114LVFHN24/103, LPC1114LVFHN24/303.

**Fig 3. Pin configuration HVQFN24 package**




For parts LPC1112LVFHI33/103 and LPC1114LVFHI33/303.

**Fig 4. Pin configuration HVQFN33 package**

**Table 3. LPC110xLVUK/LPC111xLV pin description table**

| Symbol | WLCSP25 | HVQFN24 | HVQFN33 | | Start logic input | Type | Reset state [1] | Description |
|---|---|---|---|---|---|---|---|---|
| SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2 | B4 | 14 | 19 | [3] | yes | I | I; PU | **SWCLK —** Serial wire clock. |
| | | | | | | I/O | - | **PIO0_10 —** General purpose digital input/output pin. |
| | | | | | | I/O | - | **SCK0 —** Serial clock for SPI0. |
| | | | | | | O | - | **CT16B0_MAT2 —** Match output 2 for 16-bit timer 0. |
| R/PIO0_11/ AD0/CT32B0_MAT3 | C5 | 15 | 21 | [5] | yes | I | I; PU | **R —** Reserved. Configure for an alternate function in the IOCON block. |
| | | | | | | I/O | - | **PIO0_11 —** General purpose digital input/output pin. |
| | | | | | | I | - | **AD0 —** A/D converter, input 0. |
| | | | | | | O | - | **CT32B0_MAT3 —** Match output 3 for 32-bit timer 0. |
| R/PIO1_0/ AD1/CT32B1_CAP0 | C4 | 16 | 22 | [5] | yes | I | I; PU | **R —** Reserved. Configure for an alternate function in the IOCON block. |
| | | | | | | I/O | - | **PIO1_0 —** General purpose digital input/output pin. |
| | | | | | | I | - | **AD1 —** A/D converter, input 1. |
| | | | | | | I | - | **CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1. |
| R/PIO1_1/ AD2/CT32B1_MAT0 | D5 | 17 | 23 | [5] | no | O | I; PU | **R —** Reserved. Configure for an alternate function in the IOCON block. |
| | | | | | | I/O | - | **PIO1_1 —** General purpose digital input/output pin. |
| | | | | | | I | - | **AD2 —** A/D converter, input 2. |
| | | | | | | O | - | **CT32B1_MAT0 —** Match output 0 for 32-bit timer 1. |
| R/PIO1_2/ AD3/CT32B1_MAT1 | D4 | 18 | 24 | [5] | no | I | I; PU | **R —** Reserved. Configure for an alternate function in the IOCON block. |
| | | | | | | I/O | - | **PIO1_2 —** General purpose digital input/output pin. |
| | | | | | | I | - | **AD3 —** A/D converter, input 3. |
| | | | | | | O | - | **CT32B1_MAT1 —** Match output 1 for 32-bit timer 1. |
| SWDIO/PIO1_3/ AD4/CT32B1_MAT2 | E5 | 19 | 25 | [5] | no | I/O | I; PU | **SWDIO —** Serial wire debug input/output. |
| | | | | | | I/O | - | **PIO1_3 —** General purpose digital input/output pin. |
| | | | | | | I | - | **AD4 —** A/D converter, input 4. |
| | | | | | | O | - | **CT32B1_MAT2 —** Match output 2 for 32-bit timer 1. |
| PIO1_4/AD5/ CT32B1_MAT3 | D3 | 20 | 26 | [5] | no | I/O | I; PU | **PIO1_4 —** General purpose digital input/output pin with 10 ns glitch filter. |
| | | | | | | I | - | **AD5 —** A/D converter, input 5. |
| | | | | | | O | - | **CT32B1_MAT3 —** Match output 3 for 32-bit timer 1. |
| PIO1_5/$\overline{\text{RTS}}$/ CT32B0_CAP0 | E2 | 23 | 30 | [3] | no | I/O | I; PU | **PIO1_5 —** General purpose digital input/output pin. |
| | | | | | | O | - | **$\overline{\text{RTS}}$ —** Request To Send output for UART. |
| | | | | | | I | - | **CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0. |
| PIO1_6/RXD/ CT32B0_MAT0 | D2 | 24 | 31 | [3] | no | I/O | I; PU | **PIO1_6 —** General purpose digital input/output pin. |
| | | | | | | I | - | **RXD —** Receiver input for UART. |
| | | | | | | O | - | **CT32B0_MAT0 —** Match output 0 for 32-bit timer 0. |

# 7. Functional description

## 7.1 ARM Cortex-M0 processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption.

## 7.2 On-chip flash program memory

The LPC111xLV/LPC11xxLVUK contains up to 32 kB of on-chip flash memory.

The flash memory is divided into 4 kB sectors with each sector consisting of 16 pages. Individual pages of 256 byte each can be erased using the IAP erase page command.

## 7.3 On-chip SRAM

The LPC111xLV/LPC11xxLVUK contains up to 8 kB on-chip static RAM memory.

## 7.4 Memory map

The LPC111xLV/LPC11xxLVUK incorporates several distinct memory regions, shown in the following figures. Figure 5 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 megabyte in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kilobytes of space. This allows simplifying the address decoding for each peripheral.

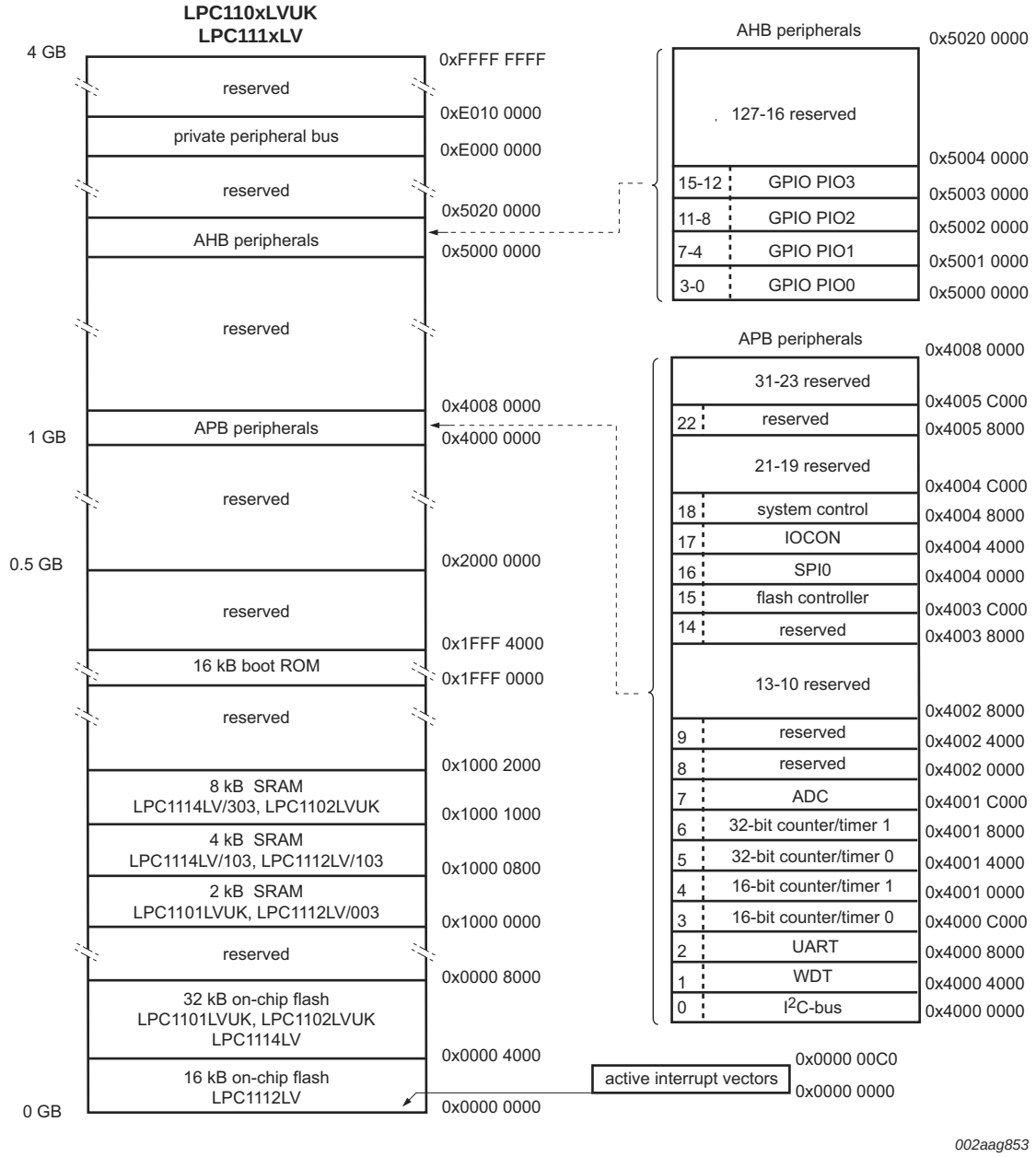



**Fig 5. LPC111xLV/LPC11xxLVUK memory map**

## 7.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

### 7.5.1 Features

- Controls system exceptions and peripheral interrupts.

- In the LPC111xLV/LPC11xxLVUK, the NVIC supports 32 vectored interrupts including up to 13 inputs to the start logic from individual GPIO pins.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation.

### 7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any GPIO pin (total of up to 18 pins) regardless of the selected function, can be programmed to generate an interrupt on a level, or rising edge or falling edge, or both.

## 7.6 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

## 7.7 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC111xLV/LPC11xxLVUK use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Additionally, any GPIO pin (total of up to 18 pins) providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

### 7.7.1 Features

- Bit level port registers allow a single instruction to set or clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with pull-ups enabled after reset with the exception of the $I^2C$-bus pins PIO0_4 and PIO0_5.
- Pull-up/pull-down resistor configuration can be programmed through the IOCON block for each GPIO pin (except for pins PIO0_4 and PIO0_5).
- All GPIO pins (except PIO0_4 and PIO0_5) are pulled up to 1.8 V ($V_{DD}$ = 1.8 V) if their pull-up resistor is enabled in the IOCON block (single power supply).
- Programmable open-drain mode.

## 7.8 UART

The LPC111xLV/LPC11xxLVUK contains one UART.

Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The UART includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

### 7.8.1 Features

- Maximum UART data bit rate of 3.125 MBit/s.
- 16 Byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.

## 7.9 SPI serial I/O controller

The LPC111xLV/LPC11xxLVUK contains one SPI controller.

The SPI controller is capable of operation on an SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SPI supports full-duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

### 7.9.1 Features

- Maximum SPI speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

## 7.10 $I^2C$-bus serial I/O controller

The LPC111xLV/LPC11xxLVUK contains one $I^2C$-bus controller.

The $I^2C$-bus is bidirectional for inter-IC control using only two wires: a Serial Clock Line (SCL) and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the

capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The $I^2C$ is a multi-master bus and can be controlled by more than one bus master connected to it.

### 7.10.1 Features

- The $I^2C$-interface is a standard $I^2C$-bus compliant interface with open-drain pins. The $I^2C$-bus interface also supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The $I^2C$-bus can be used for test and diagnostic purposes.
- The $I^2C$-bus controller supports multiple address recognition and a bus monitor mode.

## 7.11 ADC

The LPC111xLV/LPC11xxLVUK contains one ADC. It is a single 8-bit successive approximation ADC with up to eight channels.

**Remark:** ADC specifications are valid for $T_{amb}$ = -40 °C to +85 °C on HVQFN33 and WLCSP25 packages. ADC specifications are valid for $T_{amb}$ = -10 °C to 85 °C on the HVQFN24 package.

### 7.11.1 Features

- 8-bit successive approximation ADC.
- Input multiplexing among 6 pins (WLCSP25 and HVQFN24 packages).
- Input multiplexing among 8 pins (HVQFN33 packages).
- Power-down mode.
- Measurement range 0 V to $V_{DD}$.
- 8-bit sampling rate of up to 10 kSamples/s.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

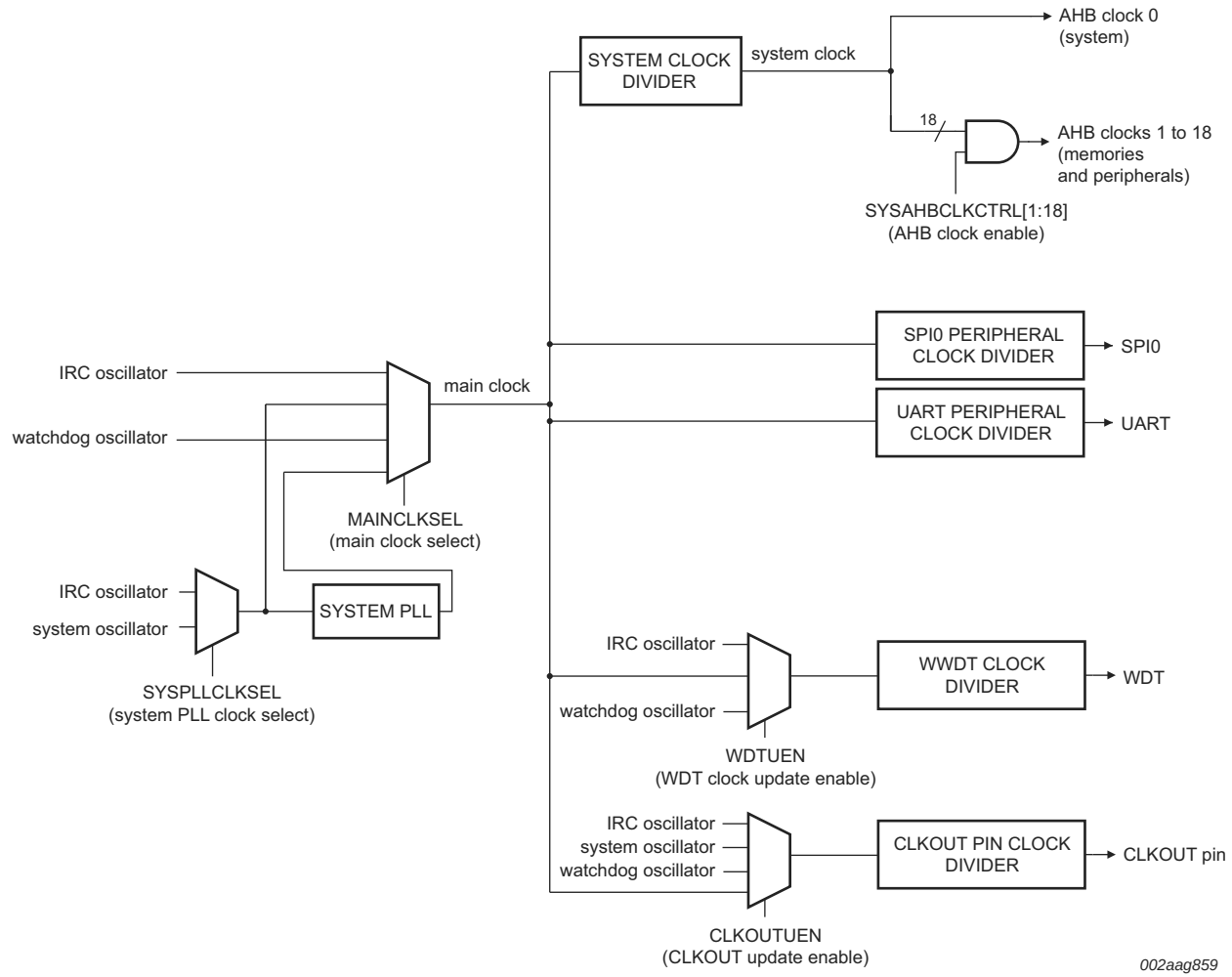



**Fig 6. LPC111xLV/LPC11xxLVUK clock generation block diagram**

#### 7.15.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 2.5 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC111xLV/LPC11xxLVUK use the IRC as the clock source. Software may later switch to one of the other available clock sources.

#### 7.15.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

# 8. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*[1]

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage (core and external rail) | | | 1.65 | 1.95 | V |
| $V_I$ | input voltage | only valid when the $V_{DD}$ supply voltage is present<br>$1.65\ V \leq V_{DD} < 1.8\ V$ | [2] | −0.5 | +3.0 | V |
| | | $V_{DD} \geq 1.8\ V$ | | −0.5 | +5.0 | V |
| $I_{DD}$ | supply current | per supply pin | | - | 100 | mA |
| $I_{SS}$ | ground current | per ground pin | | - | 100 | mA |
| $I_{latch}$ | I/O latch-up current | $-(0.5V_{DD}) < V_I < (1.5V_{DD})$;<br>$T_j < 125\ °C$ | | - | 100 | mA |
| $T_{stg}$ | storage temperature | non-operating | [3] | −65 | +150 | °C |
| $T_{j(max)}$ | maximum junction temperature | | | - | 150 | °C |
| $P_{tot(pack)}$ | total power dissipation (per package) | based on package heat transfer, not device power consumption | | - | 1.5 | W |
| $V_{ESD}$ | electrostatic discharge voltage | human body model; all pins | [4] | −6500 | +6500 | V |

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to $V_{SS}$ unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Refer to the JEDEC spec (J-STD-033B.1) for further details.

[4] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

**Table 5. Static characteristics (single power supply** *…continued*
*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{OHS}$ | HIGH-level short-circuit output current | $V_{OH}$ = 0 V | [10] | - | - | −45 | mA |
| $I_{OLS}$ | LOW-level short-circuit output current | $V_{OL} = V_{DD}$ | [10] | - | - | 50 | mA |
| $I_{pd}$ | pull-down current | $V_I$ = 1.8 V ($V_{DD}$ = 1.8 V) | | 10 | 29 | 90 | μA |
| $I_{pu}$ | pull-up current | $V_I$ = 0 V; 1.65 V ≤ $V_{DD}$ ≤ 1.95 V | | −3 | −13 | −85 | μA |
| | | $V_{DD} < V_I < 3.0$ V | | 0 | 0 | 0 | μA |
| **High-drive output pin (PIO0_7)** | | | | | | | |
| $I_{IL}$ | LOW-level input current | $V_I$ = 0 V; on-chip pull-up resistor disabled | | - | 0.5 | 10 | nA |
| $I_{IH}$ | HIGH-level input current | $V_I = V_{DD}$; on-chip pull-down resistor disabled | | - | 0.5 | 10 | nA |
| $I_{OZ}$ | OFF-state output current | $V_O$ = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled | | - | 0.5 | 10 | nA |
| $V_I$ | input voltage | pin configured to provide a digital function; | [8][9] | | | | |
| | | $V_{DD}$ = 1.8 V | | 0 | - | 3.0 | V |
| $V_O$ | output voltage | output active | | 0 | - | $V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | $0.7V_{DD}$ | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | | - | - | $0.3V_{DD}$ | V |
| $V_{hys}$ | hysteresis voltage | | | - | 0.4 | - | V |
| $V_{OH}$ | HIGH-level output voltage | 1.65 V ≤ $V_{DD}$ ≤ 1.95 V; $I_{OH}$ = 10 mA | | $V_{DD}$ − 0.4 | - | - | V |
| $V_{OL}$ | LOW-level output voltage | 1.65 V ≤ $V_{DD}$ ≤ 1.95 V; $I_{OL}$ = 3 mA | | - | - | 0.4 | V |
| $I_{OH}$ | HIGH-level output current | $V_{OH} = V_{DD}$ − 0.4 V; 1.65 V ≤ $V_{DD}$ ≤ 1.95 V | | 10 | - | - | mA |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V 1.65 V ≤ $V_{DD}$ ≤ 1.95 V | | 3 | - | - | mA |
| $I_{OLS}$ | LOW-level short-circuit output current | $V_{OL} = V_{DD}$ | [10] | - | - | 50 | mA |
| $I_{pd}$ | pull-down current | $V_I$ = 1.8 V | | 10 | 29 | 90 | μA |
| $I_{pu}$ | pull-up current | $V_I$ = 0 V; 1.65 V ≤ $V_{DD}$ ≤ 1.95 V | | −3 | −13 | −85 | μA |
| | | $V_{DD} < V_I < 3.0$ V | | 0 | 0 | 0 | μA |

**Table 5. Static characteristics (single power supply** *…continued*
*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| **I²C-bus pins (PIO0_4 and PIO0_5)** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | | $0.7V_{DD}$ | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | | - | - | $0.3V_{DD}$ | V |
| $V_{hys}$ | hysteresis voltage | | | - | $0.05V_{DD}$ | - | V |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V; I²C-bus pins configured as standard mode pins<br>1.65 V ≤ $V_{DD}$ ≤ 1.95 V | | 2.5 | - | - | mA |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V; I²C-bus pins configured as Fast-mode Plus pins<br>1.65 V ≤ $V_{DD}$ ≤ 1.95 V; | | 15 | - | - | mA |
| $I_{LI}$ | input leakage current | $V_I = V_{DD}$ | [11] | - | 2 | 4 | μA |
| **Oscillator pins** | | | | | | | |
| $V_{i(xtal)}$ | crystal input voltage | | | −0.5 | 1.8 | 1.95 | V |
| $V_{o(xtal)}$ | crystal output voltage | | | −0.5 | 1.8 | 1.95 | V |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] $T_{amb}$ = 25 °C.

[3] $I_{DD}$ measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled. BOD disabled for all measurements.

[4] IRC enabled; system oscillator disabled; system PLL disabled.

[5] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to UART and SPI0 disabled in system configuration block.

[6] IRC disabled; system oscillator enabled; system PLL enabled.

[7] All oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 18FF.

[8] Including voltage on outputs in 3-state mode.

[9] $V_{DD}$ supply voltage must be present.

[10] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

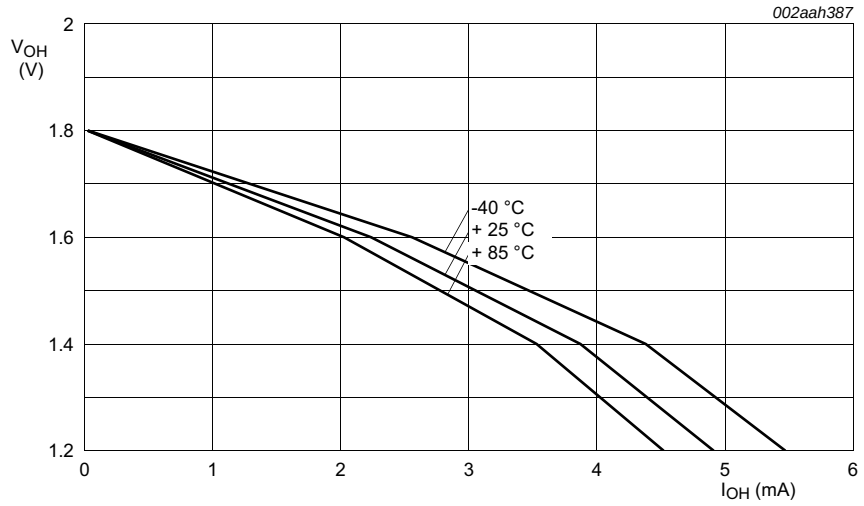
[11] To $V_{SS}$.

### 9.1.1 Analog characteristics

**Remark:** ADC specifications are valid for $T_{amb}$ = -40 °C to +85 °C on HVQFN33 and WLCSP25 packages. ADC specifications are valid for $T_{amb}$ = -10 °C to +85 °C on the HVQFN24 package.

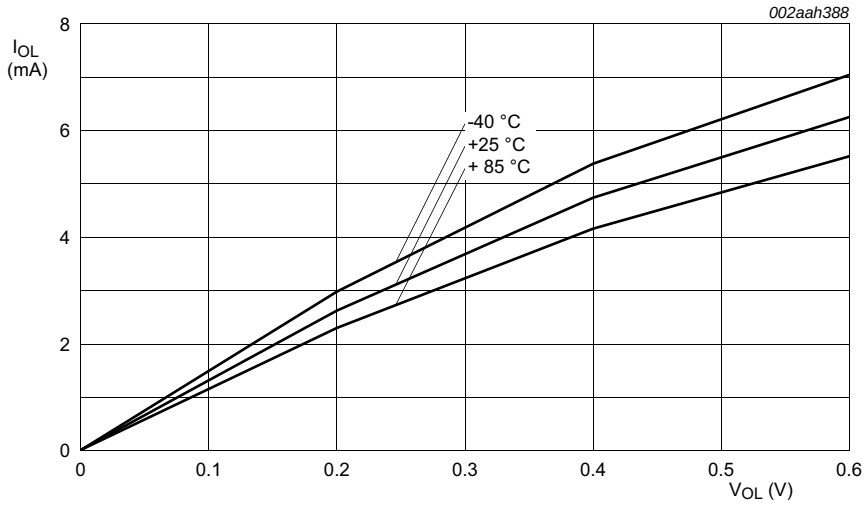
**Table 6. 8-bit ADC static characteristics**
*$T_{amb}$ = −40 °C to +85 °C for HVQFN33 and WLCSP25 packages. $T_{amb}$ = −10 °C to +85 °C for the HVQFN24 package. $V_{DD}$ = 1.8 V ± 5 %; 8-bit resolution.*

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IA}$ | analog input voltage | | 0 | - | $V_{DD}$ | V |
| $C_{ia}$ | analog input capacitance | | - | - | 1 | pF |
| DNL | differential non-linearity | [1][2] | - | - | ± 1 | LSB |
| INL | integral non-linearity | [3] | - | - | ± 1.5 | LSB |
| $E_O$ | offset error | [4] | - | - | ± 1 | LSB |



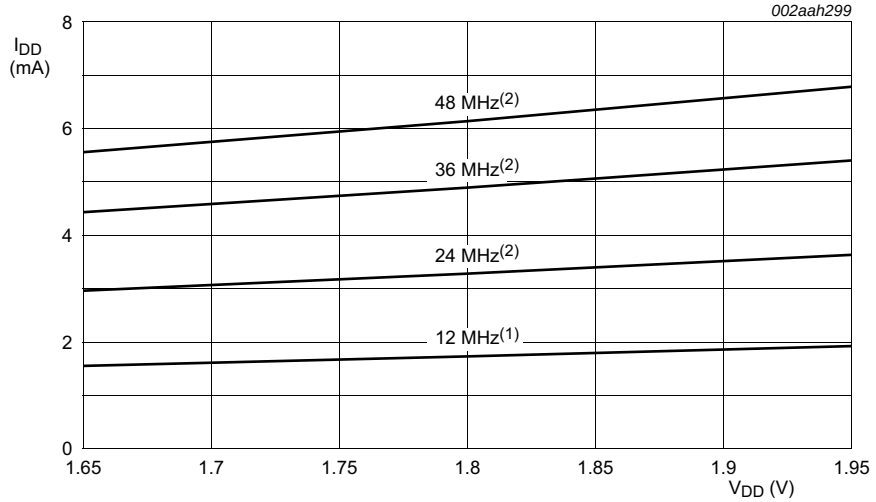

Conditions: standard port pins; $V_{DD}$ = 1.8 V.

**Fig 10. Typical HIGH-level output voltage $V_{OH}$ versus HIGH-level output source current $I_{OH}$**




Conditions: standard port pins; $V_{DD}$ = 1.8 V.

**Fig 11. Typical LOW-level output current $I_{OL}$ versus LOW-level output voltage $V_{OL}$**

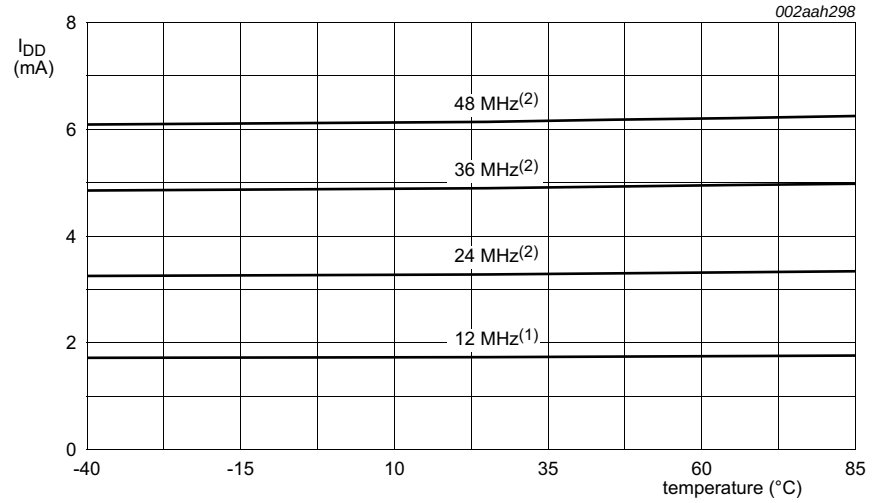



Conditions: $T_{amb}$ = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

**Fig 16. Active mode: Typical supply current $I_{DD}$ versus supply voltage for different system clock frequencies**




Conditions: $V_{DD}$ = 1.8 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

**Fig 17. Active mode: Typical supply current $I_{DD}$ versus temperature for different system clock frequencies**

## 9.4 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at $T_{amb}$ = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

**Table 7. Power consumption for individual analog and digital blocks**

| Peripheral | Typical supply current in mA | | | Notes |
|---|---|---|---|---|
| | n/a | 12 MHz | 48 MHz | |
| IRC | 0.26 | - | - | System oscillator running; PLL off; independent of main clock frequency. |
| System oscillator at 12 MHz | 0.18 | - | - | IRC running; PLL off; independent of main clock frequency. |
| Watchdog oscillator at 500 kHz/2 | 0.004 | - | - | System oscillator running; PLL off; independent of main clock frequency. |
| Main PLL | - | 0.061 | - | |
| ADC | - | 0.08 | 0.29 | |
| CLKOUT | - | 0.18 | 0.45 | Main clock divided by 4 in the CLKOUTDIV register. |
| CT16B0 | - | 0.02 | 0.06 | |
| CT16B1 | - | 0.02 | 0.06 | |
| CT32B0 | - | 0.02 | 0.07 | |
| CT32B1 | - | 0.02 | 0.06 | |
| GPIO | - | 0.23 | 0.88 | GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register. |
| IOCON | - | 0.03 | 0.10 | |
| I2C | - | 0.04 | 0.13 | |
| ROM | - | 0.04 | 0.15 | |
| SPI0 | - | 0.12 | 0.45 | |
| UART | - | 0.22 | 0.82 | |
| WWDT | - | 0.02 | 0.06 | Main clock selected as clock source for the WWDT. |

## 9.5 BOD static characteristics

**Table 8. BOD static characteristics**

*$T_{amb}$ = 25 °C.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{th}$ | threshold voltage | reset level 0 | | | | |
| | | assertion | - | 1.46 | - | V |
| | | de-assertion | - | 1.63 | - | V |

## 10.3 Internal oscillators

**Table 11. Dynamic characteristic: internal oscillators**
*$V_{DD}$ = 1.65V to 1.95 V.*

| Symbol | Parameter | Conditions | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{osc(RC)}$ | internal RC oscillator frequency | *-20 °C ≤ $T_{amb}$ ≤ +85 °C* | 12 - 2.5 % | 12 | 12 + 2.5 % | MHz |
| | | *-40 °C ≤ $T_{amb}$ < -20 °C* | 12 - 5 % | 12 | 12 + 5 % | MHz |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

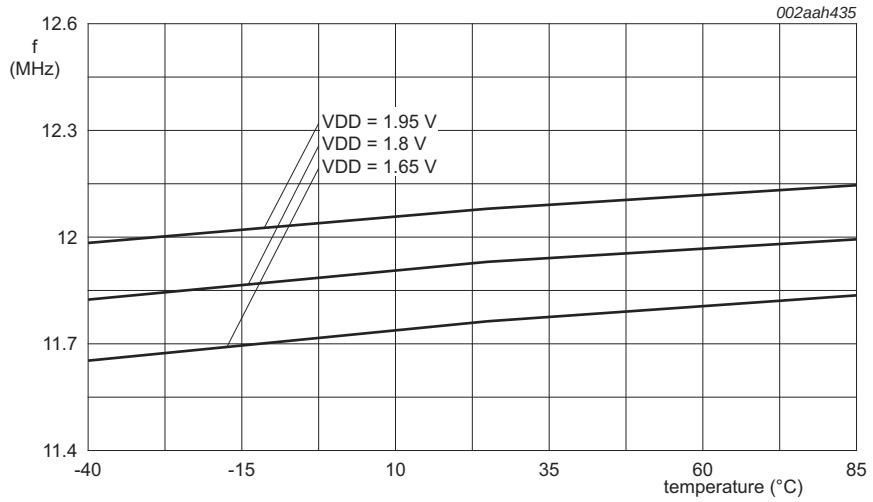



**Fig 23. Typical internal RC oscillator frequency for different supply voltages $V_{DD}$**

**Table 12. Dynamic characteristics: Watchdog oscillator**

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{osc(int)}$ | internal oscillator frequency | DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register; | [2][3] | - | 9.4 | - | kHz |
| | | DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register | [2][3] | - | 2300 | - | kHz |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature ($T_{amb}$ = −40 °C to +85 °C) is ±40 %.

[3] See the *LPC111xLV user manual*.

## 10.4 I²C-bus

**Table 13. Dynamic characteristic: I²C-bus pins[1]**
*$T_{amb}$ = −40 °C to +85 °C.[2]*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | Standard-mode | 0 | 100 | kHz |
| | | Fast-mode | 0 | 400 | kHz |
| | | Fast-mode Plus | 0 | 1 | MHz |

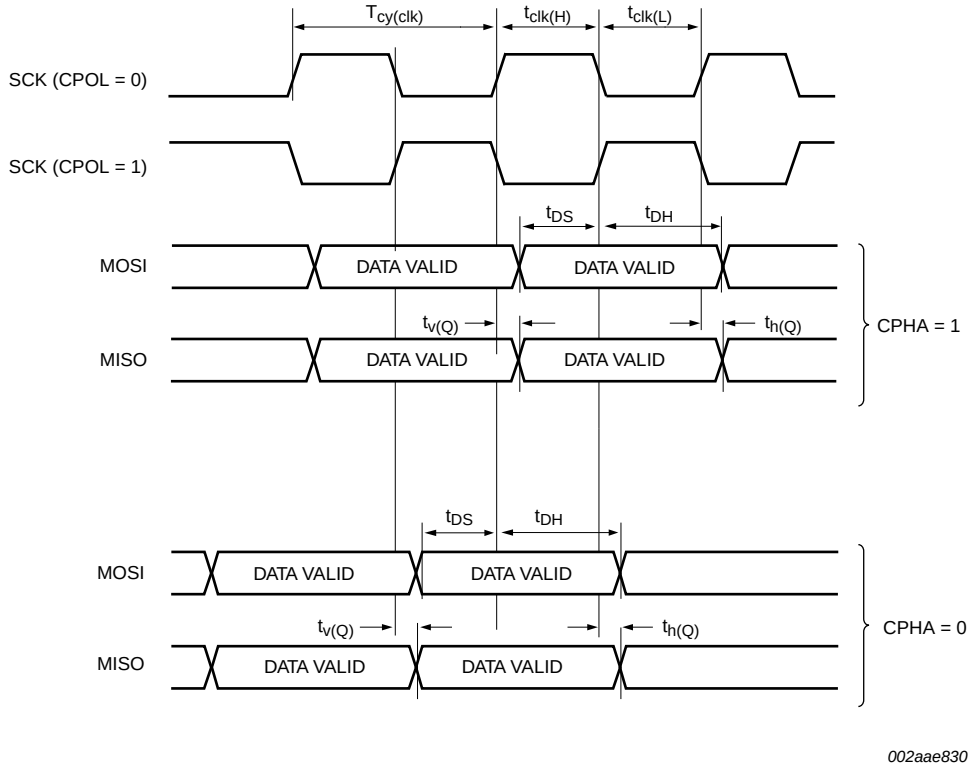



**Fig 26. SPI slave timing in SPI mode**

# 11. Application information

## 11.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 6:

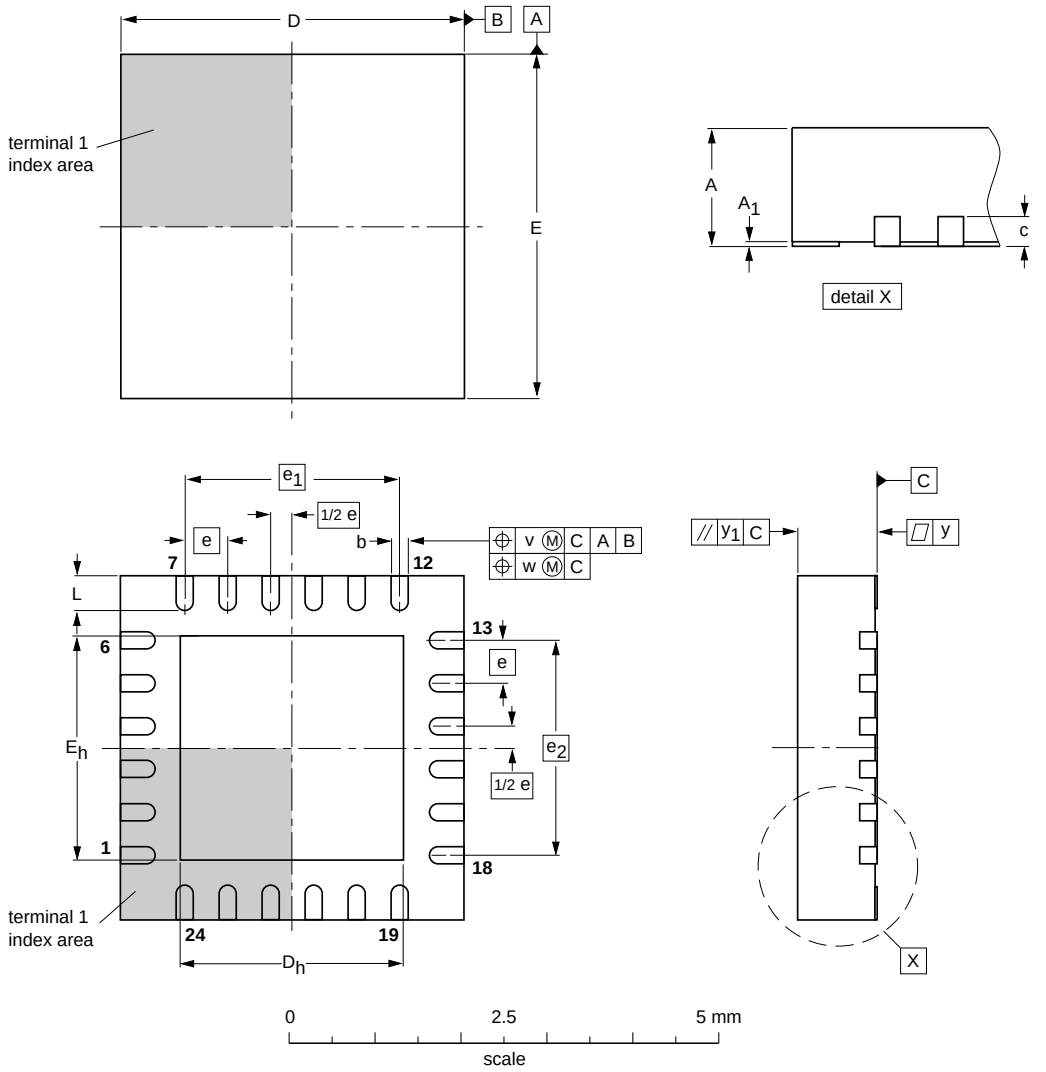
- The ADC input trace must be short and as close as possible to the LPC111xLV/LPC11xxLVUK chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

## 11.2 Standard I/O pad configuration

Figure 27 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input

**HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm** **SOT616-3**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | $A^{(1)}$ max. | $A_1$ | b | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $e_1$ | $e_2$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 4.1<br>3.9 | 2.75<br>2.45 | 4.1<br>3.9 | 2.75<br>2.45 | 0.5 | 2.5 | 2.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT616-3 | - - - | MO-220 | - - - | | | ~~04-11-19~~<br>05-03-10 |

**Fig 30. Package outline (HVQFN24)**