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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	16.5MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	DMA
Number of I/O	56
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.21x24.21)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ia80c152jb-jdplc68ir1

LIST OF FIGURES

  - CSMA/CD
  - SDLC/HDLC
  - User Definable

- Separate Transmit & Receive FIFOs
- Special Protocol Features:
  - Up to 2.0625 Mbps Serial Operation
  - CSMA and SDLC Frame Formats with CRC Checking
  - Manchester, NRZ, & NRZI Data Encoding
  - Collision Detection & Resolution in CSMA Mode

- Selectable Full/Half Duplex

2. Packaging, Pin Descriptions, and Physical Dimensions

Information on the packages and pin descriptions is provided in this chapter.

2.1 Packages and Pinouts

The IA80C152 is available in the following packages:

- 68-Pin PLCC pinout JA/JC versions
- 68-Pin PLCC pinout JB/JD versions

2.1.1 JA/JC

The pinout for the JA/JC package is as shown in Figure 1. The corresponding numeric and alphabetic pin listings are provided in Tables 2 and 3.

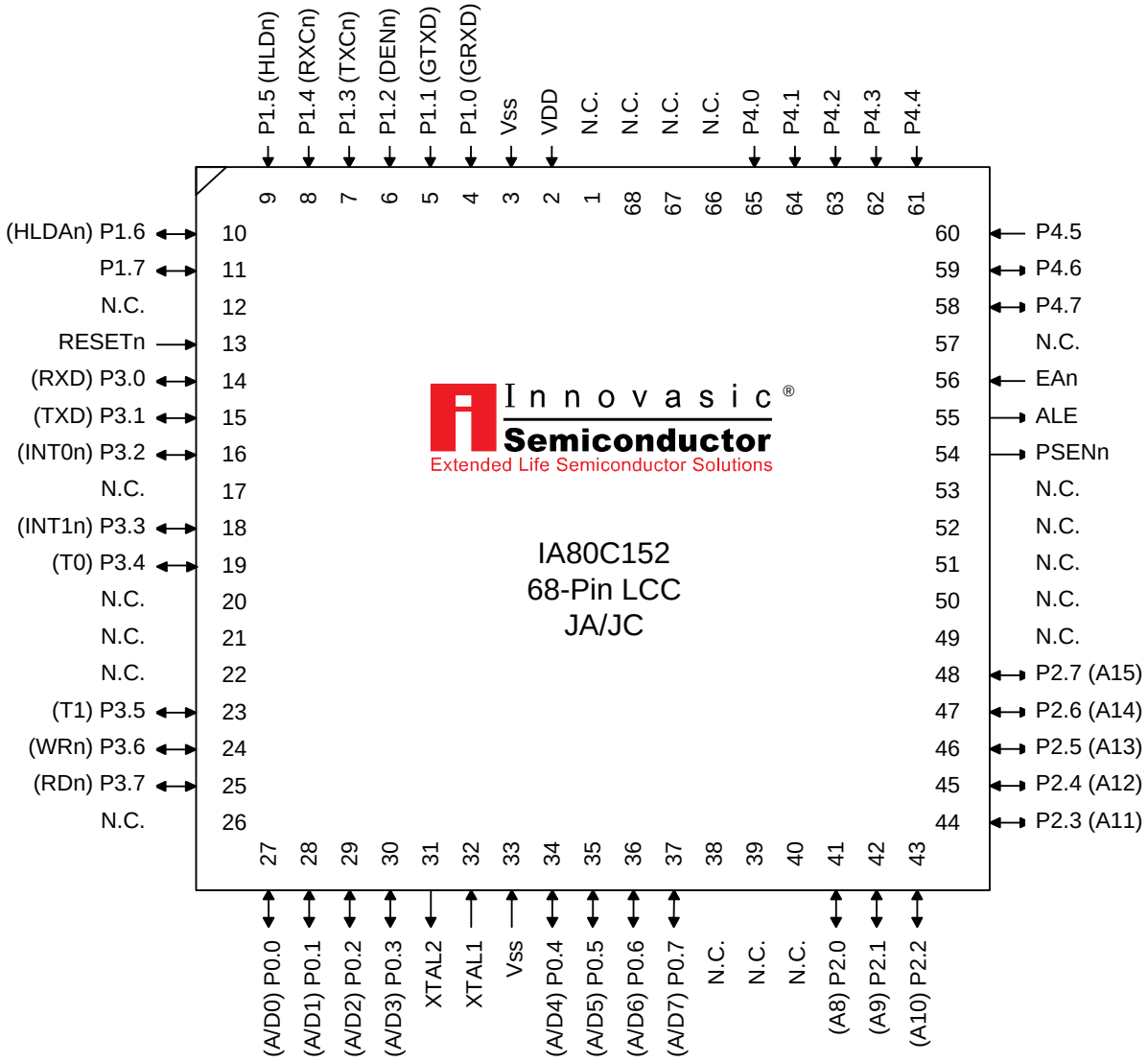
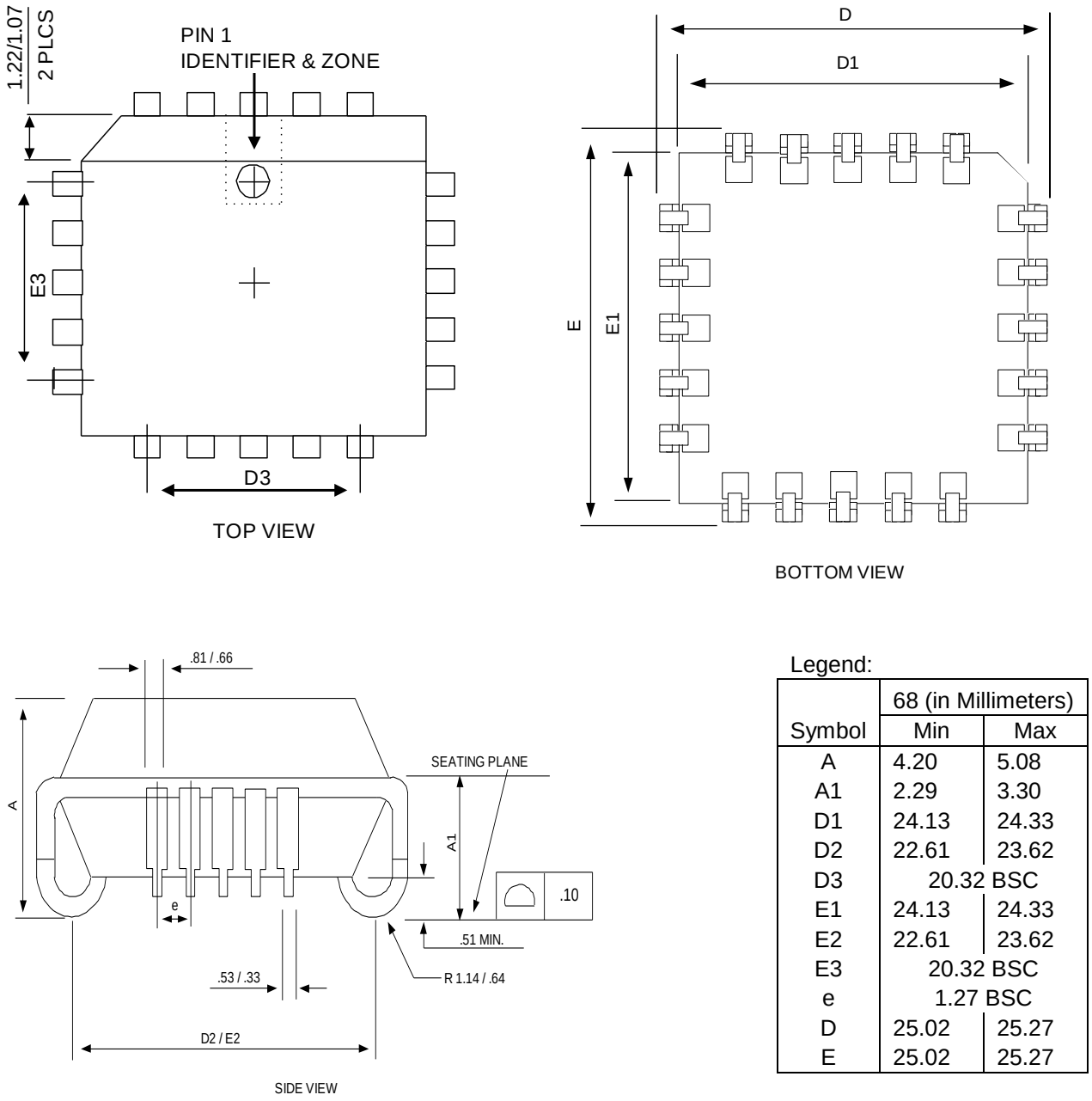


Figure 1. JA/JC Versions Package Diagram

2.1.3 Physical Dimensions

The package dimensions are as shown in Figure 3.



Legend:

Symbol	68 (in Millimeters) Min	Max
A	4.20	5.08
A1	2.29	3.30
D1	24.13	24.33
D2	22.61	23.62
D3	20.32 BSC	
E1	24.13	24.33
E2	22.61	23.62
E3	20.32 BSC	
e	1.27 BSC	
D	25.02	25.27
E	25.02	25.27

Figure 3. Package Dimensions

Table 6. I/O Signal Descriptions *(Continued)*

Signal Name	Description
P1.0 - GRXD, GSC Receive P1.1 - GTXD, GSC Transmit P1.2 - DENn, Driver Enable P1.3 - TXCn, External Transmit Clock P1.4 - RXCn, External Receive Clock P1.5 - HLDn, DMA Hold P1.6 - HLDAn, DMA Hold Acknowledge P1.7	Port 1—8-bit bi-directional port that is bit addressable. To use a port signal as an input, write a 1 to the port location. Internal pull-ups pull the input high and source current when the input is driven low. To use a port signal as an output, a 1 or 0 written to the port location is presented at the output. Port signals in this port also serve as I/O for IA80C152 functions. These I/O signals are defined next to the port name.
P2.0 P2.1 P2.2 P2.3 P2.4 P2.5 P2.6 P2.7	Port 2—8-bit bi-directional port that is bit addressable. To use a port signal as an input, write a 1 to the port location. Internal pull-ups pull the input high and source current when the input is driven low. To use a port signal as an output, a 1 or 0 written to the port location is presented at the output. This port also provides the high-byte of the multiplexed address and data bus depending on the state of EBEN.
P3.0 - RXD, UART Receive P3.1 - TXD, UART Transmit P3.2 - INT0n, External Interrupt 0 P3.3 - INT1n, External Interrupt 1 P3.4 - T0, Timer 0 External Input P3.5 - T1, Timer 1 External Input P3.6 - WRn, External Data Memory Write Strobe P3.7 - RDn, External Data Memory Read Strobe	Port 3—8-bit bi-directional port that is bit addressable. To use a port signal as an input, write a 1 to the port location. Internal pull-ups pull the input high and source current when the input is driven low. To use a port signal as an output, a 1 or 0 written to the port location is presented at the output. Port signals in this port also serve as I/O for IA80C152 functions. These I/O signals are defined next to the port name.

Table 9. DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{CC}	Supply Voltage	4.5	–	5.5	V	–
V_{IL}	Input Low Voltage (All Except XTAL1)	–	–	0.9	V	–
V_{IH}	Input High Voltage (All Except XTAL1)	2.1	–	–	V	–
V_{OL}	Output Low Voltage	–	–	0.4	V	–
V_{OH}	Output High Voltage (All Except Port 0 in port mode)	3.5	–	–	V	–
		–	–	–		–
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	3.5	–	–	V	–
		–	–	–	–	–
I_{IL}	Logical 0 Input Current	-1	–	1	µA	No pullup or pulldown
I_{IH}	Logical 1 Input Current	-1	–	1	µA	No pullup or pulldown
I_{oz}	Input Leakage (Port 0,1,2,3,4,5,6, ALE,PSEN, EPSEN)	-10	–	10	µA	Tri-state leakage current
Rup, Rdn	Pull-up Resistor, Pull-down Resistor	–	50	–	kW	–
I_{DD}[a]	Power Supply Current: Active (16.5 MHz) Idle (16.5 MHz) Power Down Mode	–	–	50	mA	–
			–	–	mA	–
			–	–	µA	–

[a]Static Idd current is exclusive of input/output drive requirements and is measured with the clocks stopped and all inputs tied to Vdd or Vss configured to draw minimum current.

4. Device Architecture

4.1 Functional Block Diagram

Figure 4 shows the major functional blocks of the IA80C152. Each version of the IA80C152 function identically to each other with the exception of the 2 additional I/O ports (Port 5 and Port 6) in the JB and JD versions.

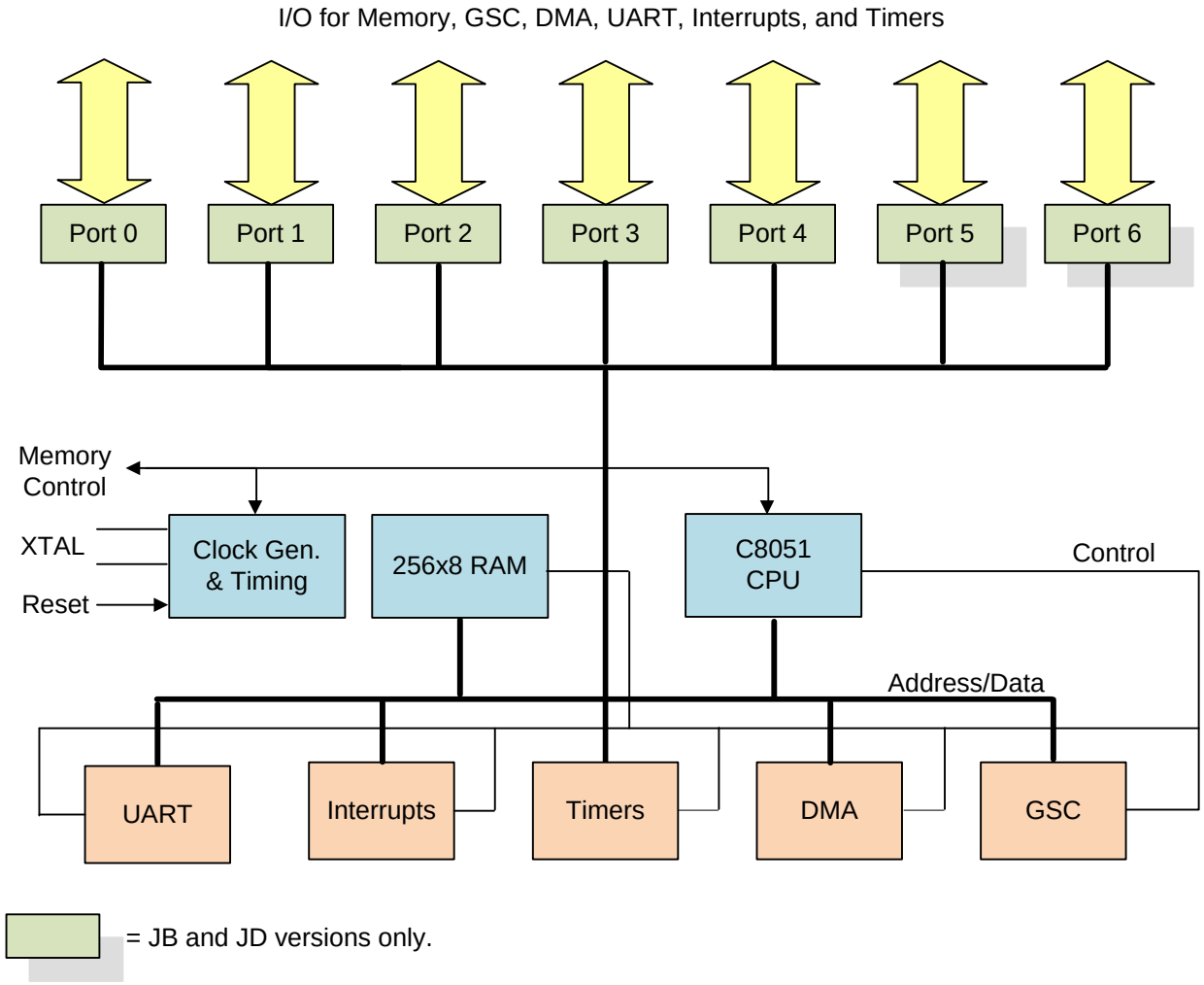


Figure 4. Functional Block Diagram

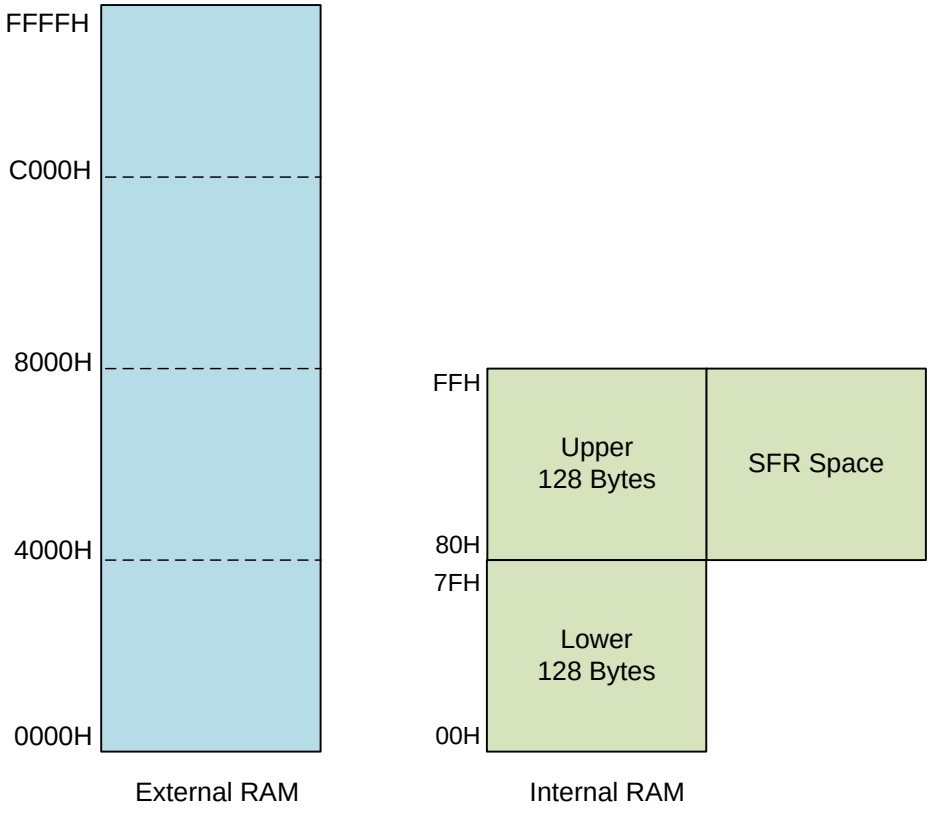


Figure 5. Memory Space

In the Raw Transmit mode the receiver operates as normal and zero bit detection is performed in SDLC mode. The transmit output is internally connected to the receiver input for loopback testing. Data transmitted is done so without a preamble, flag or zero bit insertion and without a CRC.

In the Alternate Backoff mode the backoff is modified so it is delayed until the end of the IFS. Since the IFS time is generally longer than the slot time this should help to prevent collisions.

- Bit [4]—AL → This bit determines the address length used. If set to a 1, the 16-bit addressing is used. If set to a 0, the 8 bit addressing is used.
- Bit [3]—CT → This bit determines the CRC type used. If set to a 1, the 32-bit AUTODIN II-32 is used. If set to a 0, the 16 bit CRC-CCITT is used.
- Bits [2–1]—PL0, PL1 → Preamble length:

PL1	PL0	Preamble length in bits
0	0	0
0	1	8
1	0	32
1	1	64

The length noted in the table includes the two-bit BOF in CSMA/CD mode but not the SDLC flag. Zero length preamble is not compatible with CSMA/CD mode.

- Bit [0]—PR → If set to a 1, the GSC is in SDLC mode. If set to a 0, the GSC is in CSMA/CD mode.

5.2.14 IE* (0A8h)

The Interrupt Enable register allows the software to select which interrupts are enabled as shown in Table 15. If a bit is 0, the interrupt is disabled. If a bit is 1, the interrupt is enabled.

Table 15. IE* Register

7	6	5	4	3	2	1	0
EA	Reserved	Reserved	ES	ET1	EX1	ET0	EX0

- Bit [7]—EA → Enable All interrupts. This bit globally enables or disables all interrupts regardless of the state of the individual bits.
- Bit [6]—Reserved.
- Bit [5]—Reserved.

- Bit [4]—ES → Enable or disable serial port interrupt.
- Bit [3]—ET1 → Enable or disable Timer 1 overflow interrupt.
- Bit [2]—EX1 → Enable or disable External Interrupt 1.
- Bit [1]—ET0 → Enable or disable Timer 0 overflow interrupt.
- Bit [0]—EX0 → Enable or disable External Interrupt 0.

5.2.15 IEN1* (0C8h)

The Interrupt Enable Number 1 register allows the software to select which interrupts are enabled as shown in Table 16. If a bit is 0, the interrupt is disabled. If a bit is 1, the interrupt is enabled.

Table 16. IEN1* Register

7	6	5	4	3	2	1	0
Reserved	Reserved	EGSTE	EDMA1	EGSTV	EDMA0	EGSRE	EGSRV

- Bit [7]—Reserved.
- Bit [6]—Reserved.
- Bit [5]—EGSTE → Enable or disable GSC Transmit Error interrupt.
- Bit [4]—EDMA1 → Enable or disable DMA channel 1 interrupt.
- Bit [3]—EGSTV → Enable or disable GSC Transmit Valid interrupt.
- Bit [2]—EDMA0 → Enable or disable DMA channel 0 interrupt.
- Bit [1]—EGSRE → Enable or disable GSC Receive Error interrupt.
- Bit [0]—EGSRV → Enable or disable GSC Receive Valid interrupt.

5.2.16 IFS (0A4h)

The Interframe Spacing register determines the number of bit times between transmitted frames in both CSMA/CD and SDLC. Only even bit times can be used. The number written to this register is divided by two and loaded into the seven most significant bits. An interframe space is created by counting down this seven bit number twice. The value read from this register is the current count value in the upper seven bits and the first or second count down in the LSB. A 1 indicates the first count down and a 0 indicates the second count down. The value may not be valid because the register is clocked asynchronously to the CPU.

Table 20. P0*, P1*, P2*, P3*, P4*, P5, P6 Register

Port		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0	Function	Multiplexed Address/Data							
	Bit Address	087h	086h	085h	084h	083h	082h	081h	080h
P1	Function	–	HLDAn	HLDn	RXCn	TXCn	DENn	GTXD	GRXD
	Bit Address	097h	096h	095h	094h	093h	092h	091h	090h
P2	Function	Address and User Defined							
	Bit Address	0A7h	0A6h	0A5h	0A4h	0A3h	0A2h	0A1h	0A0h
P3	Function	RDn	WRn	T1	T0	INT1n	INT0n	TXD	RXD
	Bit Address	0B7h	0B6h	0B5h	0B4h	0B3h	0B2h	0B1h	0B0h
P4	Function	User Defined							
	Bit Address	0C7h	0C6h	0C5h	0C4h	0C3h	0C2h	0C1h	0C0h
P5	Function	User Defined							
	Bit Address	091h							
P6	Function	User Defined							
	Address	0A1h							

5.2.21 PCON (087h)

The Power Control register controls the power down and idle states of the IA80C152 as well as various UART, GSC, and DMA functions as defined in Table 21.

Table 21. PCON Register

7	6	5	4	3	2	1	0
SMOD	ARB	REQ	GAREN	XRCLK	GFIEN	PD	IDL

- Bit [7]—SMOD → Doubles the baud rate of the UART if the bit is set to 1.
- Bit [6]—ARB → The DMA (both channels) is put into Arbiter mode if the bit is set to 1.
- Bit [5]—REQ → The DMA (both channels) is put into Requester mode if the bit is set to 1.
- Bit [4]—GAREN → The GSC Auxiliary Receive Enable allows the GSC to receive back-to-back SDLC frames by setting the bit to 1. This bit has no effect in CSMA mode.
- Bit [3]—XRCLK → Setting this bit enables the External Receive Clock to be used by the receiver portion of the GSC.
- Bit [2]—GFIEN → The GSC Flag Idle Enable bit generates idle flags between transmitted SDLC frames when this bit is set to a 1. This bit has no effect in CSMA mode.

Table 25. TCON* Register

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

- Bit [7]—TF1 → Timer overFlow 1 interrupt flag set by hardware when timer 1 overflows. Hardware clears this flag when the processor vectors to the interrupt service routine.
- Bit [6]—TR1 → Timer Run 1 flag set by software to turn on timer 1 and cleared by software to turn off timer 1.
- Bit [5]—TF0 → Timer overFlow 0 interrupt flag set by hardware when timer 0 overflows. Hardware clears this flag when the processor vectors to the interrupt service routine.
- Bit [4]—TR0 → Timer Run 0 flag set by software to turn on timer 0 and cleared by software to turn off timer 0.
- Bit [3]—IE1 → Interrupt External 1 flag set by hardware when an edge is detected on External Interrupt 1. Hardware clears this flag when the processor vectors to the interrupt service routine.
- Bit [2]—IT1 → Interrupt Type 1 flag is set by software to specify a falling edge triggered interrupt for External Interrupt 1. The flag is cleared by software to specify a low level triggered interrupt for External Interrupt 1.
- Bit [1]—IE0 → Interrupt External 0 flag set by hardware when an edge is detected on External Interrupt 0. Hardware clears this flag when the processor vectors to the interrupt service routine.
- Bit [0]—IT0 → Interrupt Type 0 flag is set by software to specify a falling edge triggered interrupt for External Interrupt 0. The flag is cleared by software to specify a low level triggered interrupt for External Interrupt 0.

5.2.34 TFIFO (085h)

This is the 3 byte buffer used for storing GSC transmit data. If TEN is set to a 1 transmission begins as soon as data is written to TFIFO.

5.2.35 TH0, TL0 (08Ch, 08Ah)

These registers provide the high byte (TH0) and low byte (TL0) values for Timer 0. These registers may be used together or separately depending on Timer 0 mode bits.

Power Down Mode is entered through software control of the PCON register. Power Down disables the oscillator causing all functions to stop. RAM data is maintained because power is not removed from the device. The only way to exit power down mode is to invoke a hardware reset.

Table 28. Power Conservation Modes

Mode	Program Fetch	ALE	PSENn	EPSENn[a]	Port 0	Port 1	Port 2	Port 3	Port 4	Port 5[a]	Port 6[a]
Idle	P0, P2	1	1	1	Float	Data	Addr.	Data	Data	Data	Data
	P5, P6[a]	1	1	1	Data	Data	Data	Data	Data	0FFh	Addr.
Power Down	P0, P2	0	0	1	Float	Data	Data	Data	Data	Data	Data
	P5, P6[a]	0	1	0	Data	Data	Data	Data	Data	0FFh	0FFh

[a]JB and JD versions only.

5.4 Oscillator Pins

There are 2 methods for providing a clock to the IA80C152. One method is to provide a crystal oscillator and the other method is to provide an external clock source. When providing a crystal oscillator, the XTAL1 pin is the input and XTAL2 is the output. The min and max crystal frequencies are 3.5 and 16.5 MHz, respectively.

When providing an external clock source, XTAL1 is the input and XTAL2 has no connection. Duty cycle does not matter to the device, however, the external clock source requires a minimum pulse width of 20 ns.

Figures 6 through 13 present the external program memory read cycle, the external data memory read cycle, the external data memory write cycle, the external clock drive waveform, the shift register mode timing waveforms, the GSC receiver timings (internal baud rate generator), the GSC transmit timings (internal baud rate generator), the GSC timings (external clock) respectively. Tables 29 through 32 present the external clock drive, the local serial channel timing—shift register mode, the global serial port timing—internal baud rate generator, and the global serial port timing—external clock, respectively.

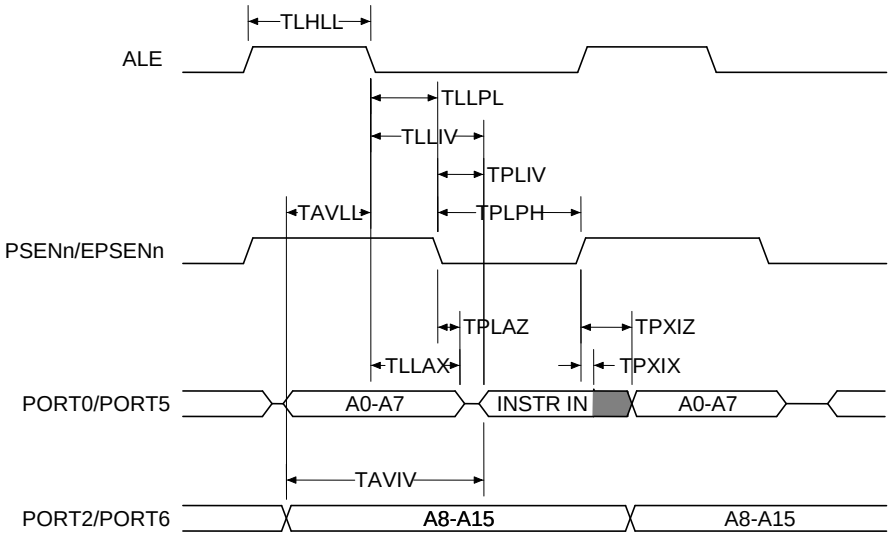


Figure 6. External Program Memory Read Cycle

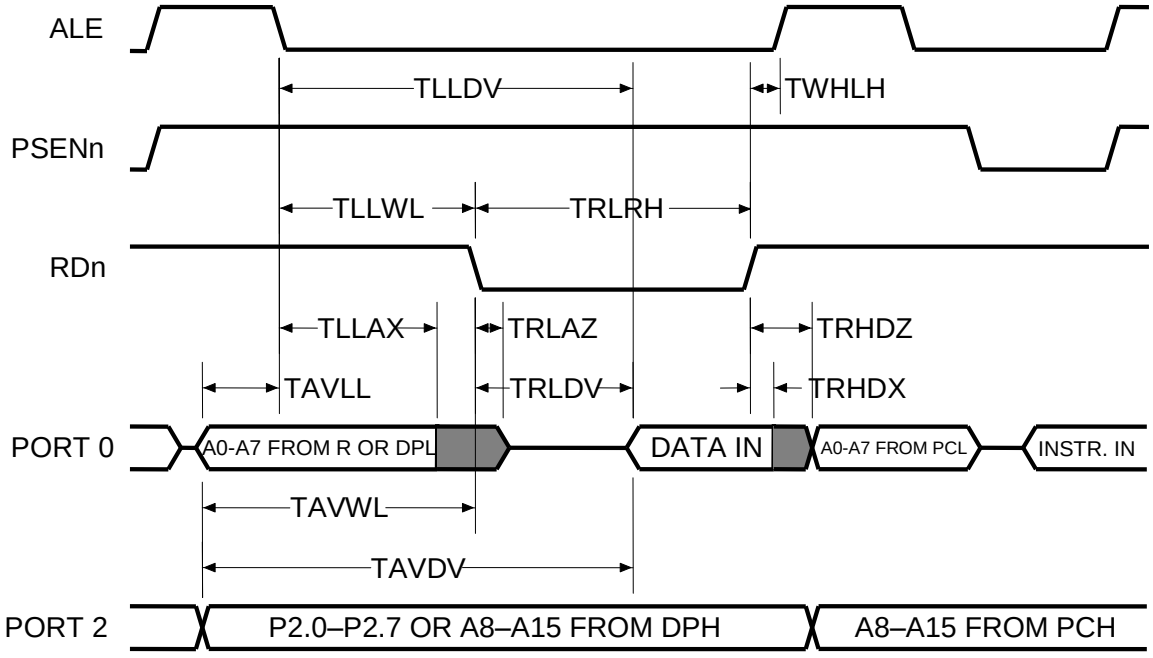


Figure 7. External Data Memory Read Cycle

6. Instruction Set Summary Table

Table 33 provides a summary of the instruction set organized by hexadecimal opcode. Please refer to the original Intel Data Book for individual instruction set details.

Table 33. Instruction Set Summary

Opcode	Mnemonic
00 H	NOP
01 H	AJMP addr11
02 H	LJMP addr16
03 H	RR A
04 H	INC A
05 H	INC direct
06 H	INC @R0
07 H	INC @R1
08 H	INC R0
09 H	INC R1
0A H	INC R2
0B H	INC R3
0C H	INC R4
0D H	INC R5
0E H	INC R6
0F H	INC R7
10 H	JBC bit,rel
11 H	ACALL addr11
12 H	LCALL addr16
13 H	RRC A
14 H	DEC A
15 H	DEC direct
16 H	DEC @R0
17 H	DEC @R1
18 H	DEC R0
19 H	DEC R1
1A H	DEC R2
1B H	DEC R3
1C H	DEC R4
1D H	DEC R5
1E H	DEC R6
1F H	DEC R7
20 H	JB bit.rel
21 H	AJMP addr11
22 H	RET
23 H	RL A
24 H	ADD A,#data
25 H	ADD A,direct
26 H	ADD A,@R0
27 H	ADD A,@R1
28 H	ADD A,R0

Table 33. Instruction Set Summary *(Continued)*

Opcode	Mnemonic
29 H	ADD A,R1
2A H	ADD A,R2
2B H	ADD A,R3
2C H	ADD A,R4
2D H	ADD A,R5
2E H	ADD A,R6
2F H	ADD A,R7
30 H	JNB bit.rel
31 H	ACALL addr11
32 H	RETI
33 H	RLC A
34 H	ADDC A,#data
35 H	ADDC A,direct
36 H	ADDC A,@R0
37 H	ADDC A,@R1
38 H	ADDC A,R0
39 H	ADDC A,R1
3A H	ADDC A,R2
3B H	ADDC A,R3
3C H	ADDC A,R4
3D H	ADDC A,R5
3E H	ADDC A,R6
3F H	ADDC A,R7
40 H	JC rel
41 H	AJMP addr11
42 H	ORL direct,A
43 H	ORL direct,#data
44 H	ORL A,#data
45 H	ORL A,direct
46 H	ORL A,@R0
47 H	ORL A,@R1
48 H	ORL A,R0
49 H	ORL A,R1
4A H	ORL A,R2
4B H	ORL A,R3
4C H	ORL A,R4
4D H	ORL A,R5
4E H	ORL A,R6
4F H	ORL A,R7
50 H	JNC rel
51 H	ACALL addr11
52 H	ANL direct,A
53 H	ANL direct,#data
54 H	ANL A,#data
55 H	ANL A,direct
56 H	ANL A,@R0

Table 33. Instruction Set Summary *(Continued)*

Opcode	Mnemonic
B3 H	CPL C
B4 H	CJNE A,#data,rel
B5 H	CJNE A,direct,rel
B6 H	CJNE @R0,#data,rel
B7 H	CJNE @R1,#data,rel
B8 H	CJNE R0,#data,rel
B9 H	CJNE R1,#data,rel
BA H	CJNE R2,#data,rel
BB H	CJNE R3,#data,rel
BC H	CJNE R4,#data,rel
BD H	CJNE R5,#data,rel
BE H	CJNE R6,#data,rel
BF H	CJNE R7,#data,rel
C0 H	PUSH direct
C1 H	AJMP addr11
C2 H	CLR bit
C3 H	CLR C
C4 H	SWAP A
C5 H	XCH A,direct
C6 H	XCH A,@R0
C7 H	XCH A,@R1
C8 H	XCH A,R0
C9 H	XCH A,R1
CA H	XCH A,R2
CB H	XCH A,R3
CC H	XCH A,R4
CD H	XCH A,R5
CE H	XCH A,R6
CF H	XCH A,R7
D0 H	POP direct
D1 H	ACALL addr11
D2 H	SETB bit
D3 H	SETB C
D4 H	DA A
D5 H	DJNZ direct,rel
D6 H	XCHD A,@R0
D7 H	XCHD A,@R1
D8 H	DJNZ R0,rel
D9 H	DJNZ R1,rel
DA H	DJNZ R2,rel
DB H	DJNZ R3,rel
DC H	DJNZ R4,rel
DD H	DJNZ R5,rel
DE H	DJNZ R6,rel

Table 33. Instruction Set Summary *(Continued)*

Opcode	Mnemonic
DF H	DJNZ R7,rel
E0 H	MOVX A,@DPTR
E1 H	AJMP addr11
E2 H	MOVX A,@R0
E3 H	MOVX A,@R1
E4 H	CLR A
E5 H	MOV A,direct
E6 H	MOV A,@R0
E7 H	MOV A,@R1
E8 H	MOV A,R0
E9 H	MOV A,R1
EA H	MOV A,R2
EB H	MOV A,R3
EC H	MOV A,R4
ED H	MOV A,R5
EE H	MOV A,R6
EF H	MOV A,R7
F0 H	MOVX @DPTR,A
F1 H	ACALL addr11
F2 H	MOVX @R0,A
F3 H	MOVX @R1,A
F4 H	CPL A
F5 H	MOV direct,A
F6 H	MOV @R0,A
F7 H	MOV @R1,A
F8 H	MOV R0,A
F9 H	MOV R1,A
FA H	MOV R2,A
FB H	MOV R3,A
FC H	MOV R4,A
FD H	MOV R5,A
FE H	MOV R6,A
FF H	MOV R7,A

9. Errata

The following errata are associated with all versions of the IA80C152. A workaround to the identified problem has been provided where possible.

9.1 Errata Summary

Table 36 presents a summary of errata.

Table 36. Summary of Errata

Errata No.	Problem	Rev. 01
1	Under certain circumstances, the DMA arbiter will "lock up" in alternate cycles mode. This problem occurs when one DMA channel has finished performing a transfer and another DMA initiates a transfer with the byte Count Register having been set to 0001 by the CPU.	Exists
2	Original Intel device has a linear resistor as the pullup on input RESET.	Exists
3	DMA can interfere with processing of interrupts of different priority.	Exists
4	Corruption of read data may occur if Port 0 bit written to 0.	Exists

9.2 Errata Detail

Errata No. 1

Problem: Under certain circumstances, the DMA arbiter will "lock up" in alternate cycles mode. This problem occurs when one DMA channel has finished performing a transfer and another DMA initiates a transfer with the byte Count Register having been set to 0001 by the CPU.

Workaround: Avoid using the alternate cycles DMA mode in conjunction with a byte count of one.

Errata No. 2

Problem: Original Intel device has a linear resistor as the pullup on input RESET.

Workaround: None. A non-linear resistor is on the Innovasic device. This may affect operation of certain R/C reset circuits.

Revision History

Table 37 presents the sequence of revisions to document IA211040524.

Table 37. Revision History

Date	Revision	Description	Page(s)
August 17, 2005	1	Edition released.	NA
July 27, 2007	2	Renamed data sheet for clarity	NA
August 31, 2007	3	Updated Errata and RoHS information	57, 58
June 18, 2009	4	Document reformatted to meet publication standards. Added Conventions, Acronyms and Abbreviations, and Summary of Errata table. Added new errata and added range for supply voltage in Table 9.	All
August 17, 2009	5	Added a note regarding recommendations for using the JB/JD version of the device in JA/JC applications. Revised Tables 2, 3 and 5.	7, 11, 12, 15
July 29, 2010	6	Errata 3 and 4 added.	58, 59