Microsemi Corporation - 5962-9215602MXA Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	140
Number of Gates	8000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Through Hole
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	176-BCPGA
Supplier Device Package	176-CPGA (39.88x39.88)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/5962-9215602mxa

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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ACT 2 Family Overview

Detailed Specifications

Package Pin Assignments

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2 – Detailed Specifications

Operating Conditions

Table 2-1 • **Absolute Maximum Ratings**[1]

Symbol	Parameter	Limits	Units
VCC	DC supply voltage	–0.5 to +7.0	V
VI	Input voltage	–0.5 to VCC + 0.5	V
VO	Output voltage	–0.5 to VCC + 0.5	V
IIO	I/O source sink current[2]	±20	mA
T_{STG}	Storage temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND –0.5 V, the internal protection diodes will be forward biased and can draw excessive current.*

Table 2-2 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature range*	0 to +70	–40 to +85	–55 to +125	°C
Power supply tolerance	±5	±10	±10	%VCC

*Note: *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Static Power Component

Microsemi FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated in Table 2-5 for commercial, worst case conditions.

Table 2-5 • **Standby Power Calculation**

ICC	VCC	Power
2 mA	5.25 V	10.5 mW

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs.

An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by EQ 3.

$$\text{Power } (\mu W) = C_{EQ} * VCC^2 * F$$

EQ 3

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

VCC is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring ICC active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown in Table 2-6.

Table 2-6 • **CEQ Values for Microsemi FPGAs**

Item	CEQ Value
Modules (C_{EQM})	5.8
Input Buffers (C_{EQI})	12.9
Output Buffers (C_{EQO})	23.8
Routed Array Clock Buffer Loads (C_{EQCR})	3.9

Parameter Measurement

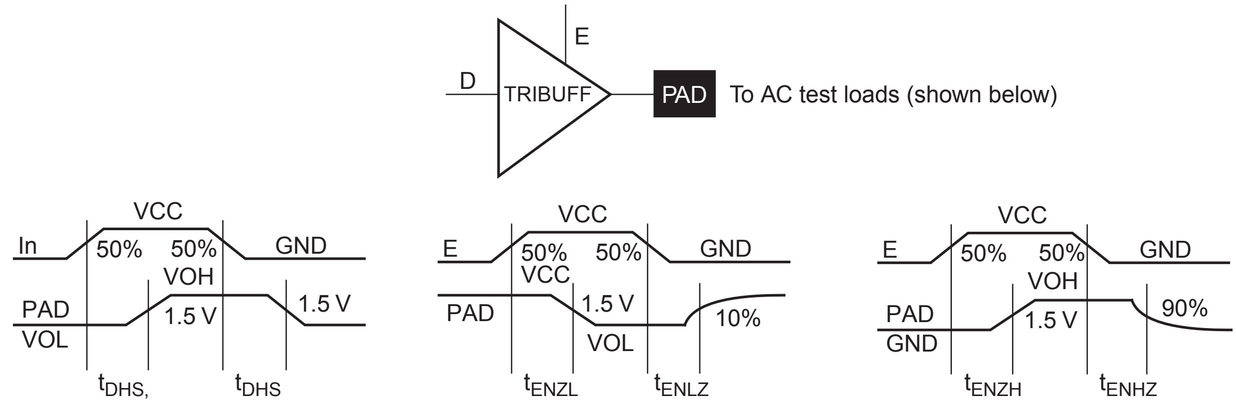


Figure 2-2 • **Output Buffer Delays**

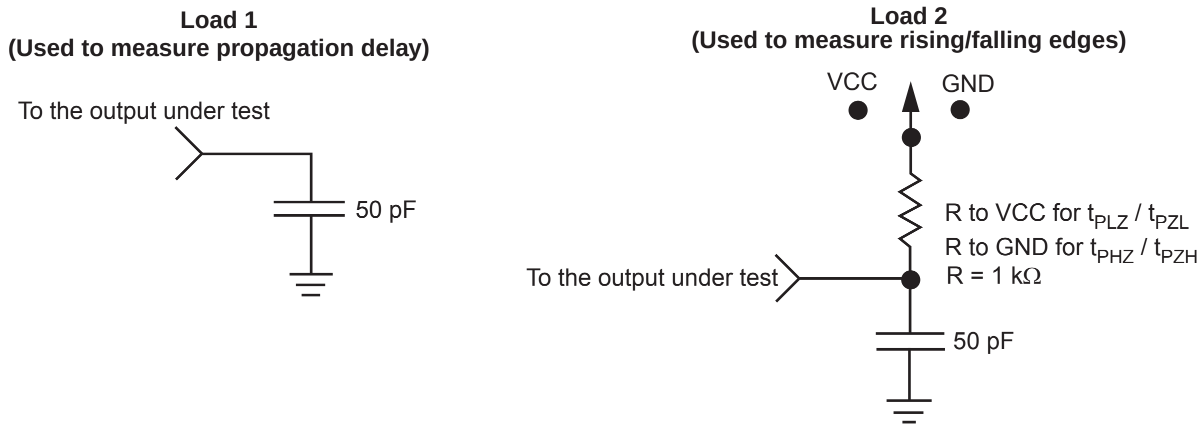


Figure 2-3 • **AC Test Loads**

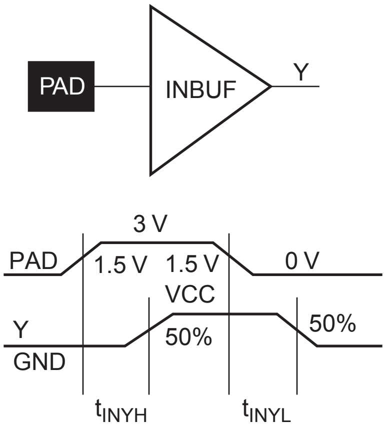


Figure 2-4 • **Input Buffer Delays**

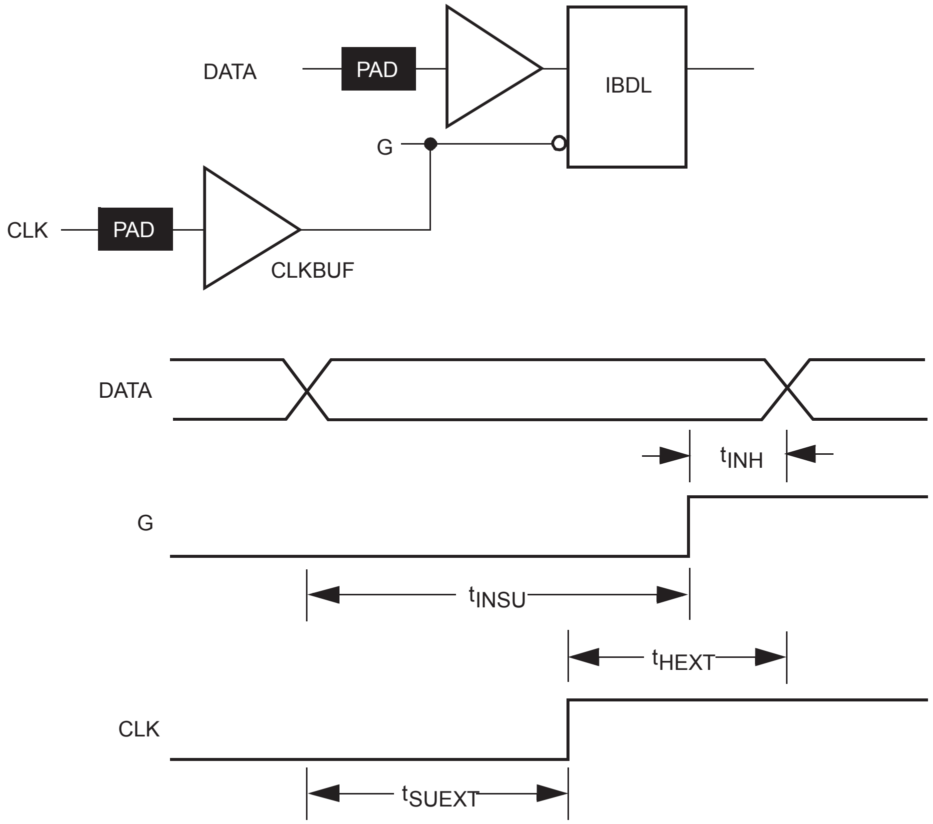


Figure 2-7 • **Input Buffer Latches**

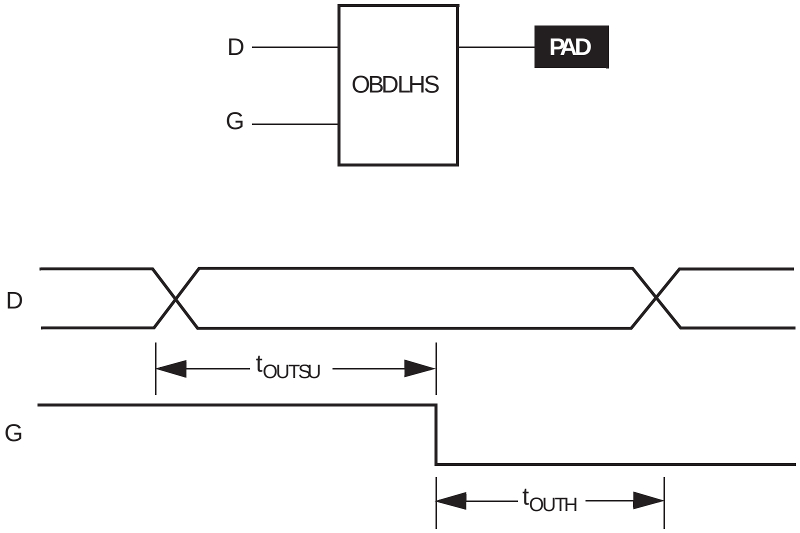


Figure 2-8 • **Output Buffer Latches**

Timing Derating Factor (Temperature and Voltage)

Table 2-9 • **Timing Derating Factor (Temperature and Voltage)**

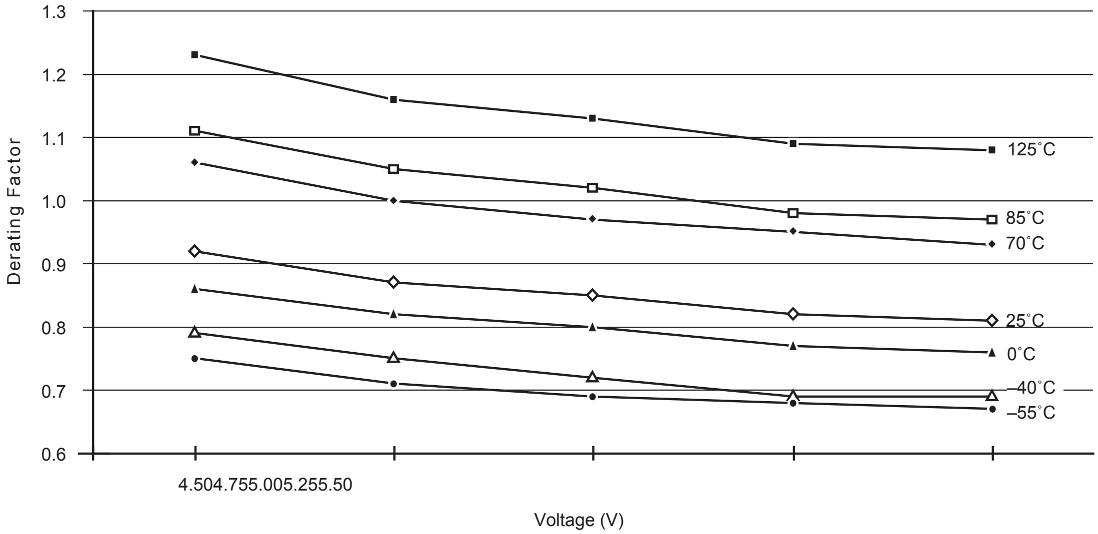
(Commercial Minimum/Maximum Specification) x	**Industrial**		**Military**	
	Min.	**Max.**	**Min.**	Max.
	0.69	1.11	0.67	1.23

Table 2-10 • **Timing Derating Factor for Designs at Typical Temperature (T_J = 25°C) and Voltage (5.0 V)**

(Commercial Maximum Specification) x	0.85

Table 2-11 • **Temperature and Voltage Derating Factors (normalized to Worst-Case Commercial, TJ = 4.75 V, 70°C)**

	–55	**–40**	**0**	**25**	**70**	**85**	**125**
4.50	0.75	0.79	0.86	0.92	1.06	1.11	1.23
4.75	0.71	0.75	0.82	0.87	1.00	1.05	1.13
5.00	0.69	0.72	0.80	0.85	0.97	1.02	1.13
5.25	0.68	0.69	0.77	0.82	0.95	0.98	1.09
5.50	0.67	0.69	0.76	0.81	0.93	0.97	1.08



Note: This derating factor applies to all routing and propagation delays.

Figure 2-9 • **Junction Temperature and Voltage Derating Curves (normalized to Worst-Case Commercial, T_J = 4.75 V, 70°C)**

A1240A Timing Characteristics (continued)

***Table 2-16* • A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

I/O Module Input Propagation Delays			**–2 Speed**		**–1 Speed**		**Std. Speed**		**Units**
Parameter/Description			**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{INYH}	Pad to Y High			2.9		3.3		3.8	ns
t_{INYL}	Pad to Y Low			2.6		3.0		3.5	ns
t_{INGH}	G to Y High			5.0		5.7		6.6	ns
t_{INGL}	G to Y Low			4.7		5.4		6.3	ns
Input Module Predicted Input Routing Delays*									
t_{IRD1}	FO = 1 Routing Delay			4.2		4.8		5.6	ns
t_{IRD2}	FO = 2 Routing Delay			4.8		5.4		6.4	ns
t_{IRD3}	FO = 3 Routing Delay			5.4		6.1		7.2	ns
t_{IRD4}	FO = 4 Routing Delay			5.9		6.7		7.9	ns
t_{IRD8}	FO = 8 Routing Delay			7.9		8.9		10.5	ns
Global Clock Network									
t_{CKH}	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		11.8		13.0		15.7	
t_{CKL}	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		12.0		13.2		15.9	
t_{PWH}	Minimum Pulse Width High	FO = 32	3.8		4.5		5.5		ns
		FO = 256	4.1		5.0		5.8		
t_{PWL}	Minimum Pulse Width Low	FO = 32	3.8		4.5		5.5		ns
		FO = 256	4.1		5.0		5.8		
t_{CKSW}	Maximum Skew	FO = 32		0.5		0.5		0.5	ns
		FO = 256		2.5		2.5		2.5	
t_{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t_{HEXT}	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t_P	Minimum Period	FO = 32	8.1		9.1		11.1		ns
		FO = 256	8.8		10.0		11.7		
f_{MAX}	Maximum Frequency	FO = 32		125.0		110.0		90.0	ns
		FO = 256		115.0		100.0		85.0	

Note: **These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1280A Timing Characteristics (continued)

***Table 2-19* • A1280A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

I/O Module Input Propagation Delays			**–2 Speed**		**–1 Speed**		**Std. Speed**		**Units**
Parameter/Description			**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{INYH}	Pad to Y High			2.9		3.3		3.8	ns
t_{INYL}	Pad to Y Low			2.7		3.0		3.5	ns
t_{INGH}	G to Y High			5.0		5.7		6.6	ns
t_{INGL}	G to Y Low			4.8		5.4		6.3	ns
Input Module Predicted Input Routing Delays*									
t_{IRD1}	FO = 1 Routing Delay			4.6		5.1		6.0	ns
t_{IRD2}	FO = 2 Routing Delay			5.2		5.9		6.9	ns
t_{IRD3}	FO = 3 Routing Delay			5.6		6.3		7.4	ns
t_{IRD4}	FO = 4 Routing Delay			6.5		7.3		8.6	ns
t_{IRD8}	FO = 8 Routing Delay			9.4		10.5		12.4	ns
Global Clock Network									
t_{CKH}	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		13.1		14.6		17.2	
t_{CKL}	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		13.3		14.9		17.5	
t_{PWH}	Minimum Pulse Width High	FO = 32	5.0		5.5		6.6		ns
		FO = 256	5.8		6.4		7.6		
t_{PWL}	Minimum Pulse Width Low	FO = 32	5.0		5.5		6.6		ns
		FO = 256	5.8		6.4		7.6		
t_{CKSW}	Maximum Skew	FO = 32		0.5		0.5		0.5	ns
		FO = 256		2.5		2.5		2.5	
t_{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t_{HEXT}	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t_P	Minimum Period	FO = 32	9.6		11.2		13.3		ns
		FO = 256	10.6		12.6		15.3		
f_{MAX}	Maximum Frequency	FO = 32		105.0		90.0		75.0	ns
		FO = 256		95.0		80.0		65.0	

Note: **These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1280A Timing Characteristics (continued)

Table 2-20 • A1280A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

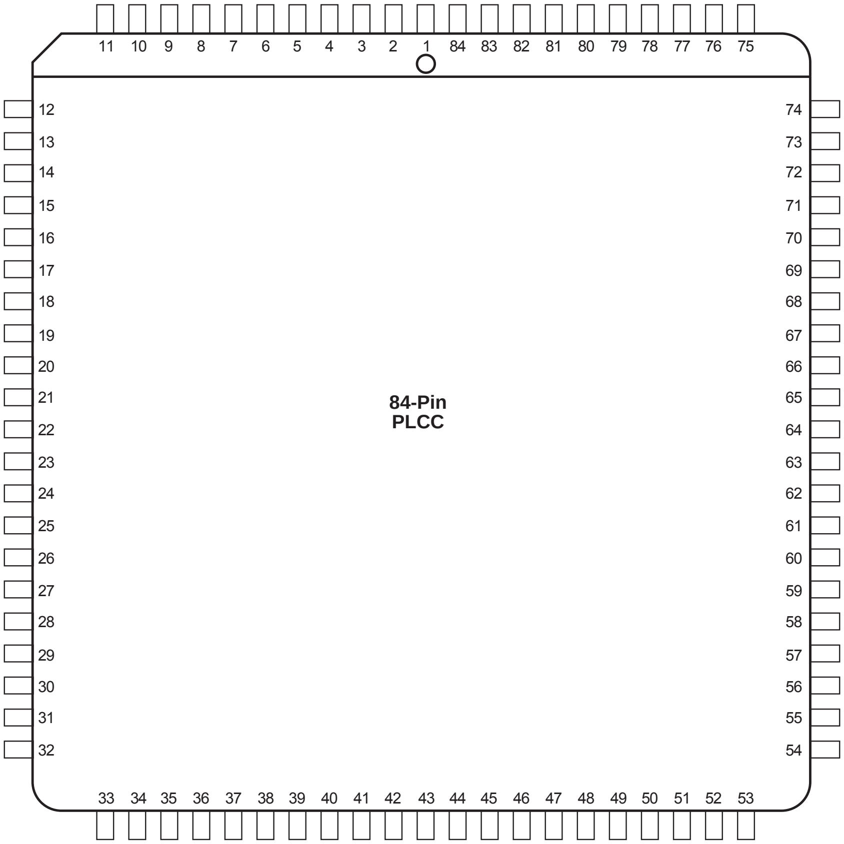
TTL Output Module Timing[1]		–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{DLH}	Data to Pad High		8.1		9.0		10.6	ns
t_{DHL}	Data to Pad Low		10.2		11.4		13.4	ns
t_{ENZH}	Enable Pad Z to High		9.0		10.0		11.8	ns
t_{ENZL}	Enable Pad Z to Low		11.8		13.2		15.5	ns
t_{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t_{ENLZ}	Enable Pad Low to Z		8.4		9.5		11.1	ns
t_{GLH}	G to Pad High		9.0		10.2		11.9	ns
t_{GHL}	G to Pad Low		11.3		12.7		14.9	ns
d_{TLH}	Delta Low to High		0.07		0.08		0.09	ns/pF
d_{THL}	Delta High to Low		0.12		0.13		0.16	ns/pF
CMOS Output Module Timing[1]								
t_{DLH}	Data to Pad High		10.3		11.5		13.5	ns
t_{DHL}	Data to Pad Low		8.5		9.6		11.2	ns
t_{ENZH}	Enable Pad Z to High		9.0		10.0		11.8	ns
t_{ENZL}	Enable Pad Z to Low		11.8		13.2		15.5	ns
t_{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t_{ENLZ}	Enable Pad Low to Z		8.4		9.5		11.1	ns
t_{GLH}	G to Pad High		9.0		10.2		11.9	ns
t_{GHL}	G to Pad Low		11.3		12.7		14.9	ns
d_{TLH}	Delta Low to High		0.12		0.13		0.16	ns/pF
d_{THL}	Delta High to Low		0.09		0.10		0.12	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.*

3 – Package Pin Assignments

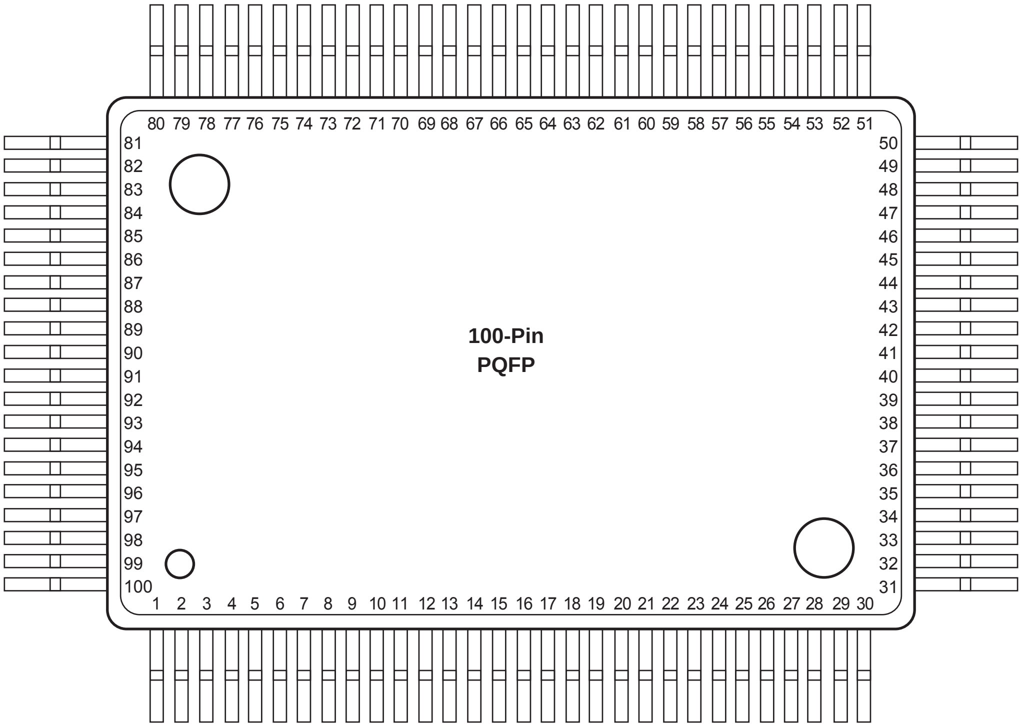
PL84



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

PQ100



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

PQ144	
Pin Number	**A1240A Function**
2	MODE
9	GND
10	GND
11	GND
18	VCC
19	VCC
20	VCC
21	VCC
28	GND
29	GND
30	GND
44	GND
45	GND
46	GND
54	VCC
55	VCC
56	VCC
64	GND
65	GND
71	SDO
79	GND
80	GND
81	GND
88	GND

PQ144	
Pin Number	**A1240A Function**
89	VCC
90	VCC
91	VCC
92	VCC
93	VCC
100	GND
101	GND
102	GND
110	SDI, I/O
116	GND
117	GND
118	GND
123	PRA, I/O
125	CLKA, I/O
126	VCC
127	VCC
128	VCC
130	CLKB, I/O
132	PRB, I/O
136	GND
137	GND
138	GND
144	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PQ160	
Pin Number	**A1280A Function**
2	DCLK, I/O
6	VCC
11	GND
16	PRB, I/O
18	CLKB, I/O
20	VCC
21	CLKA, I/O
23	PRA, I/O
30	GND
35	VCC
38	SDI, I/O
40	GND
44	GND
49	GND
54	VCC
57	VCC
58	VCC
59	GND
60	VCC
61	GND
64	GND

PQ160	
Pin Number	**A1280A Function**
69	GND
80	GND
82	SDO
86	VCC
89	GN
98	GND
99	GND
109	GND
114	VCC
120	GND
125	GND
130	GND
135	VCC
138	VCC
139	VCC
140	GND
145	GND
150	VCC
155	GND
159	MODE
160	GND

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

TQ176		
Pin Number	**A1240A Function**	**A1280A Function**
1	GND	GND
2	MODE	MODE
8	NC	NC
10	NC	I/O
11	NC	I/O
13	NC	VCC
18	GND	GND
19	NC	I/O
20	NC	I/O
22	NC	I/O
23	GND	GND
24	NC	VCC
25	VCC	VCC
26	NC	I/O
27	NC	I/O
28	VCC	VCC
29	NC	I/O
33	NC	NC
37	NC	I/O
38	NC	NC
45	GND	GND
52	NC	VCC
54	NC	I/O
55	NC	I/O
57	NC	NC
61	NC	I/O
64	NC	I/O
66	NC	I/O
67	GND	GND
68	VCC	VCC
74	NC	I/O
77	NC	NC
78	NC	I/O
80	NC	I/O

TQ176		
Pin Number	**A1240A Function**	**A1280A Function**
82	NC	VCC
86	NC	I/O
87	SDO	SDO
89	GND	GND
96	NC	I/O
97	NC	I/O
101	NC	NC
103	NC	I/O
106	GND	GND
107	NC	I/O
108	NC	I/O
109	GND	GND
110	VCC	VCC
111	GND	GND
112	VCC	VCC
113	VCC	VCC
114	NC	I/O
115	NC	I/O
116	NC	VCC
121	NC	NC
124	NC	I/O
125	NC	I/O
126	NC	NC
133	GND	GND
135	SDI, I/O	SDI, I/O
136	NC	I/O
140	NC	VCC
143	NC	I/O
144	NC	I/O
145	NC	NC
147	NC	I/O
151	NC	I/O
152	PRA, I/O	PRA, I/O
154	CLKA, I/O	CLKA, I/O

CQ172	
Pin Number	**A1280A Function**
1	MODE
7	GND
12	VCC
17	GND
22	GND
23	VCC
24	VCC
27	VCC
32	GND
37	GND
50	VCC
55	GND
65	GND
66	VCC
75	GND
80	VCC
85	SDO
98	GND
103	GND
106	GND

CQ172	
Pin Number	**A1280A Function**
107	VCC
108	GND
109	VCC
110	VCC
113	VCC
118	GND
123	GND
131	SDI, I/O
136	VCC
141	GND
148	PRA, I/O
150	CLKA, I/O
151	VCC
152	GND
154	CLKB, I/O
156	PRB, I/O
161	GND
166	VCC
171	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG100	
Pin Number	**A1225A Function**
A4	PRB, I/O
A7	PRA, I/O
B6	VCC
C2	MODE
C3	DCLK, I/O
C5	GND
C6	CLKA, I/O
C7	GND
C8	SDI, I/O
D6	CLKB, I/O
D10	GND
E3	GND

PG100	
Pin Number	**A1225A Function**
E11	VCC
F3	VCC
F9	VCC
F10	VCC
F11	GND
G1	VCC
G3	GND
G9	GND
J5	GND
J7	GND
J9	SDO
K6	VCC

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG176	
Pin Number	**A1280A Function**
A9	CLKA, I/O
B3	DCLK, I/O
B8	CLKB, I/O
B14	SDI, I/O
C3	MODE
C8	GND
C9	PRA, I/O
D4	GND
D5	VCC
D6	GND
D7	PRB, I/O
D8	VCC
D10	GND
D11	VCC
D12	GND
E4	GND
E12	GND
F4	VCC
F12	GND
G4	GND
G12	VCC
H2	VCC

PG176	
Pin Number	**A1280A Function**
H3	VCC
H4	GND
H12	GND
H13	VCC
H14	VCC
J4	VCC
J12	GND
J13	GND
J14	VCC
K4	GND
K12	GND
L4	GND
M4	GND
M5	VCC
M6	GND
M8	GND
M10	GND
M11	VCC
M12	GND
N8	VCC
P13	SDO

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

Safety Critical, Life Support, and High-Reliability Applications Policy

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