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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	140
Number of Gates	8000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	172-CQFP with Tie Bar
Supplier Device Package	172-CQFP (63.37x63.37)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microsemi/5962-9215602mya">https://www.e-xfl.com/product-detail/microsemi/5962-9215602mya</a>

## Ordering Information



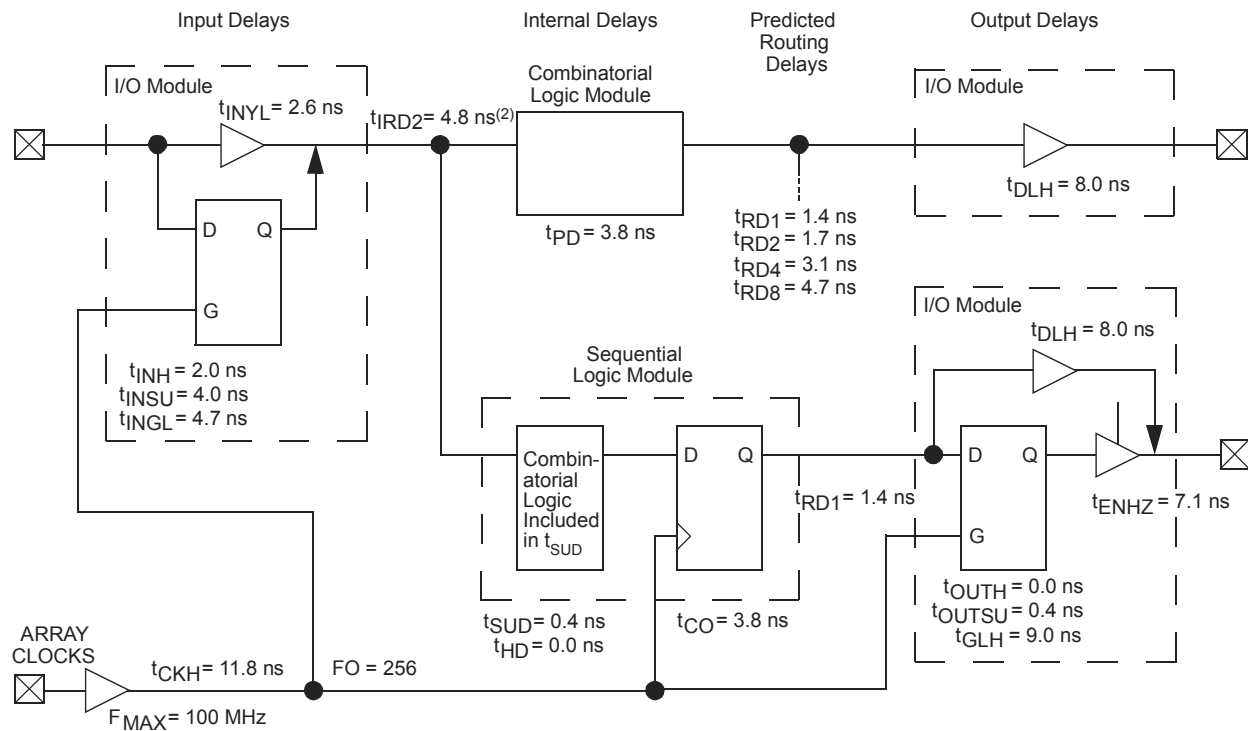
# 1 – ACT 2 Family Overview

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## General Description

The ACT 2 family represents Actel's second generation of field programmable gate arrays (FPGAs). The ACT 2 family presents a two-module architecture, consisting of C-modules and S-modules. These modules are optimized for both combinatorial and sequential designs. Based on Actel's patented channeled array architecture, the ACT 2 family provides significant enhancements to gate density and performance while maintaining downward compatibility with the ACT 1 design environment and upward compatibility with the ACT 3 design environment. The devices are implemented in silicon gate, 1.0- $\mu\text{m}$ , two-level metal CMOS, and employ Actel's PLICE® antifuse technology. This revolutionary architecture offers gate array design flexibility, high performance, and fast time-to-production with user programming. The ACT 2 family is supported by the Designer and Designer Advantage Systems, which offers automatic pin assignment, validation of electrical and design rules, automatic placement and routing, timing analysis, user programming, and diagnostic probe capabilities. The systems are supported on the following platforms: 386/486™ PC, Sun™, and HP™ workstations. The systems provide CAE interfaces to the following design environments: Cadence, Viewlogic®, Mentor Graphics®, and OrCAD™.

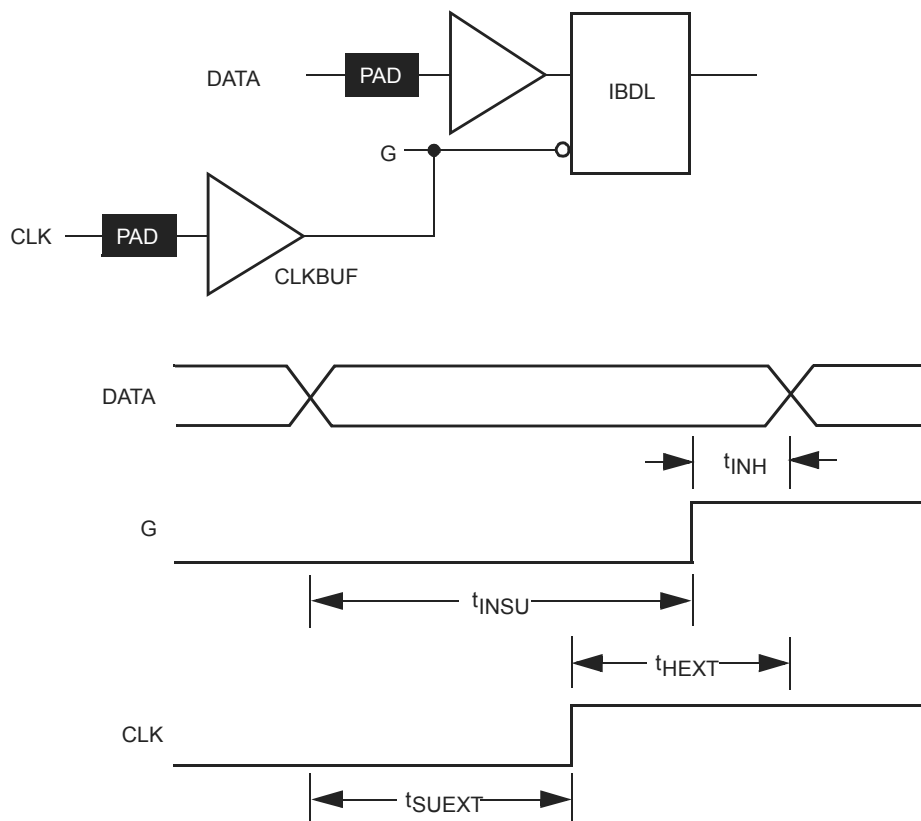
## ACT 2 Timing Model<sup>1</sup>



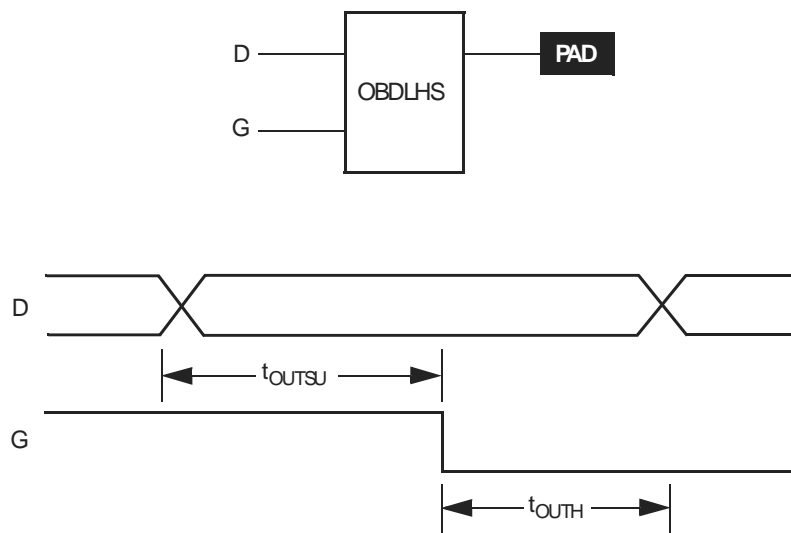
Notes:

1. Values shown for A1240A-2 at worst-case commercial conditions.
2. Input module predicted routing delay

**Figure 2-1 • Timing Model**



**Figure 2-7 • Input Buffer Latches**



**Figure 2-8 • Output Buffer Latches**

## Timing Derating Factor (Temperature and Voltage)

**Table 2-9 • Timing Derating Factor (Temperature and Voltage)**

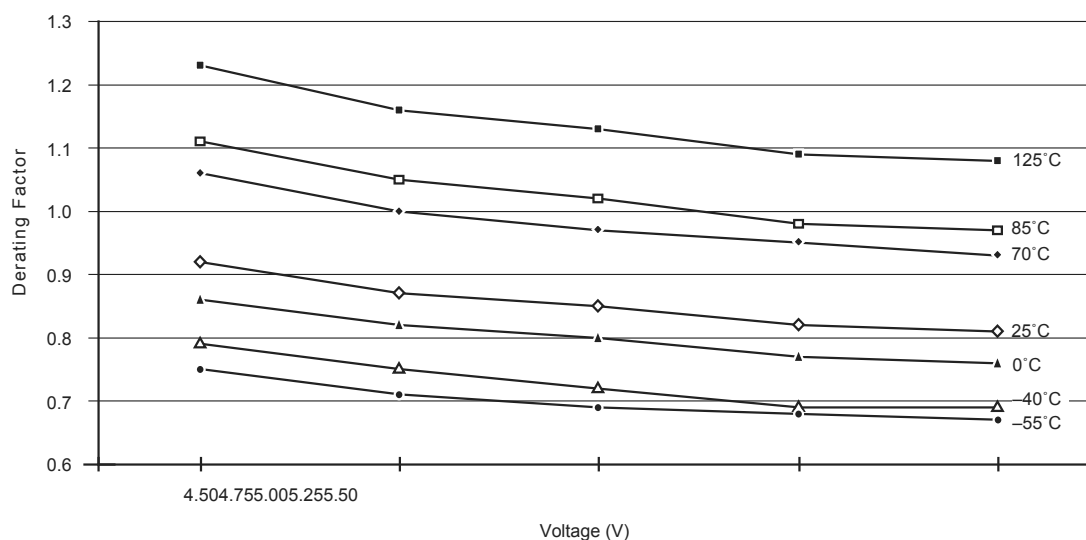
(Commercial Minimum/Maximum Specification) x	Industrial		Military	
	Min.	Max.	Min.	Max.
	0.69	1.11	0.67	1.23

**Table 2-10 • Timing Derating Factor for Designs at Typical Temperature ( $T_J = 25^\circ\text{C}$ ) and Voltage (5.0 V)**

(Commercial Maximum Specification) x	0.85
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**Table 2-11 • Temperature and Voltage Derating Factors  
(normalized to Worst-Case Commercial,  $T_J = 4.75\text{ V}$ ,  $70^\circ\text{C}$ )**

	-55	-40	0	25	70	85	125
<b>4.50</b>	0.75	0.79	0.86	0.92	1.06	1.11	1.23
<b>4.75</b>	0.71	0.75	0.82	0.87	1.00	1.05	1.13
<b>5.00</b>	0.69	0.72	0.80	0.85	0.97	1.02	1.13
<b>5.25</b>	0.68	0.69	0.77	0.82	0.95	0.98	1.09
<b>5.50</b>	0.67	0.69	0.76	0.81	0.93	0.97	1.08



*Note: This derating factor applies to all routing and propagation delays.*

**Figure 2-9 • Junction Temperature and Voltage Derating Curves  
(normalized to Worst-Case Commercial,  $T_J = 4.75\text{ V}$ ,  $70^\circ\text{C}$ )**

## A1225A Timing Characteristics (continued)

Table 2-13 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C

I/O Module Input Propagation Delays			–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description			Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>INYH</sub>	Pad to Y High			2.9		3.3		3.8	ns
t <sub>INYL</sub>	Pad to Y Low			2.6		3.0		3.5	ns
t <sub>INGH</sub>	G to Y High			5.0		5.7		6.6	ns
t <sub>INGL</sub>	G to Y Low			4.7		5.4		6.3	ns
<b>Input Module Predicted Input Routing Delays*</b>									
t <sub>IRD1</sub>	FO = 1 Routing Delay			4.1		4.6		5.4	ns
t <sub>IRD2</sub>	FO = 2 Routing Delay			4.6		5.2		6.1	ns
t <sub>IRD3</sub>	FO = 3 Routing Delay			5.3		6.0		7.1	ns
t <sub>IRD4</sub>	FO = 4 Routing Delay			5.7		6.4		7.6	ns
t <sub>IRD8</sub>	FO = 8 Routing Delay			7.4		8.3		9.8	ns
<b>Global Clock Network</b>									
t <sub>CKH</sub>	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		11.8		13.0		15.7	
t <sub>CKL</sub>	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		12.0		13.2		15.9	
t <sub>PWH</sub>	Minimum Pulse Width High	FO = 32	3.4		4.1		4.5		ns
		FO = 256	3.8		4.5		5.0		
t <sub>PWL</sub>	Minimum Pulse Width Low	FO = 32	3.4		4.1		4.5		ns
		FO = 256	3.8		4.5		5.0		
t <sub>CKSW</sub>	Maximum Skew	FO = 32		0.7		0.7		0.7	ns
		FO = 256		3.5		3.5		3.5	
t <sub>SUEXT</sub>	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t <sub>HEXT</sub>	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t <sub>P</sub>	Minimum Period	FO = 32	7.7		8.3		9.1		ns
		FO = 256	8.1		8.8		10.0		
f <sub>MAX</sub>	Maximum Frequency	FO = 32		130.0		120.0		110.0	ns
		FO = 256		125.0		115.0		100.0	

Note: \*These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

## A1225A Timing Characteristics (continued)

Table 2-14 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C

TTL Output Module Timing <sup>1</sup>		–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>DLH</sub>	Data to Pad High		8.0		9.0		10.6	ns
t <sub>DHL</sub>	Data to Pad Low		10.1		11.4		13.4	ns
t <sub>ENZH</sub>	Enable Pad Z to High		8.9		10.0		11.8	ns
t <sub>ENZL</sub>	Enable Pad Z to Low		11.6		13.2		15.5	ns
t <sub>ENHZ</sub>	Enable Pad High to Z		7.1		8.0		9.4	ns
t <sub>ENLZ</sub>	Enable Pad Low to Z		8.3		9.5		11.1	ns
t <sub>GLH</sub>	G to Pad High		8.9		10.2		11.9	ns
t <sub>GHL</sub>	G to Pad Low		11.2		12.7		14.9	ns
d <sub>TLH</sub>	Delta Low to High		0.07		0.08		0.09	ns/pF
d <sub>THL</sub>	Delta High to Low		0.12		0.13		0.16	ns/pF
CMOS Output Module Timing <sup>1</sup>								
t <sub>DLH</sub>	Data to Pad High		10.1		11.5		13.5	ns
t <sub>DHL</sub>	Data to Pad Low		8.4		9.6		11.2	ns
t <sub>ENZH</sub>	Enable Pad Z to High		8.9		10.0		11.8	ns
t <sub>ENZL</sub>	Enable Pad Z to Low		11.6		13.2		15.5	ns
t <sub>ENHZ</sub>	Enable Pad High to Z		7.1		8.0		9.4	ns
t <sub>ENLZ</sub>	Enable Pad Low to Z		8.3		9.5		11.1	ns
t <sub>GLH</sub>	G to Pad High		8.9		10.2		11.9	ns
t <sub>GHL</sub>	G to Pad Low		11.2		12.7		14.9	ns
d <sub>TLH</sub>	Delta Low to High		0.12		0.13		0.16	ns/pF
d <sub>THL</sub>	Delta High to Low		0.09		0.10		0.12	ns/pF

Notes:

1. Delays based on 50 pF loading.
2. SSO information can be found at [www.microsemi.com/soc/techdocs/appnotes/board\\_consideration.aspx](http://www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx).



## A1240A Timing Characteristics

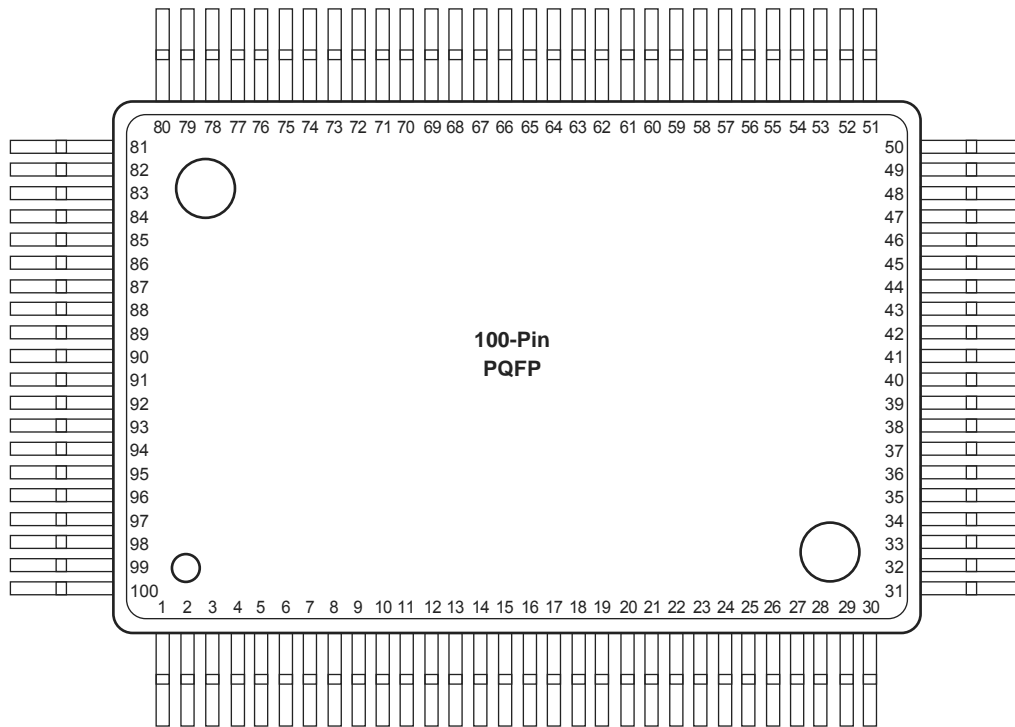
**Table 2-15 • A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C**

Logic Module Propagation Delays <sup>1</sup>		–2 Speed <sup>3</sup>		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PD1</sub>	Single Module		3.8		4.3		5.0	ns
t <sub>CO</sub>	Sequential Clock to Q		3.8		4.3		5.0	ns
t <sub>GO</sub>	Latch G to Q		3.8		4.3		5.0	ns
t <sub>RS</sub>	Flip-Flop (Latch) Reset to Q		3.8		4.3		5.0	ns
<b>Predicted Routing Delays<sup>2</sup></b>								
t <sub>RD1</sub>	FO = 1 Routing Delay		1.4		1.5		1.8	ns
t <sub>RD2</sub>	FO = 2 Routing Delay		1.7		2.0		2.3	ns
t <sub>RD3</sub>	FO = 3 Routing Delay		2.3		2.6		3.0	ns
t <sub>RD4</sub>	FO = 4 Routing Delay		3.1		3.5		4.1	ns
t <sub>RD8</sub>	FO = 8 Routing Delay		4.7		5.4		6.3	ns
<b>Sequential Timing Characteristics<sup>3,4</sup></b>								
t <sub>SUD</sub>	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		ns
t <sub>HD</sub>	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t <sub>SUENA</sub>	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		ns
t <sub>HENA</sub>	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t <sub>WCLKA</sub>	Flip-Flop (Latch) Clock Active Pulse Width	4.5		6.0		6.5		ns
t <sub>WASYN</sub>	Flip-Flop (Latch) Clock Asynchronous Pulse Width	4.5		6.0		6.5		ns
t <sub>A</sub>	Flip-Flop Clock Input Period	9.8		12.0		15.0		ns
t <sub>INH</sub>	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t <sub>INSU</sub>	Input Buffer Latch Setup	0.4		0.4		0.5		ns
t <sub>OUTH</sub>	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t <sub>OUTSU</sub>	Output Buffer Latch Setup	0.4		0.4		0.5		ns
f <sub>MAX</sub>	Flip-Flop (Latch) Clock Frequency		100.0		80.0		66.0	MHz

**Notes:**

1. For dual-module macros, use t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, t<sub>CO</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, or t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>SUD</sub>—whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
4. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

## PQ100



### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

PQ100	
Pin Number	A1225A Function
2	DCLK, I/O
4	MODE
9	GND
16	VCC
17	VCC
22	GND
34	GND
40	VCC
46	GND
52	SDO
57	GND
64	GND

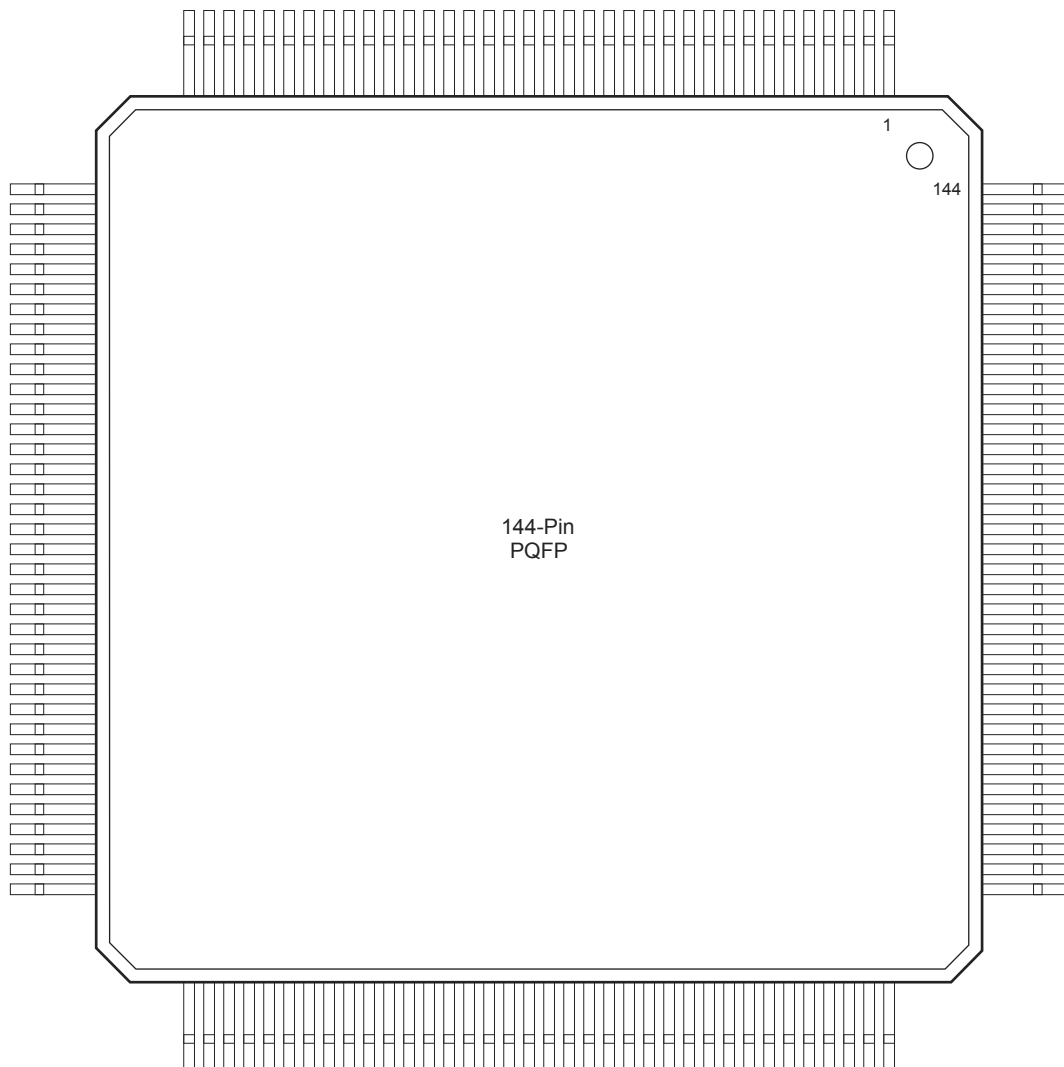
PQ100	
Pin Number	A1225A Function
65	VCC
66	VCC
67	VCC
72	GND
79	SDI, I/O
84	GND
87	PRA, I/O
89	CLKA, I/O
90	VCC
92	CLKB, I/O
94	PRB, I/O
96	GND

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

## PQ144

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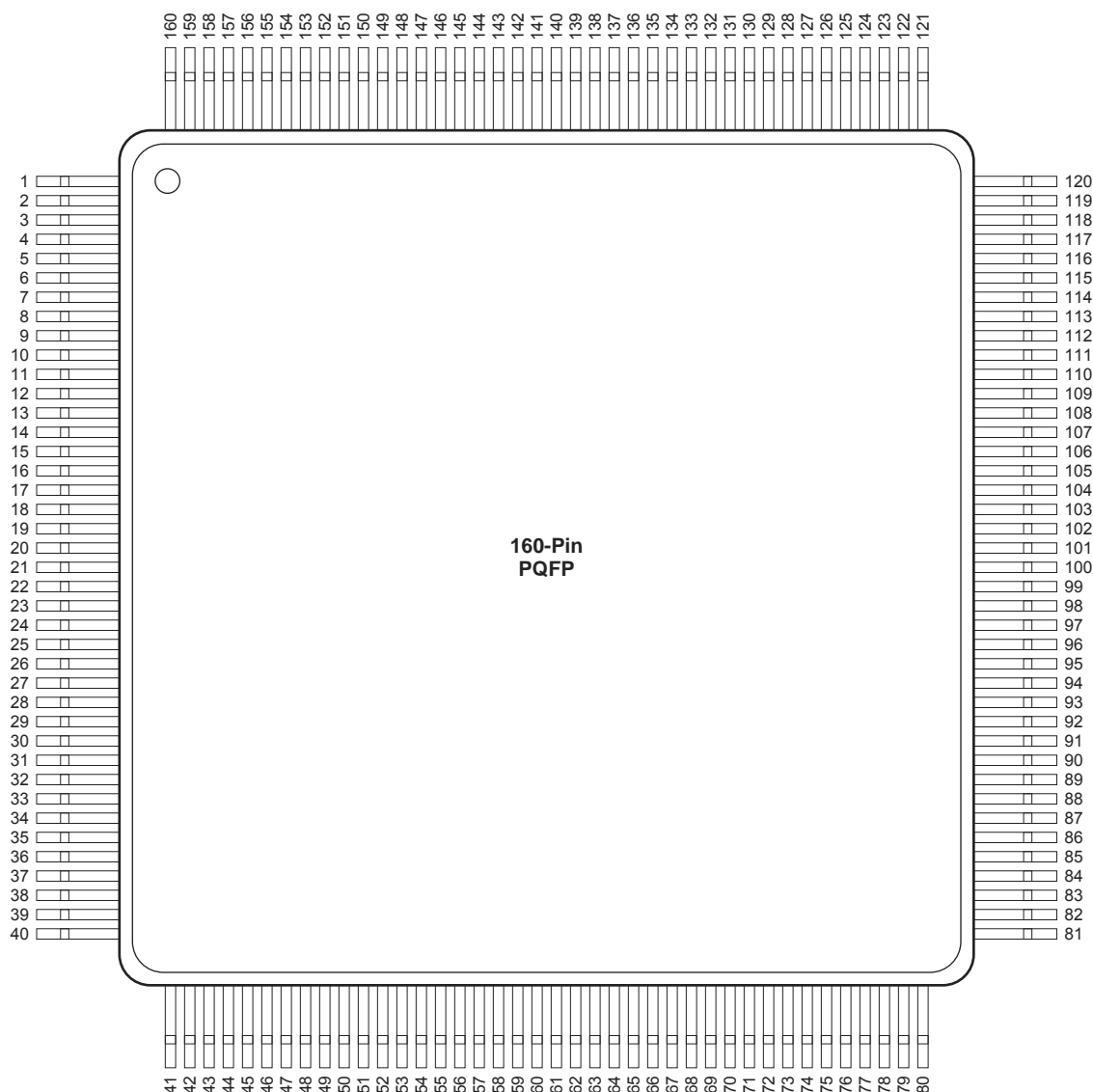


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### **Note**

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

# PQ160

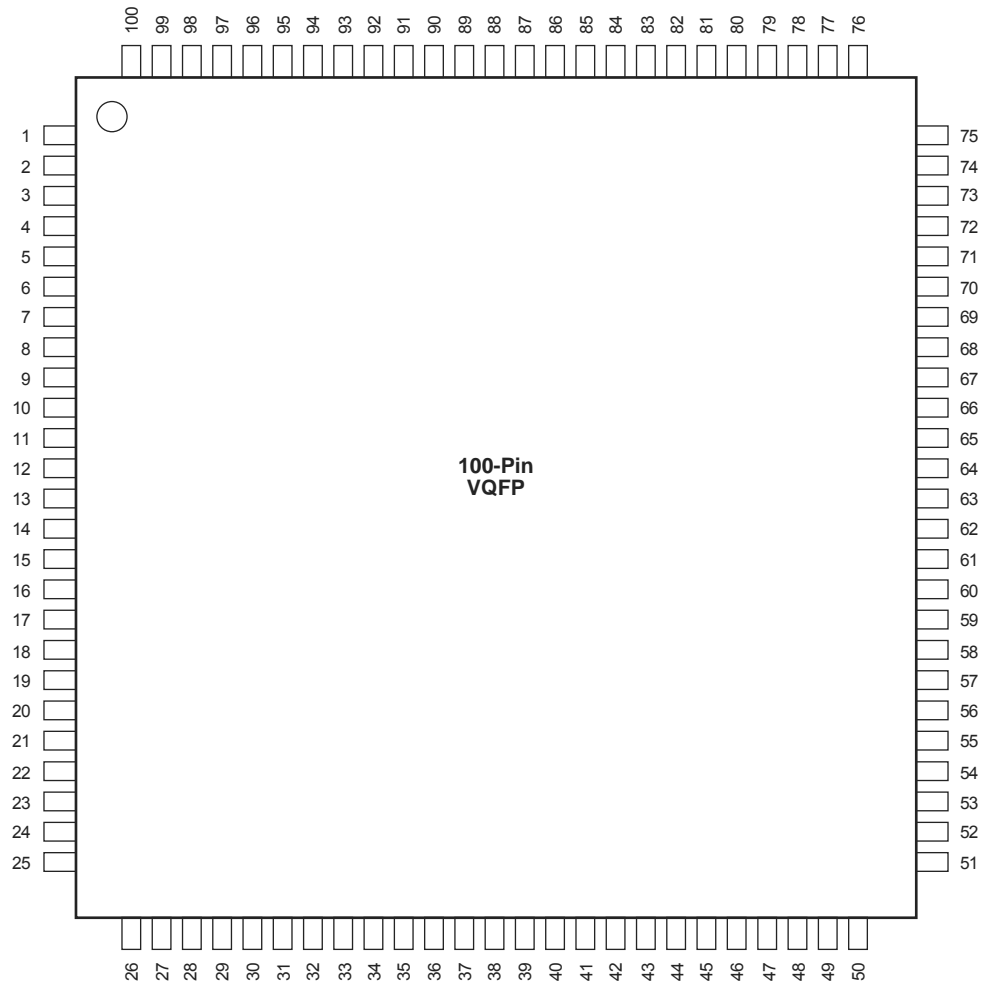


*Note:* This is the top view of the package

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

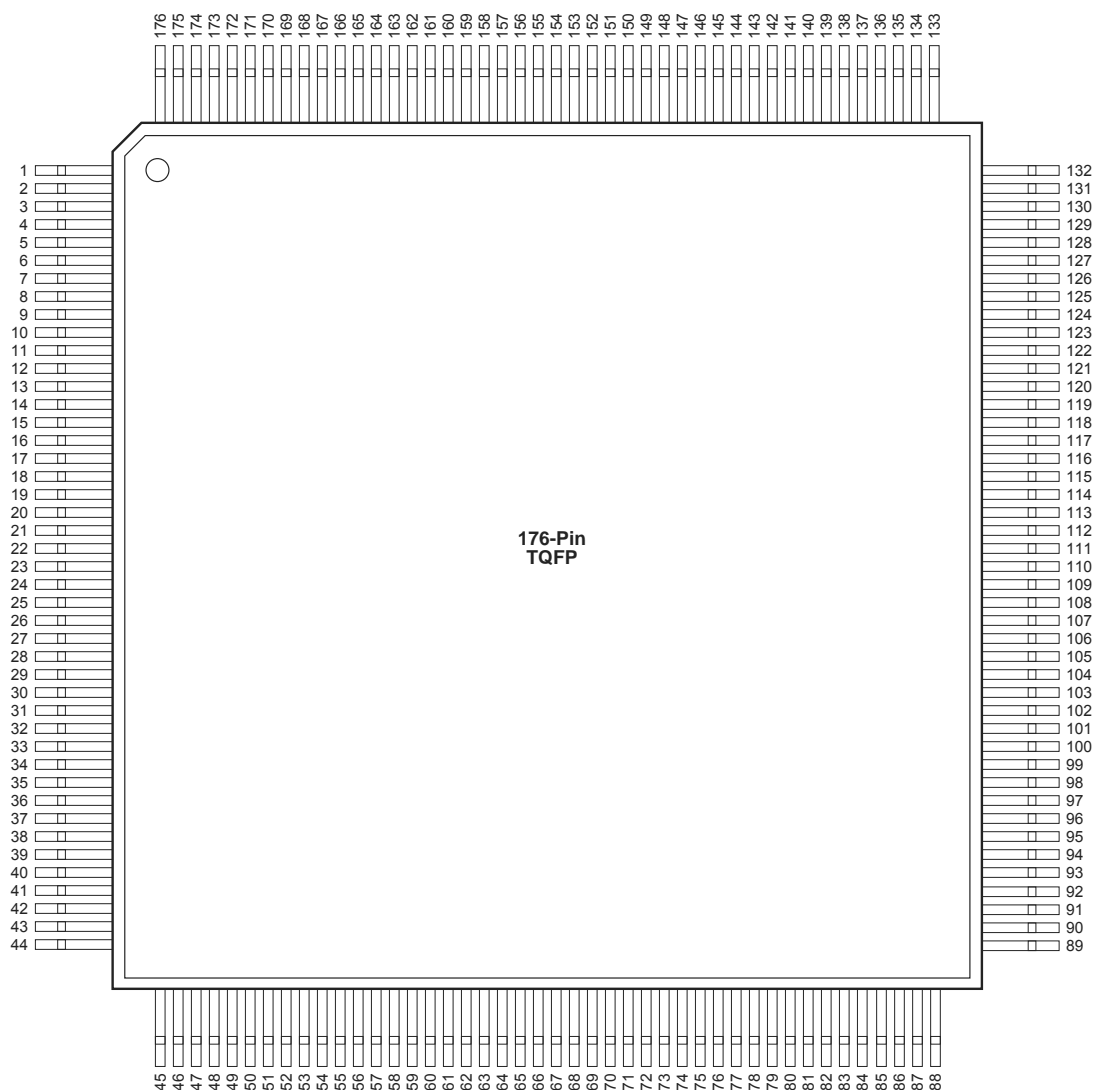
## VQ100



### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

# TQ176



## Note

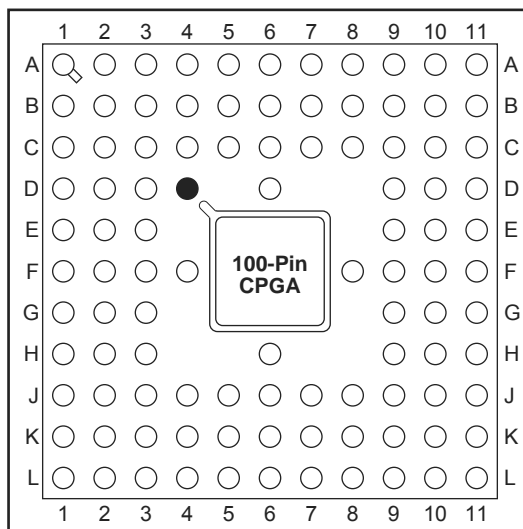
For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

TQ176		
Pin Number	A1240A Function	A1280A Function
1	GND	GND
2	MODE	MODE
8	NC	NC
10	NC	I/O
11	NC	I/O
13	NC	VCC
18	GND	GND
19	NC	I/O
20	NC	I/O
22	NC	I/O
23	GND	GND
24	NC	VCC
25	VCC	VCC
26	NC	I/O
27	NC	I/O
28	VCC	VCC
29	NC	I/O
33	NC	NC
37	NC	I/O
38	NC	NC
45	GND	GND
52	NC	VCC
54	NC	I/O
55	NC	I/O
57	NC	NC
61	NC	I/O
64	NC	I/O
66	NC	I/O
67	GND	GND
68	VCC	VCC
74	NC	I/O
77	NC	NC
78	NC	I/O
80	NC	I/O

TQ176		
Pin Number	A1240A Function	A1280A Function
82	NC	VCC
86	NC	I/O
87	SDO	SDO
89	GND	GND
96	NC	I/O
97	NC	I/O
101	NC	NC
103	NC	I/O
106	GND	GND
107	NC	I/O
108	NC	I/O
109	GND	GND
110	VCC	VCC
111	GND	GND
112	VCC	VCC
113	VCC	VCC
114	NC	I/O
115	NC	I/O
116	NC	VCC
121	NC	NC
124	NC	I/O
125	NC	I/O
126	NC	NC
133	GND	GND
135	SDI, I/O	SDI, I/O
136	NC	I/O
140	NC	VCC
143	NC	I/O
144	NC	I/O
145	NC	NC
147	NC	I/O
151	NC	I/O
152	PRA, I/O	PRA, I/O
154	CLKA, I/O	CLKA, I/O



## PG100



● Orientation Pin

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

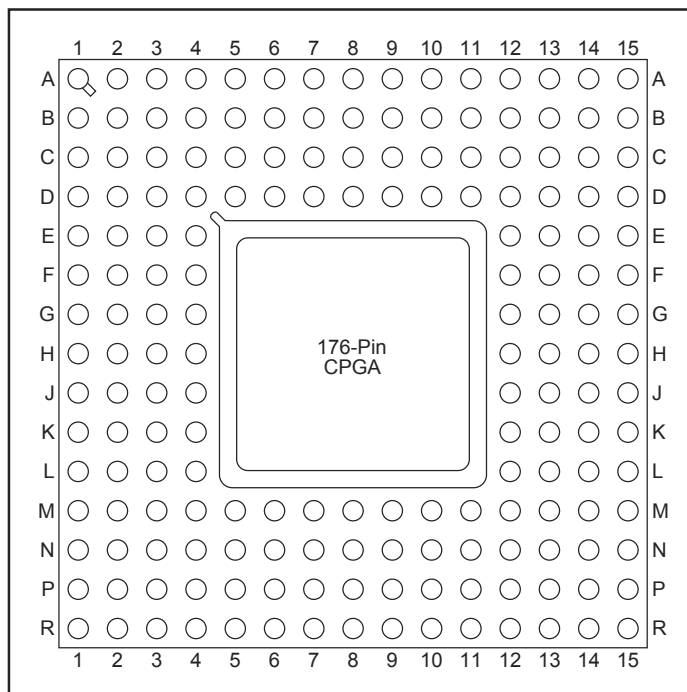
PG132	
Pin Number	A1240A Function
A1	MODE
B5	GND
B6	CLKB, I/O
B7	CLKA, I/O
B8	PRA, I/O
B9	GND
B12	SDI, I/O
C3	DCLK, I/O
C5	GND
C6	PRB, I/O
C7	VCC
C9	GND
D7	VCC
E3	GND
E11	GND
E12	GND
F4	GND
G2	VCC

PG132	
Pin Number	A1240A Function
G3	VCC
G4	VCC
G10	VCC
G11	VCC
G12	VCC
G13	VCC
H13	GND
J2	GND
J3	GND
J11	GND
K7	VCC
K12	GND
L5	GND
L7	VCC
L9	GND
M9	GND
N12	SDO

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

## PG176



### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

PG176	
Pin Number	A1280A Function
A9	CLKA, I/O
B3	DCLK, I/O
B8	CLKB, I/O
B14	SDI, I/O
C3	MODE
C8	GND
C9	PRA, I/O
D4	GND
D5	VCC
D6	GND
D7	PRB, I/O
D8	VCC
D10	GND
D11	VCC
D12	GND
E4	GND
E12	GND
F4	VCC
F12	GND
G4	GND
G12	VCC
H2	VCC

PG176	
Pin Number	A1280A Function
H3	VCC
H4	GND
H12	GND
H13	VCC
H14	VCC
J4	VCC
J12	GND
J13	GND
J14	VCC
K4	GND
K12	GND
L4	GND
M4	GND
M5	VCC
M6	GND
M8	GND
M10	GND
M11	VCC
M12	GND
N8	VCC
P13	SDO

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

