Microsemi Corporation - A1225A-1PQ100I Datasheet

**Welcome to E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

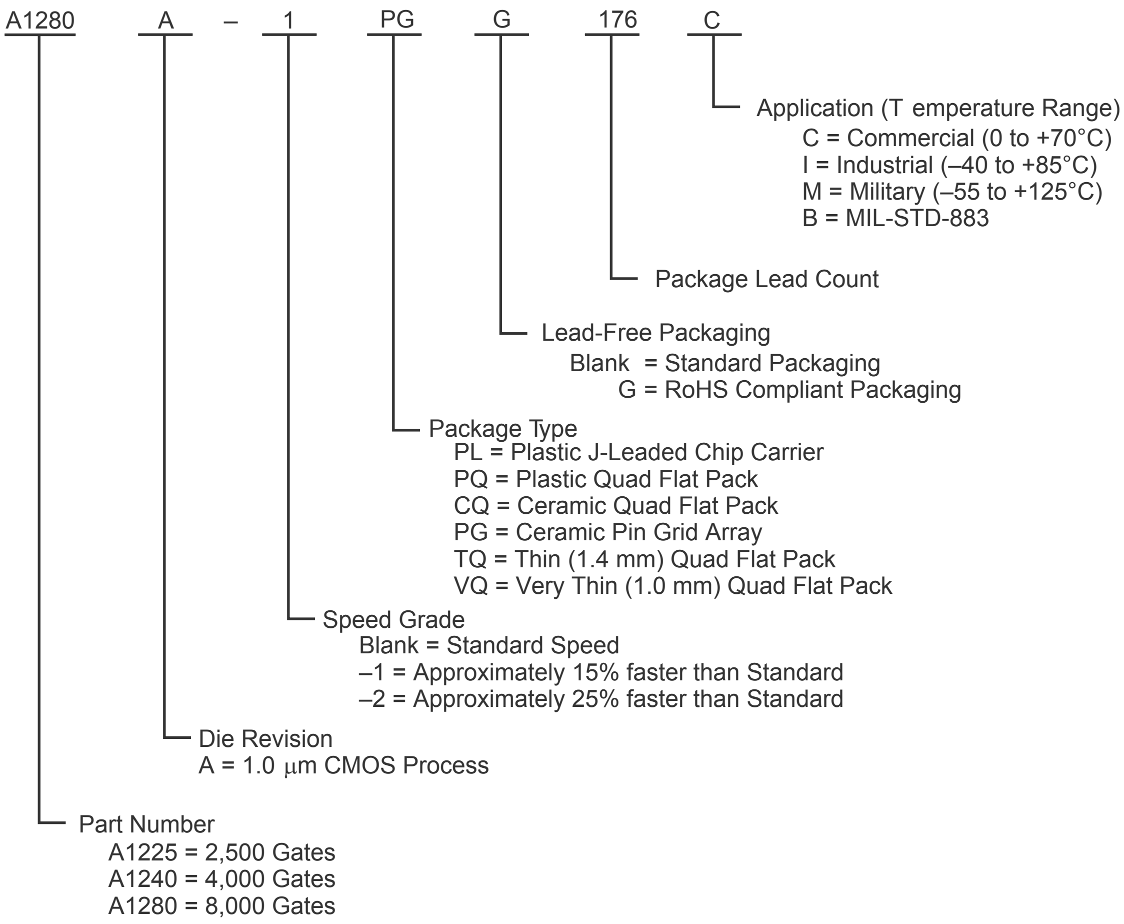
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 451 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 83 |
| Number of Gates | 2500 |
| Voltage - Supply | 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 100-BQFP |
| Supplier Device Package | 100-PQFP (20x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a1225a-1pq100i |

# Ordering Information



A1280 A – 1 PG G 176 C

Application (Temperature Range)
C = Commercial (0 to +70°C)
I = Industrial (–40 to +85°C)
M = Military (–55 to +125°C)
B = MIL-STD-883

Package Lead Count

Lead-Free Packaging
Blank = Standard Packaging
G = RoHS Compliant Packaging

Package Type
PL = Plastic J-Leaded Chip Carrier
PQ = Plastic Quad Flat Pack
CQ = Ceramic Quad Flat Pack
PG = Ceramic Pin Grid Array
TQ = Thin (1.4 mm) Quad Flat Pack
VQ = Very Thin (1.0 mm) Quad Flat Pack

Speed Grade
Blank = Standard Speed
–1 = Approximately 15% faster than Standard
–2 = Approximately 25% faster than Standard

Die Revision
A = 1.0 μm CMOS Process

Part Number
A1225 = 2,500 Gates
A1240 = 4,000 Gates
A1280 = 8,000 Gates

# 2 – Detailed Specifications

## Operating Conditions

*Table 2-1* • **Absolute Maximum Ratings**[1]

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| VCC | DC supply voltage | –0.5 to +7.0 | V |
| VI | Input voltage | –0.5 to VCC + 0.5 | V |
| VO | Output voltage | –0.5 to VCC + 0.5 | V |
| IIO | I/O source sink current[2] | ±20 | mA |
| $T_{STG}$ | Storage temperature | –65 to +150 | °C |

*Notes:*

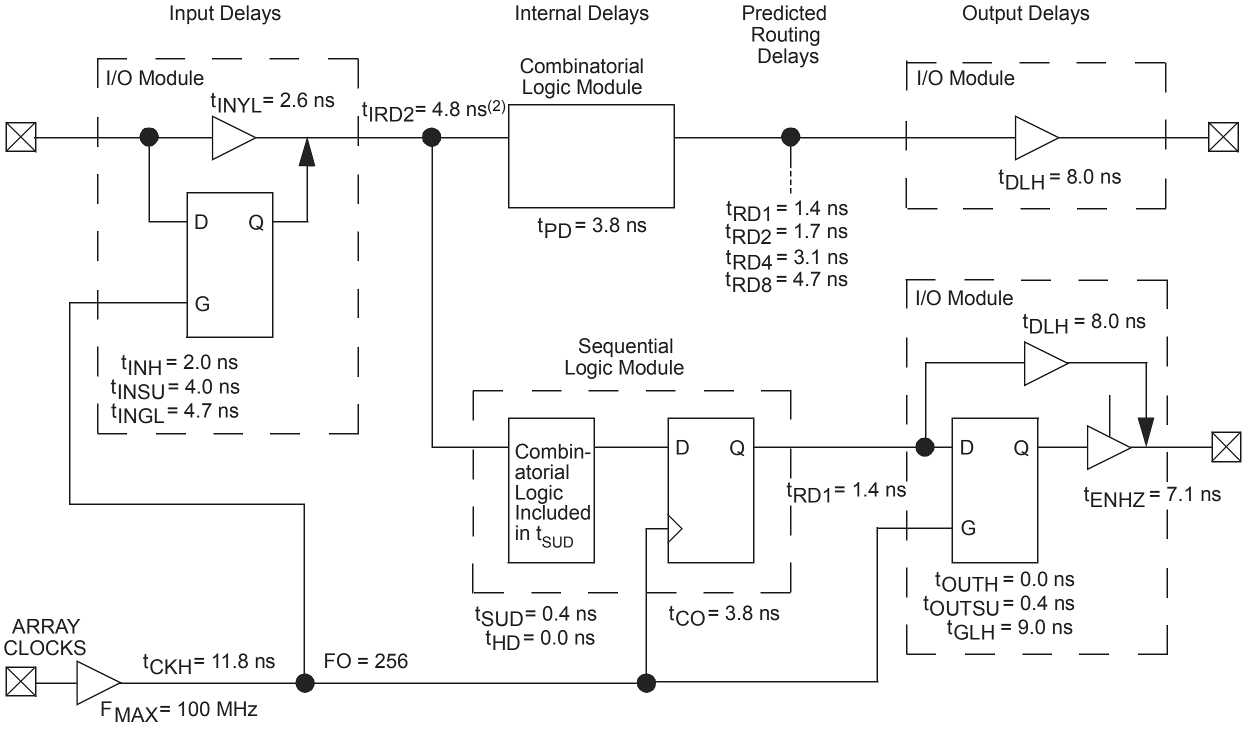
1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND –0.5 V, the internal protection diodes will be forward biased and can draw excessive current.*

*Table 2-2* • **Recommended Operating Conditions**

| Parameter | Commercial | Industrial | Military | Units |
|---|---|---|---|---|
| Temperature range* | 0 to +70 | –40 to +85 | –55 to +125 | °C |
| Power supply tolerance | ±5 | ±10 | ±10 | %VCC |

*Note: *Ambient temperature ($T_A$) is used for commercial and industrial; case temperature ($T_C$) is used for military.*

# ACT 2 Timing Model[1]



*Notes:*

1. *Values shown for A1240A-2 at worst-case commercial conditions.*
2. *Input module predicted routing delay*

***Figure 2-1 •*** **Timing Model**

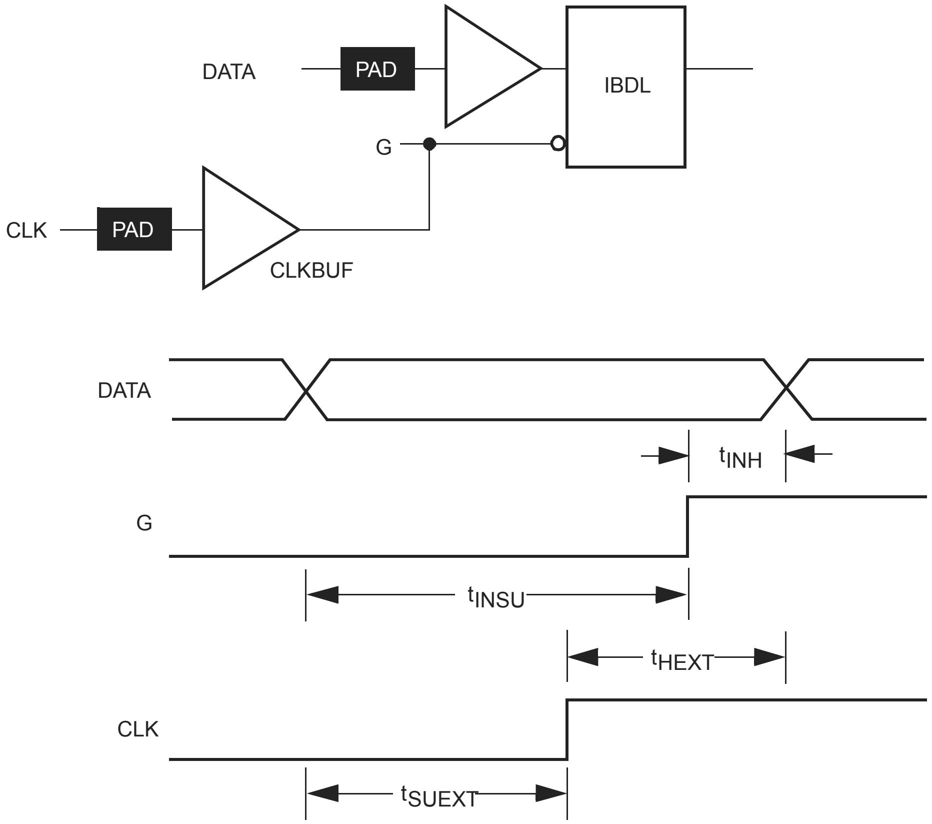


*Figure 2-7 •* **Input Buffer Latches**

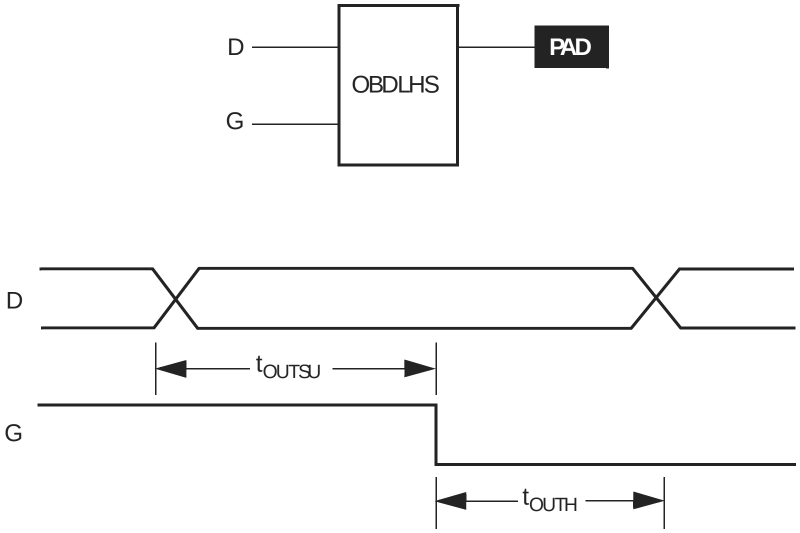


*Figure 2-8 •* **Output Buffer Latches**

## A1225A Timing Characteristics

***Table 2-12* • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| **Logic Module Propagation Delays[1]** | | **–2 Speed[3]** | | **–1 Speed** | | **Std. Speed** | | **Units** |
|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{PD1}$ | Single Module | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{CO}$ | Sequential Clock to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{GO}$ | Latch G to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{RS}$ | Flip-Flop (Latch) Reset to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| **Predicted Routing Delays[2]** | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 1.1 | | 1.2 | | 1.4 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.7 | | 1.9 | | 2.2 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 2.3 | | 2.6 | | 3.0 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 2.8 | | 3.1 | | 3.7 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 4.4 | | 4.9 | | 5.8 | ns |
| **Sequential Timing Characteristics[3,4]** | | | | | | | | |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Setup | 0.8 | | 0.9 | | 1.0 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 4.5 | | 5.0 | | 6.0 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Clock Asynchronous Pulse Width | 4.5 | | 5.0 | | 6.0 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 9.4 | | 11.0 | | 13.0 | | ns |
| $t_{INH}$ | Input Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Buffer Latch Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| $t_{OUTH}$ | Output Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTSU}$ | Output Buffer Latch Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency | | 105.0 | | 90.0 | | 75.0 | MHz |

*Notes:*

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$—whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

## A1225A Timing Characteristics (continued)

***Table 2-13* • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| **I/O Module Input Propagation Delays** | | | **–2 Speed** | | **–1 Speed** | | **Std. Speed** | | **Units** |
|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{INYH}$ | Pad to Y High | | | 2.9 | | 3.3 | | 3.8 | ns |
| $t_{INYL}$ | Pad to Y Low | | | 2.6 | | 3.0 | | 3.5 | ns |
| $t_{INGH}$ | G to Y High | | | 5.0 | | 5.7 | | 6.6 | ns |
| $t_{INGL}$ | G to Y Low | | | 4.7 | | 5.4 | | 6.3 | ns |
| **Input Module Predicted Input Routing Delays*** | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | | 4.1 | | 4.6 | | 5.4 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | | 4.6 | | 5.2 | | 6.1 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | | 5.3 | | 6.0 | | 7.1 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | | 5.7 | | 6.4 | | 7.6 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | | 7.4 | | 8.3 | | 9.8 | ns |
| **Global Clock Network** | | | | | | | | | |
| $t_{CKH}$ | Input Low to High | FO = 32 | | 10.2 | | 11.0 | | 12.8 | ns |
| | | FO = 256 | | 11.8 | | 13.0 | | 15.7 | |
| $t_{CKL}$ | Input High to Low | FO = 32 | | 10.2 | | 11.0 | | 12.8 | ns |
| | | FO = 256 | | 12.0 | | 13.2 | | 15.9 | |
| $t_{PWH}$ | Minimum Pulse Width High | FO = 32 | 3.4 | | 4.1 | | 4.5 | | ns |
| | | FO = 256 | 3.8 | | 4.5 | | 5.0 | | |
| $t_{PWL}$ | Minimum Pulse Width Low | FO = 32 | 3.4 | | 4.1 | | 4.5 | | ns |
| | | FO = 256 | 3.8 | | 4.5 | | 5.0 | | |
| $t_{CKSW}$ | Maximum Skew | FO = 32 | | 0.7 | | 0.7 | | 0.7 | ns |
| | | FO = 256 | | 3.5 | | 3.5 | | 3.5 | |
| $t_{SUEXT}$ | Input Latch External Setup | FO = 32 | 0.0 | | 0.0 | | 0.0 | | ns |
| | | FO = 256 | 0.0 | | 0.0 | | 0.0 | | |
| $t_{HEXT}$ | Input Latch External Hold | FO = 32 | 7.0 | | 7.0 | | 7.0 | | ns |
| | | FO = 256 | 11.2 | | 11.2 | | 11.2 | | |
| $t_P$ | Minimum Period | FO = 32 | 7.7 | | 8.3 | | 9.1 | | ns |
| | | FO = 256 | 8.1 | | 8.8 | | 10.0 | | |
| $f_{MAX}$ | Maximum Frequency | FO = 32 | | 130.0 | | 120.0 | | 110.0 | ns |
| | | FO = 256 | | 125.0 | | 115.0 | | 100.0 | |

*Note: *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

## A1240A Timing Characteristics

***Table 2-15* • A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| **Logic Module Propagation Delays**[1] | | **–2 Speed**[3] | | **–1 Speed** | | **Std. Speed** | | **Units** |
|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{PD1}$ | Single Module | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{CO}$ | Sequential Clock to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{GO}$ | Latch G to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{RS}$ | Flip-Flop (Latch) Reset to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| **Predicted Routing Delays**[2] | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 1.4 | | 1.5 | | 1.8 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.7 | | 2.0 | | 2.3 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 2.3 | | 2.6 | | 3.0 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 3.1 | | 3.5 | | 4.1 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 4.7 | | 5.4 | | 6.3 | ns |
| **Sequential Timing Characteristics**[3,4] | | | | | | | | |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Setup | 0.8 | | 0.9 | | 1.0 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 4.5 | | 6.0 | | 6.5 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Clock Asynchronous Pulse Width | 4.5 | | 6.0 | | 6.5 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 9.8 | | 12.0 | | 15.0 | | ns |
| $t_{INH}$ | Input Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Buffer Latch Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| $t_{OUTH}$ | Output Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTSU}$ | Output Buffer Latch Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency | | 100.0 | | 80.0 | | 66.0 | MHz |

*Notes:*

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$—whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

## A1240A Timing Characteristics (continued)

***Table 2-17* • A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| **TTL Output Module Timing**[1] | | **–2 Speed** | | **–1 Speed** | | **Std. Speed** | | **Units** |
|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{DLH}$ | Data to Pad High | | 8.0 | | 9.0 | | 10.6 | ns |
| $t_{DHL}$ | Data to Pad Low | | 10.1 | | 11.4 | | 13.4 | ns |
| $t_{ENZH}$ | Enable Pad Z to High | | 8.9 | | 10.0 | | 11.8 | ns |
| $t_{ENZL}$ | Enable Pad Z to Low | | 11.7 | | 13.2 | | 15.5 | ns |
| $t_{ENHZ}$ | Enable Pad High to Z | | 7.1 | | 8.0 | | 9.4 | ns |
| $t_{ENLZ}$ | Enable Pad Low to Z | | 8.4 | | 9.5 | | 11.1 | ns |
| $t_{GLH}$ | G to Pad High | | 9.0 | | 10.2 | | 11.9 | ns |
| $t_{GHL}$ | G to Pad Low | | 11.2 | | 12.7 | | 14.9 | ns |
| $d_{TLH}$ | Delta Low to High | | 0.07 | | 0.08 | | 0.09 | ns/pF |
| $d_{THL}$ | Delta High to Low | | 0.12 | | 0.13 | | 0.16 | ns/pF |
| **CMOS Output Module Timing**[1] | | | | | | | | |
| $t_{DLH}$ | Data to Pad High | | 10.2 | | 11.5 | | 13.5 | ns |
| $t_{DHL}$ | Data to Pad Low | | 8.4 | | 9.6 | | 11.2 | ns |
| $t_{ENZH}$ | Enable Pad Z to High | | 8.9 | | 10.0 | | 11.8 | ns |
| $t_{ENZL}$ | Enable Pad Z to Low | | 11.7 | | 13.2 | | 15.5 | ns |
| $t_{ENHZ}$ | Enable Pad High to Z | | 7.1 | | 8.0 | | 9.4 | ns |
| $t_{ENLZ}$ | Enable Pad Low to Z | | 8.4 | | 9.5 | | 11.1 | ns |
| $t_{GLH}$ | G to Pad High | | 9.0 | | 10.2 | | 11.9 | ns |
| $t_{GHL}$ | G to Pad Low | | 11.2 | | 12.7 | | 14.9 | ns |
| $d_{TLH}$ | Delta Low to High | | 0.12 | | 0.13 | | 0.16 | ns/pF |
| $d_{THL}$ | Delta High to Low | | 0.09 | | 0.10 | | 0.12 | ns/pF |

*Notes:*

1. *Delays based on 50 pF loading.*
2. *SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.*

**Table 2-20** • **A1280A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| **TTL Output Module Timing[1]** | | **–2 Speed** | | **–1 Speed** | | **Std. Speed** | | **Units** |
|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{DLH}$ | Data to Pad High | | 8.1 | | 9.0 | | 10.6 | ns |
| $t_{DHL}$ | Data to Pad Low | | 10.2 | | 11.4 | | 13.4 | ns |
| $t_{ENZH}$ | Enable Pad Z to High | | 9.0 | | 10.0 | | 11.8 | ns |
| $t_{ENZL}$ | Enable Pad Z to Low | | 11.8 | | 13.2 | | 15.5 | ns |
| $t_{ENHZ}$ | Enable Pad High to Z | | 7.1 | | 8.0 | | 9.4 | ns |
| $t_{ENLZ}$ | Enable Pad Low to Z | | 8.4 | | 9.5 | | 11.1 | ns |
| $t_{GLH}$ | G to Pad High | | 9.0 | | 10.2 | | 11.9 | ns |
| $t_{GHL}$ | G to Pad Low | | 11.3 | | 12.7 | | 14.9 | ns |
| $d_{TLH}$ | Delta Low to High | | 0.07 | | 0.08 | | 0.09 | ns/pF |
| $d_{THL}$ | Delta High to Low | | 0.12 | | 0.13 | | 0.16 | ns/pF |
| **CMOS Output Module Timing[1]** | | | | | | | | |
| $t_{DLH}$ | Data to Pad High | | 10.3 | | 11.5 | | 13.5 | ns |
| $t_{DHL}$ | Data to Pad Low | | 8.5 | | 9.6 | | 11.2 | ns |
| $t_{ENZH}$ | Enable Pad Z to High | | 9.0 | | 10.0 | | 11.8 | ns |
| $t_{ENZL}$ | Enable Pad Z to Low | | 11.8 | | 13.2 | | 15.5 | ns |
| $t_{ENHZ}$ | Enable Pad High to Z | | 7.1 | | 8.0 | | 9.4 | ns |
| $t_{ENLZ}$ | Enable Pad Low to Z | | 8.4 | | 9.5 | | 11.1 | ns |
| $t_{GLH}$ | G to Pad High | | 9.0 | | 10.2 | | 11.9 | ns |
| $t_{GHL}$ | G to Pad Low | | 11.3 | | 12.7 | | 14.9 | ns |
| $d_{TLH}$ | Delta Low to High | | 0.12 | | 0.13 | | 0.16 | ns/pF |
| $d_{THL}$ | Delta High to Low | | 0.09 | | 0.10 | | 0.12 | ns/pF |

*Notes:*

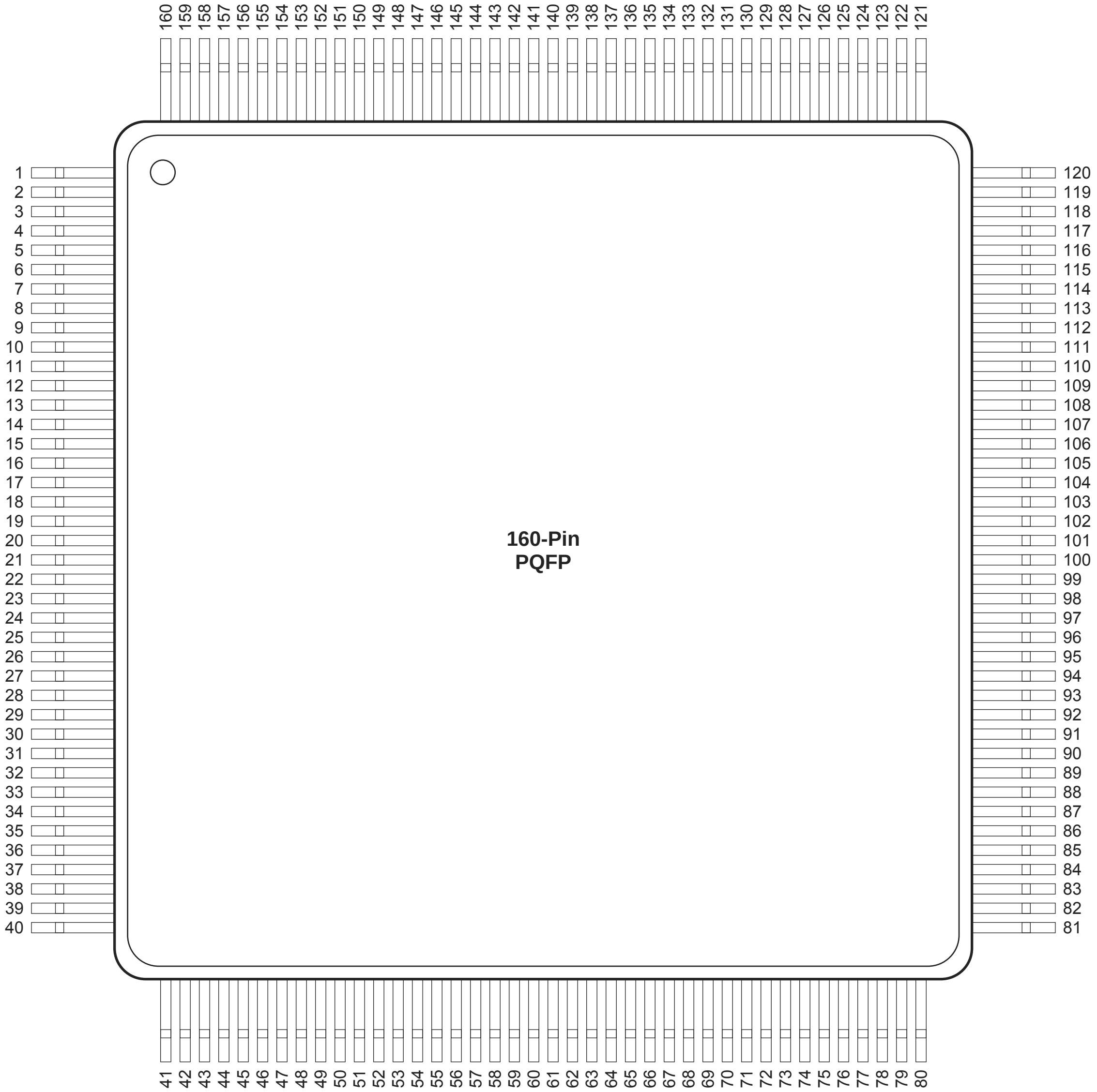
1. *Delays based on 50 pF loading.*
2. *SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.*

| PL84 | | | |
|---|---|---|---|
| **Pin Number** | **A1225A Function** | **A1240A Function** | **A1280A Function** |
| 2 | CLKB, I/O | CLKB, I/O | CLKB, I/O |
| 4 | PRB, I/O | PRB, I/O | PRB, I/O |
| 6 | GND | GND | GND |
| 10 | DCLK, I/O | DCLK, I/O | DCLK, I/O |
| 12 | MODE | MODE | MODE |
| 22 | VCC | VCC | VCC |
| 23 | VCC | VCC | VCC |
| 28 | GND | GND | GND |
| 43 | VCC | VCC | VCC |
| 49 | GND | GND | GND |
| 52 | SDO | SDO | SDO |
| 63 | GND | GND | GND |
| 64 | VCC | VCC | VCC |
| 65 | VCC | VCC | VCC |
| 70 | GND | GND | GND |
| 76 | SDI, I/O | SDI, I/O | SDI, I/O |
| 81 | PRA, I/O | PRA, I/O | PRA, I/O |
| 83 | CLKA, I/O | CLKA, I/O | CLKA, I/O |
| 84 | VCC | VCC | VCC |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

## PQ160



*Note: This is the top view of the package*

## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

| **VQ100** | |
|---|---|
| **Pin Number** | **A1225A Function** |
| 2 | MODE |
| 7 | GND |
| 14 | VCC |
| 15 | VCC |
| 20 | GND |
| 32 | GND |
| 38 | VCC |
| 44 | GND |
| 50 | SDO |
| 55 | GND |
| 62 | GND |
| 63 | VCC |

| **VQ100** | |
|---|---|
| **Pin Number** | **A1225A Function** |
| 64 | VCC |
| 65 | VCC |
| 70 | GND |
| 77 | SDI, I/O |
| 82 | GND |
| 85 | PRA, I/O |
| 87 | CLKA, I/O |
| 88 | VCC |
| 90 | CLKB, I/O |
| 92 | PRB, I/O |
| 94 | GND |
| 100 | DCLK, I/O |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

| TQ176 | | |
|---|---|---|
| **Pin Number** | **A1240A Function** | **A1280A Function** |
| 1 | GND | GND |
| 2 | MODE | MODE |
| 8 | NC | NC |
| 10 | NC | I/O |
| 11 | NC | I/O |
| 13 | NC | VCC |
| 18 | GND | GND |
| 19 | NC | I/O |
| 20 | NC | I/O |
| 22 | NC | I/O |
| 23 | GND | GND |
| 24 | NC | VCC |
| 25 | VCC | VCC |
| 26 | NC | I/O |
| 27 | NC | I/O |
| 28 | VCC | VCC |
| 29 | NC | I/O |
| 33 | NC | NC |
| 37 | NC | I/O |
| 38 | NC | NC |
| 45 | GND | GND |
| 52 | NC | VCC |
| 54 | NC | I/O |
| 55 | NC | I/O |
| 57 | NC | NC |
| 61 | NC | I/O |
| 64 | NC | I/O |
| 66 | NC | I/O |
| 67 | GND | GND |
| 68 | VCC | VCC |
| 74 | NC | I/O |
| 77 | NC | NC |
| 78 | NC | I/O |
| 80 | NC | I/O |

| TQ176 | | |
|---|---|---|
| **Pin Number** | **A1240A Function** | **A1280A Function** |
| 82 | NC | VCC |
| 86 | NC | I/O |
| 87 | SDO | SDO |
| 89 | GND | GND |
| 96 | NC | I/O |
| 97 | NC | I/O |
| 101 | NC | NC |
| 103 | NC | I/O |
| 106 | GND | GND |
| 107 | NC | I/O |
| 108 | NC | I/O |
| 109 | GND | GND |
| 110 | VCC | VCC |
| 111 | GND | GND |
| 112 | VCC | VCC |
| 113 | VCC | VCC |
| 114 | NC | I/O |
| 115 | NC | I/O |
| 116 | NC | VCC |
| 121 | NC | NC |
| 124 | NC | I/O |
| 125 | NC | I/O |
| 126 | NC | NC |
| 133 | GND | GND |
| 135 | SDI, I/O | SDI, I/O |
| 136 | NC | I/O |
| 140 | NC | VCC |
| 143 | NC | I/O |
| 144 | NC | I/O |
| 145 | NC | NC |
| 147 | NC | I/O |
| 151 | NC | I/O |
| 152 | PRA, I/O | PRA, I/O |
| 154 | CLKA, I/O | CLKA, I/O |

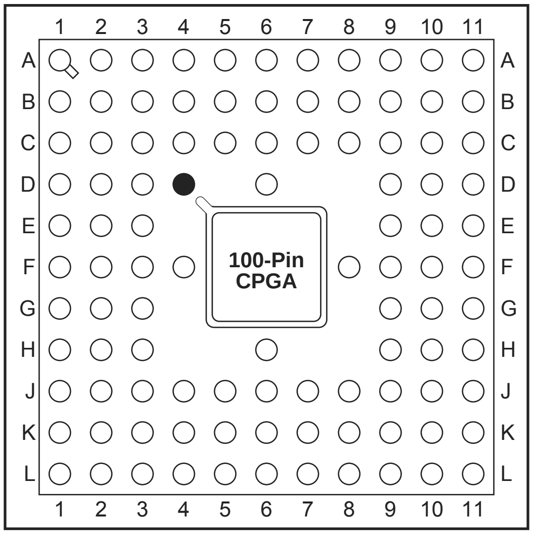
| CQ172 | |
|---|---|
| **Pin Number** | **A1280A Function** |
| 1 | MODE |
| 7 | GND |
| 12 | VCC |
| 17 | GND |
| 22 | GND |
| 23 | VCC |
| 24 | VCC |
| 27 | VCC |
| 32 | GND |
| 37 | GND |
| 50 | VCC |
| 55 | GND |
| 65 | GND |
| 66 | VCC |
| 75 | GND |
| 80 | VCC |
| 85 | SDO |
| 98 | GND |
| 103 | GND |
| 106 | GND |

| CQ172 | |
|---|---|
| **Pin Number** | **A1280A Function** |
| 107 | VCC |
| 108 | GND |
| 109 | VCC |
| 110 | VCC |
| 113 | VCC |
| 118 | GND |
| 123 | GND |
| 131 | SDI, I/O |
| 136 | VCC |
| 141 | GND |
| 148 | PRA, I/O |
| 150 | CLKA, I/O |
| 151 | VCC |
| 152 | GND |
| 154 | CLKB, I/O |
| 156 | PRB, I/O |
| 161 | GND |
| 166 | VCC |
| 171 | DCLK, I/O |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

# PG100



## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

| PG176 | |
|---|---|
| **Pin Number** | **A1280A Function** |
| A9 | CLKA, I/O |
| B3 | DCLK, I/O |
| B8 | CLKB, I/O |
| B14 | SDI, I/O |
| C3 | MODE |
| C8 | GND |
| C9 | PRA, I/O |
| D4 | GND |
| D5 | VCC |
| D6 | GND |
| D7 | PRB, I/O |
| D8 | VCC |
| D10 | GND |
| D11 | VCC |
| D12 | GND |
| E4 | GND |
| E12 | GND |
| F4 | VCC |
| F12 | GND |
| G4 | GND |
| G12 | VCC |
| H2 | VCC |

| PG176 | |
|---|---|
| **Pin Number** | **A1280A Function** |
| H3 | VCC |
| H4 | GND |
| H12 | GND |
| H13 | VCC |
| H14 | VCC |
| J4 | VCC |
| J12 | GND |
| J13 | GND |
| J14 | VCC |
| K4 | GND |
| K12 | GND |
| L4 | GND |
| M4 | GND |
| M5 | VCC |
| M6 | GND |
| M8 | GND |
| M10 | GND |
| M11 | VCC |
| M12 | GND |
| N8 | VCC |
| P13 | SDO |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

# 4 – Datasheet Information

## List of Changes

The following table lists critical changes that were made in each version of the datasheet.

| Revision | Changes | Page |
|---|---|---|
| Revision 8<br>(January 2012) | The ACT 2 datasheet was formatted newly in the style used for current datasheets. The same information is present (other than noted in the list of changes for this revision) but divided into chapters. | N/A |
| | Package names used in Table 1 • ACT 2 Product Family Profile and throughout the document were revised to match standards given in *Package Mechanical Drawings* (SAR 27395). | I |
| | The description for SDO pins had earlier been removed from the datasheet and has now been included again, in the "Pin Descriptions" section (SAR 35819). | 2-21 |
| | SDO pin numbers had earlier been removed from package pin assignment tables in the datasheet, and have now been restored to the pin tables (SAR 35819). | 3-2 |
| Revision 7<br>(June 2006) | The "Ordering Information" section was revised to include RoHS information. | II |
| Revision 6<br>(December 2000) | In the "PG176" package, pin A3 was incorrectly assigned as CLKA, I/O. A3 is a user I/O. Pin A9 is CLKA, I/O. | 3-21 |