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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	451
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	72
Number of Gates	2500
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1225a-pl84c

Ordering Information

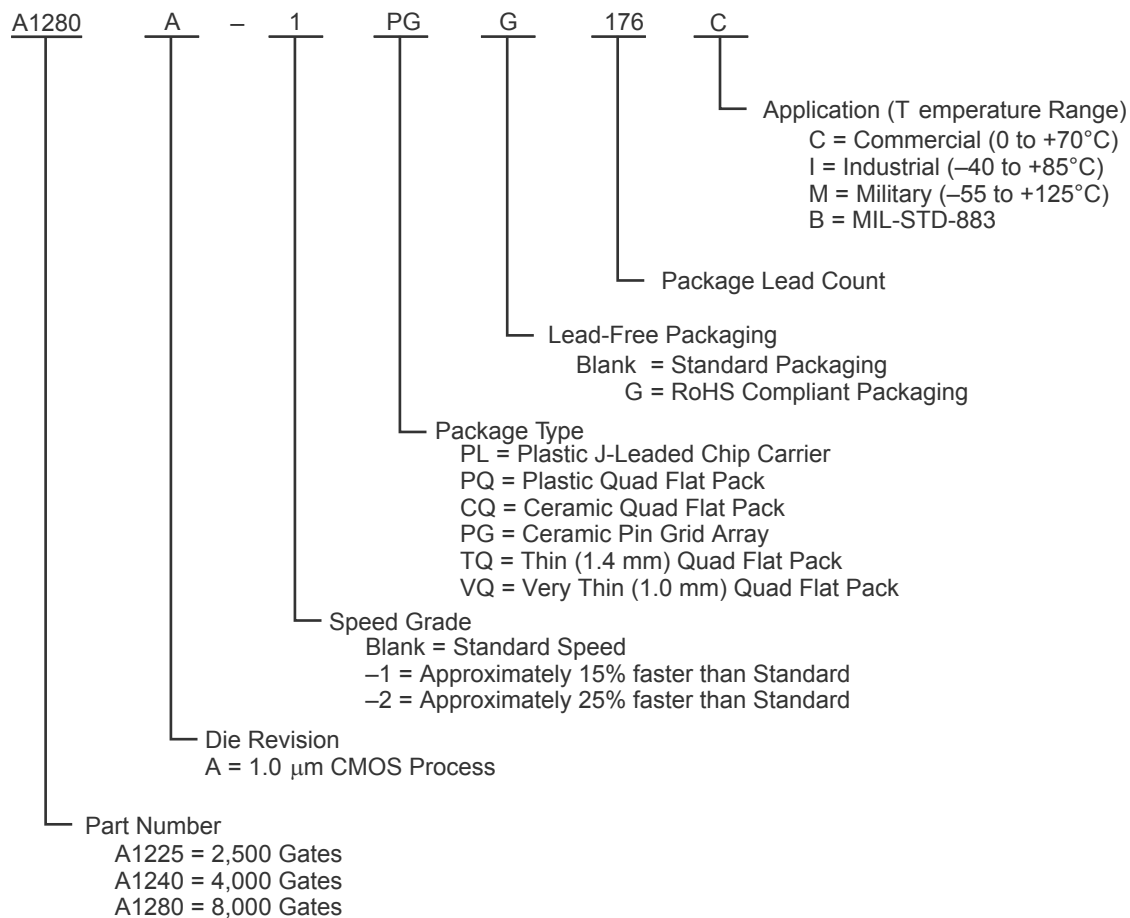


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To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. EQ 4 shows a piece-wise linear summation over all components.

$$\begin{aligned}
 \text{Power} = & VCC^2 * [(m * C_{EQM} * f_m)_{\text{modules}} + (n * C_{EQI} * f_n)_{\text{inputs}} \\
 & + (p * (C_{EQO} + C_L) * f_p)_{\text{outputs}} \\
 & + 0.5 * (q1 * C_{EQCR} * f_{q1})_{\text{routed_Clk1}} + (r1 * f_{q1})_{\text{routed_Clk1}} \\
 & + 0.5 * (q2 * C_{EQCR} * f_{q2})_{\text{routed_Clk2}} + (r2 * f_{q2})_{\text{routed_Clk2}}
 \end{aligned}$$

EQ 4

Where:

m = Number of logic modules switching at f_m

n = Number of input buffers switching at f_n

p = Number of output buffers switching at f_p

q1 = Number of clock loads on the first routed array clock

q2 = Number of clock loads on the second routed array clock

r_1 = Fixed capacitance due to first routed array clock

r_2 = Fixed capacitance due to second routed array clock

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_L = Output lead capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz

f_{q2} = Average second routed array clock rate in MHz

Table 2-7 • Fixed Capacitance Values for Microsemi FPGAs

Device Type	r1, routed_Clk1	r2, routed_Clk2
A1225A	106	106.0
A1240A	134	134.2
A1280A	168	167.8

Parameter Measurement

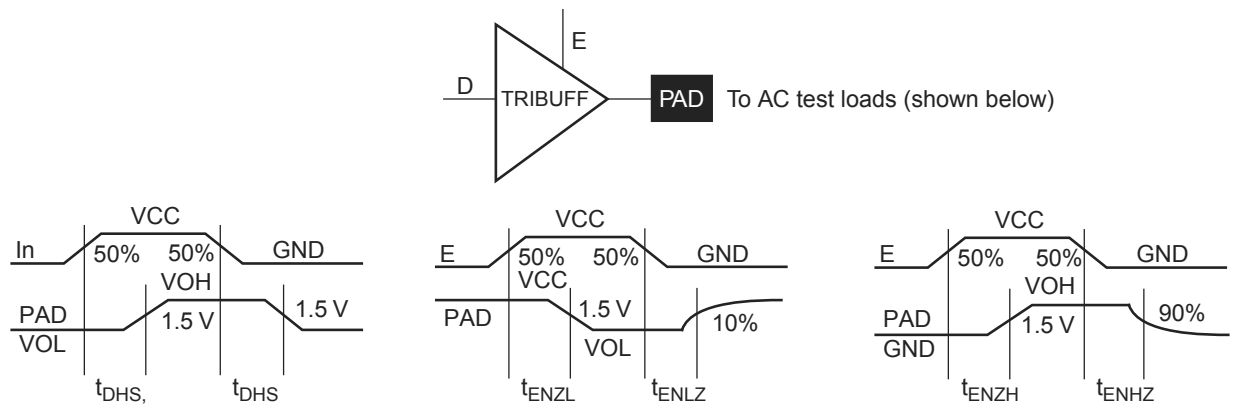


Figure 2-2 • Output Buffer Delays

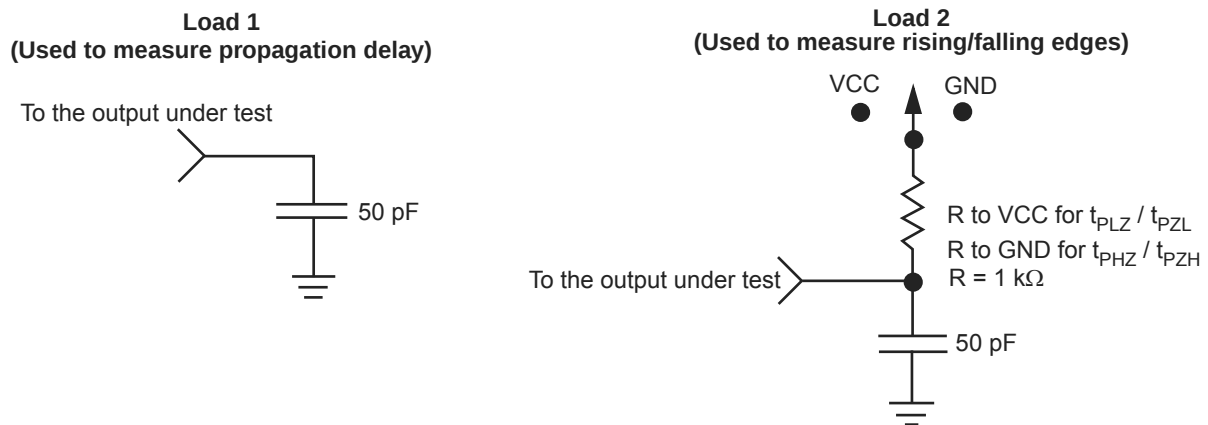


Figure 2-3 • AC Test Loads

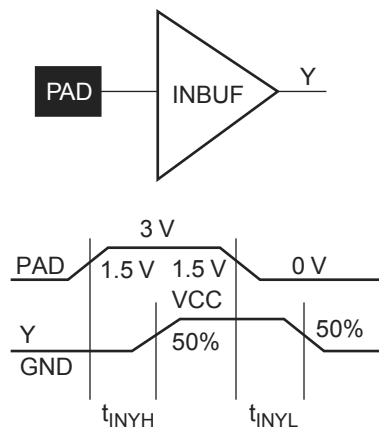


Figure 2-4 • Input Buffer Delays

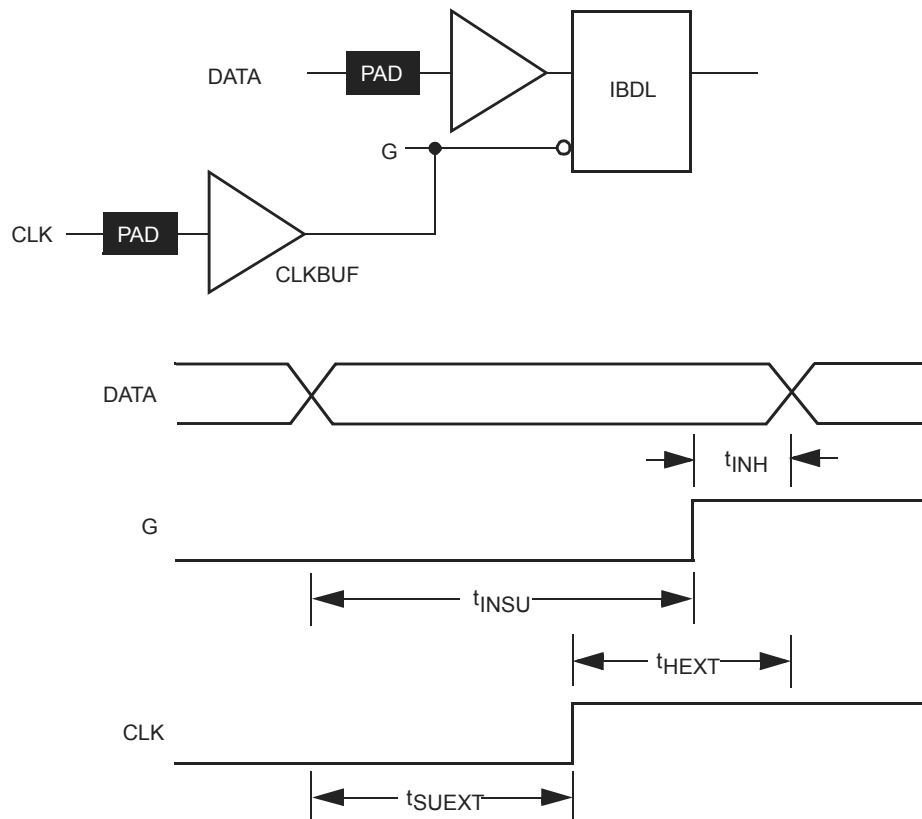


Figure 2-7 • Input Buffer Latches

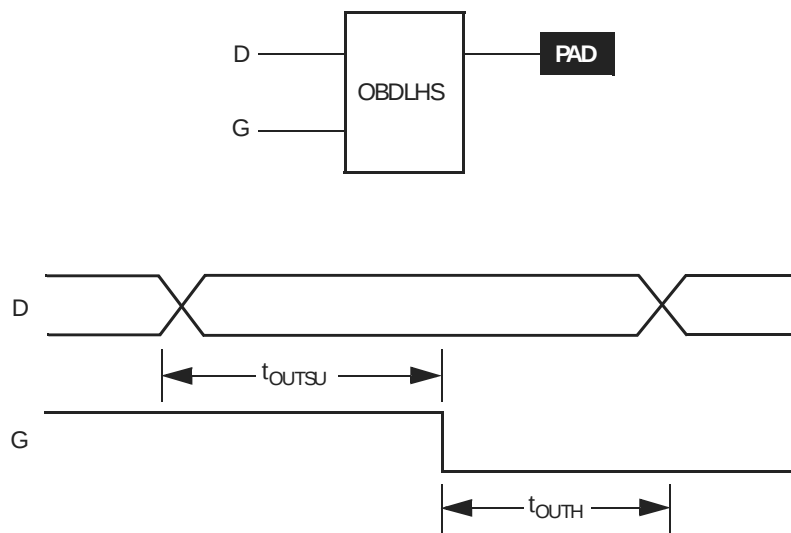


Figure 2-8 • Output Buffer Latches

A1225A Timing Characteristics

Table 2-12 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

Logic Module Propagation Delays ¹		–2 Speed ³		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD1}	Single Module		3.8		4.3		5.0	ns
t _{CO}	Sequential Clock to Q		3.8		4.3		5.0	ns
t _{GO}	Latch G to Q		3.8		4.3		5.0	ns
t _{RS}	Flip-Flop (Latch) Reset to Q		3.8		4.3		5.0	ns
Predicted Routing Delays²								
t _{RD1}	FO = 1 Routing Delay		1.1		1.2		1.4	ns
t _{RD2}	FO = 2 Routing Delay		1.7		1.9		2.2	ns
t _{RD3}	FO = 3 Routing Delay		2.3		2.6		3.0	ns
t _{RD4}	FO = 4 Routing Delay		2.8		3.1		3.7	ns
t _{RD8}	FO = 8 Routing Delay		4.4		4.9		5.8	ns
Sequential Timing Characteristics^{3,4}								
t _{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		ns
t _{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t _{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.5		5.0		6.0		ns
t _{WASYN}	Flip-Flop (Latch) Clock Asynchronous Pulse Width	4.5		5.0		6.0		ns
t _A	Flip-Flop Clock Input Period	9.4		11.0		13.0		ns
t _{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t _{INSU}	Input Buffer Latch Setup	0.4		0.4		0.5		ns
t _{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t _{OUTSU}	Output Buffer Latch Setup	0.4		0.4		0.5		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency		105.0		90.0		75.0	MHz

Notes:

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}—whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
4. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1225A Timing Characteristics (continued)

Table 2-14 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

TTL Output Module Timing ¹		-2 Speed		-1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t _{DLH}	Data to Pad High		8.0		9.0		10.6	ns
t _{DHL}	Data to Pad Low		10.1		11.4		13.4	ns
t _{ENZH}	Enable Pad Z to High		8.9		10.0		11.8	ns
t _{ENZL}	Enable Pad Z to Low		11.6		13.2		15.5	ns
t _{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t _{ENLZ}	Enable Pad Low to Z		8.3		9.5		11.1	ns
t _{GLH}	G to Pad High		8.9		10.2		11.9	ns
t _{GHL}	G to Pad Low		11.2		12.7		14.9	ns
d _{TLH}	Delta Low to High		0.07		0.08		0.09	ns/pF
d _{THL}	Delta High to Low		0.12		0.13		0.16	ns/pF
CMOS Output Module Timing ¹								
t _{DLH}	Data to Pad High		10.1		11.5		13.5	ns
t _{DHL}	Data to Pad Low		8.4		9.6		11.2	ns
t _{ENZH}	Enable Pad Z to High		8.9		10.0		11.8	ns
t _{ENZL}	Enable Pad Z to Low		11.6		13.2		15.5	ns
t _{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t _{ENLZ}	Enable Pad Low to Z		8.3		9.5		11.1	ns
t _{GLH}	G to Pad High		8.9		10.2		11.9	ns
t _{GHL}	G to Pad Low		11.2		12.7		14.9	ns
d _{TLH}	Delta Low to High		0.12		0.13		0.16	ns/pF
d _{THL}	Delta High to Low		0.09		0.10		0.12	ns/pF

Notes:

1. Delays based on 50 pF loading.
2. SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.

A1240A Timing Characteristics

Table 2-15 • A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

Logic Module Propagation Delays ¹		–2 Speed ³		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD1}	Single Module		3.8		4.3		5.0	ns
t _{CO}	Sequential Clock to Q		3.8		4.3		5.0	ns
t _{GO}	Latch G to Q		3.8		4.3		5.0	ns
t _{RS}	Flip-Flop (Latch) Reset to Q		3.8		4.3		5.0	ns
Predicted Routing Delays²								
t _{RD1}	FO = 1 Routing Delay		1.4		1.5		1.8	ns
t _{RD2}	FO = 2 Routing Delay		1.7		2.0		2.3	ns
t _{RD3}	FO = 3 Routing Delay		2.3		2.6		3.0	ns
t _{RD4}	FO = 4 Routing Delay		3.1		3.5		4.1	ns
t _{RD8}	FO = 8 Routing Delay		4.7		5.4		6.3	ns
Sequential Timing Characteristics^{3,4}								
t _{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		ns
t _{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t _{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.5		6.0		6.5		ns
t _{WASYN}	Flip-Flop (Latch) Clock Asynchronous Pulse Width	4.5		6.0		6.5		ns
t _A	Flip-Flop Clock Input Period	9.8		12.0		15.0		ns
t _{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t _{INSU}	Input Buffer Latch Setup	0.4		0.4		0.5		ns
t _{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t _{OUTSU}	Output Buffer Latch Setup	0.4		0.4		0.5		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency		100.0		80.0		66.0	MHz

Notes:

- For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}—whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
- Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1240A Timing Characteristics (continued)

Table 2-16 • A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module Input Propagation Delays			–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description			Min.	Max.	Min.	Max.	Min.	Max.	
t _{INYH}	Pad to Y High			2.9		3.3		3.8	ns
t _{INYL}	Pad to Y Low			2.6		3.0		3.5	ns
t _{INGH}	G to Y High			5.0		5.7		6.6	ns
t _{INGL}	G to Y Low			4.7		5.4		6.3	ns
Input Module Predicted Input Routing Delays*									
t _{IRD1}	FO = 1 Routing Delay			4.2		4.8		5.6	ns
t _{IRD2}	FO = 2 Routing Delay			4.8		5.4		6.4	ns
t _{IRD3}	FO = 3 Routing Delay			5.4		6.1		7.2	ns
t _{IRD4}	FO = 4 Routing Delay			5.9		6.7		7.9	ns
t _{IRD8}	FO = 8 Routing Delay			7.9		8.9		10.5	ns
Global Clock Network									
t _{CKH}	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		11.8		13.0		15.7	
t _{CKL}	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		12.0		13.2		15.9	
t _{PWH}	Minimum Pulse Width High	FO = 32	3.8		4.5		5.5		ns
		FO = 256	4.1		5.0		5.8		
t _{PWL}	Minimum Pulse Width Low	FO = 32	3.8		4.5		5.5		ns
		FO = 256	4.1		5.0		5.8		
t _{CKSW}	Maximum Skew	FO = 32		0.5		0.5		0.5	ns
		FO = 256		2.5		2.5		2.5	
t _{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t _{HEXT}	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t _P	Minimum Period	FO = 32	8.1		9.1		11.1		ns
		FO = 256	8.8		10.0		11.7		
f _{MAX}	Maximum Frequency	FO = 32		125.0		110.0		90.0	ns
		FO = 256		115.0		100.0		85.0	

*Note: *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1240A Timing Characteristics (continued)

Table 2-17 • A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

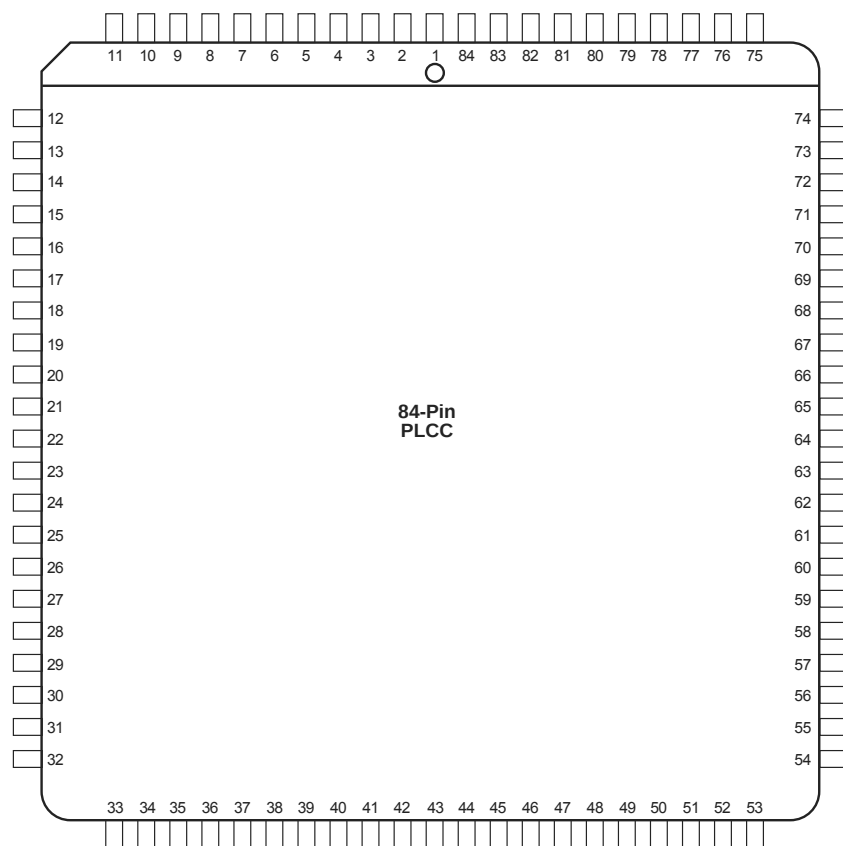
TTL Output Module Timing ¹		-2 Speed		-1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t _{DLH}	Data to Pad High		8.0		9.0		10.6	ns
t _{DHL}	Data to Pad Low		10.1		11.4		13.4	ns
t _{ENZH}	Enable Pad Z to High		8.9		10.0		11.8	ns
t _{ENZL}	Enable Pad Z to Low		11.7		13.2		15.5	ns
t _{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t _{ENLZ}	Enable Pad Low to Z		8.4		9.5		11.1	ns
t _{GLH}	G to Pad High		9.0		10.2		11.9	ns
t _{GHL}	G to Pad Low		11.2		12.7		14.9	ns
d _{TLH}	Delta Low to High		0.07		0.08		0.09	ns/pF
d _{THL}	Delta High to Low		0.12		0.13		0.16	ns/pF
CMOS Output Module Timing ¹								
t _{DLH}	Data to Pad High		10.2		11.5		13.5	ns
t _{DHL}	Data to Pad Low		8.4		9.6		11.2	ns
t _{ENZH}	Enable Pad Z to High		8.9		10.0		11.8	ns
t _{ENZL}	Enable Pad Z to Low		11.7		13.2		15.5	ns
t _{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t _{ENLZ}	Enable Pad Low to Z		8.4		9.5		11.1	ns
t _{GLH}	G to Pad High		9.0		10.2		11.9	ns
t _{GHL}	G to Pad Low		11.2		12.7		14.9	ns
d _{TLH}	Delta Low to High		0.12		0.13		0.16	ns/pF
d _{THL}	Delta High to Low		0.09		0.10		0.12	ns/pF

Notes:

1. Delays based on 50 pF loading.
2. SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.

3 – Package Pin Assignments

PL84



Note

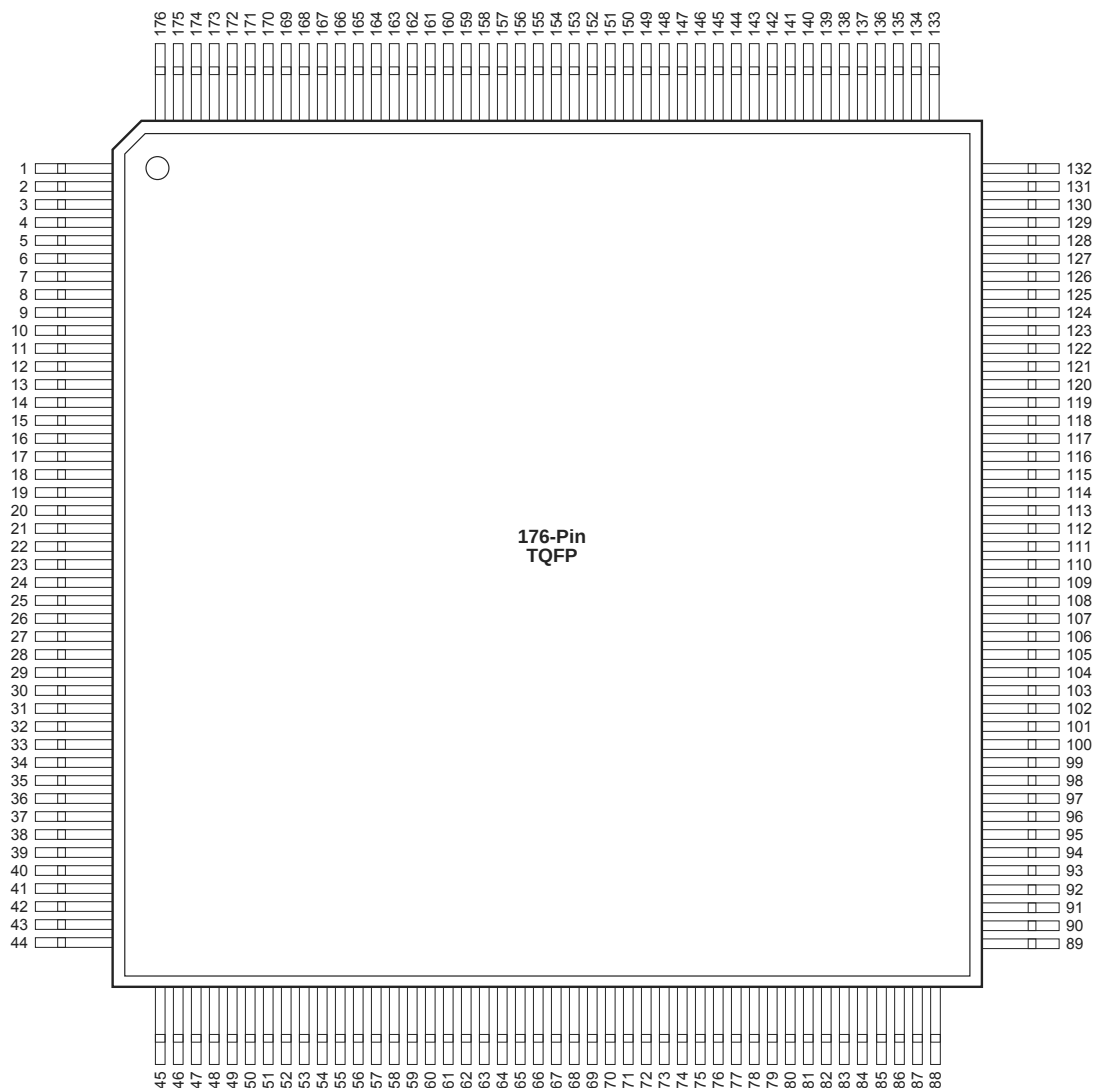
For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

PQ160		PQ160	
Pin Number	A1280A Function	Pin Number	A1280A Function
2	DCLK, I/O	69	GND
6	VCC	80	GND
11	GND	82	SDO
16	PRB, I/O	86	VCC
18	CLKB, I/O	89	GN
20	VCC	98	GND
21	CLKA, I/O	99	GND
23	PRA, I/O	109	GND
30	GND	114	VCC
35	VCC	120	GND
38	SDI, I/O	125	GND
40	GND	130	GND
44	GND	135	VCC
49	GND	138	VCC
54	VCC	139	VCC
57	VCC	140	GND
58	VCC	145	GND
59	GND	150	VCC
60	VCC	155	GND
61	GND	159	MODE
64	GND	160	GND

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

TQ176



Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

TQ176		
Pin Number	A1240A Function	A1280A Function
1	GND	GND
2	MODE	MODE
8	NC	NC
10	NC	I/O
11	NC	I/O
13	NC	VCC
18	GND	GND
19	NC	I/O
20	NC	I/O
22	NC	I/O
23	GND	GND
24	NC	VCC
25	VCC	VCC
26	NC	I/O
27	NC	I/O
28	VCC	VCC
29	NC	I/O
33	NC	NC
37	NC	I/O
38	NC	NC
45	GND	GND
52	NC	VCC
54	NC	I/O
55	NC	I/O
57	NC	NC
61	NC	I/O
64	NC	I/O
66	NC	I/O
67	GND	GND
68	VCC	VCC
74	NC	I/O
77	NC	NC
78	NC	I/O
80	NC	I/O

TQ176		
Pin Number	A1240A Function	A1280A Function
82	NC	VCC
86	NC	I/O
87	SDO	SDO
89	GND	GND
96	NC	I/O
97	NC	I/O
101	NC	NC
103	NC	I/O
106	GND	GND
107	NC	I/O
108	NC	I/O
109	GND	GND
110	VCC	VCC
111	GND	GND
112	VCC	VCC
113	VCC	VCC
114	NC	I/O
115	NC	I/O
116	NC	VCC
121	NC	NC
124	NC	I/O
125	NC	I/O
126	NC	NC
133	GND	GND
135	SDI, I/O	SDI, I/O
136	NC	I/O
140	NC	VCC
143	NC	I/O
144	NC	I/O
145	NC	NC
147	NC	I/O
151	NC	I/O
152	PRA, I/O	PRA, I/O
154	CLKA, I/O	CLKA, I/O

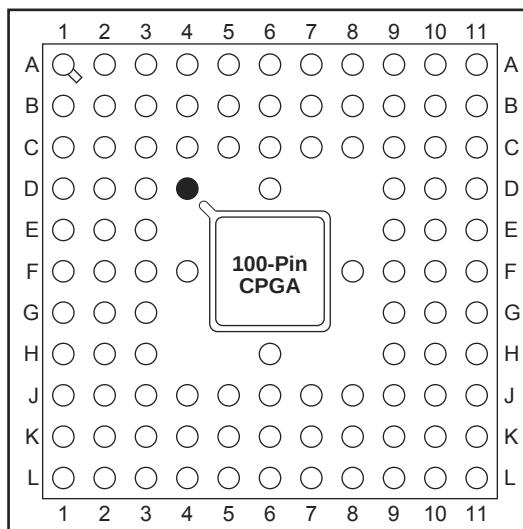
CQ172	
Pin Number	A1280A Function
1	MODE
7	GND
12	VCC
17	GND
22	GND
23	VCC
24	VCC
27	VCC
32	GND
37	GND
50	VCC
55	GND
65	GND
66	VCC
75	GND
80	VCC
85	SDO
98	GND
103	GND
106	GND

CQ172	
Pin Number	A1280A Function
107	VCC
108	GND
109	VCC
110	VCC
113	VCC
118	GND
123	GND
131	SDI, I/O
136	VCC
141	GND
148	PRA, I/O
150	CLKA, I/O
151	VCC
152	GND
154	CLKB, I/O
156	PRB, I/O
161	GND
166	VCC
171	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG100

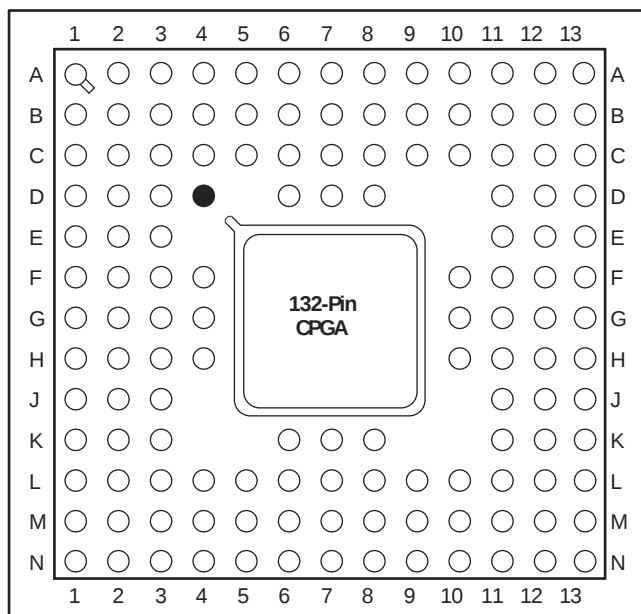


● Orientation Pin

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

PG132



● Orientation Pin

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>



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