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Details

Details	
Product Status	Obsolete
Number of LABs/CLBs	451
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	72
Number of Gates	2500
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1225a-pl84i

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ACT 2 Family FPGAs

Ordering Information



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Operating Conditions

Table 2-1 • Absolute Maximum Ratings¹

Symbol	Parameter	Limits	Units
VCC	DC supply voltage	–0.5 to +7.0	V
VI	Input voltage	-0.5 to VCC + 0.5	V
VO	Output voltage	-0.5 to VCC + 0.5	V
IIO	I/O source sink current ²	±20	mA
T _{STG}	Storage temperature	–65 to +150	°C

Notes:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.

2. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND –0.5 V, the internal protection diodes will be forward biased and can draw excessive current.

Table 2-2 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature range*	0 to +70	-40 to +85	-55 to +125	°C
Power supply tolerance	±5	±10	±10	%VCC

Note: *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.



Table 2-3 • Electrical Specifications

		Commercial		In	dustrial	Μ		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units
VOH ¹	$(IOH = -10 \text{ mA})^2$	2.4	-	-	-	-	-	V
	(IOH = –6 mA)	3.84	-	-	-	-	-	V
	(IOH = -4 mA)	-	-	3.7	-	3.7	-	V
VOL ¹	$(IOL = 10 \text{ mA})^2$	-	0.5	-	-	-	-	V
	(IOL = 6 mA)	-	0.33	-	0.40	-	0.40	V
VIL		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
VIH		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
Input Trans	ition Time t _R , t _F ²	-	500	-	500	-	500	ns
C _{IO} I/O cap	acitance ^{2,3}	-	10	-	10	-	10	pF
Standby Current, ICC ⁴ (typical = 1 mA)		-	2	-	- 10		20	mA
Leakage Current ⁵		-10	+10	-10	+10	-10	+10	μA
ICC(D) Dynamic VCC supply current. See the Power Dissipation section.								

Notes:

1. Only one output tested at a time. VCC = minimum.

2. Not tested, for information only.

3. Includes worst-case PG176 package capacitance. VOUT = 0 V, f = 1 MHz

4. All outputs unloaded. All inputs = VCC or GND, typical ICC = 1 mA. ICC limit includes IPP and ISV during normal operations.

5. VOUT, VIN = VCC or GND.

Package Thermal Characteristics

The device junction to case thermal characteristic is θ jc, and the junction to ambient air characteristic is θ ja. The thermal characteristics for θ ja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a PQ160 package at commercial temperature and still air is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja} °C/W} = \frac{150°C - 70°C}{33°C/W} = 2.4 \text{ W}$$

EQ 1

Package Type∗	Pin Count	θ _{jc}	θ _{ja} Still Air	^θ ja 300 ft./min.	Units
Ceramic Pin Grid Array	100	5	35	17	°C/W
	132	5	30	15	°C/W
	176	8	23	12	°C/W
Ceramic Quad Flatpack	172	8	25	15	°C/W
Plastic Quad Flatpack ¹	100	13	48	40	°C/W
	144	15	40	32	°C/W
	160	15	38	30	°C/W
Plastic Leaded Chip Carrier	84	12	37	28	°C/W
Very Thin Quad Flatpack	100	12	43	35	°C/W
Thin Quad Flatpack	176	15	32	25	°C/W

Table 2-4 • Package Thermal Characteristics

Notes: (Maximum Power in Still Air)

1. Maximum power dissipation values for PQFP packages are 1.9 W (PQ100), 2.3 W (PQ144), and 2.4 W (PQ160).

2. Maximum power dissipation for PLCC packages is 2.7 W.

3. Maximum power dissipation for VQFP packages is 2.3 W.

4. Maximum power dissipation for TQFP packages is 3.1 W.

Power Dissipation

P = [ICC standby + ICCactive] * VCC + IOL * VOL * N + IOH* (VCC – VOH) * M

EQ 2

where:

ICC standby is the current flowing when no inputs or outputs are changing

ICCactive is the current flowing due to CMOS switching.

IOL and IOH are TTL sink/source currents.

VOL and VOH are TTL level output voltages.

N is the number of outputs driving TTL loads to VOL.

M is the number of outputs driving TTL loads to VOH.

An accurate determination of N and M is problematical because their values depend on the family type, design details, and on the system I/O. The power can be divided into two components: static and active.



Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are given in Table 2-8.

Table 2-8 •	Guidelines	for Predicting	Power	Dissipation
	ouraonnoo	lot i roaloung		Diooipation

Data	Value
Logic Modules (m)	80% of modules
Inputs switching (n)	# inputs/4
Outputs switching (p)	# output/4
First routed array clock loads (q1)	40% of sequential modules
Second routed array clock loads (q2)	40% of sequential modules
Load capacitance (C _L)	35 pF
Average logic module switching rate (f _m)	F/10
Average input switching rate (f _n)	F/5
Average output switching rate (f _p)	F/10
Average first routed array clock rate (fq1)	F
Average second routed array clock rate (fq2)	F/2



Parameter Measurement



Figure 2-2 • Output Buffer Delays



Figure 2-3 • AC Test Loads



Figure 2-4 • Input Buffer Delays



A1225A Timing Characteristics

Table 2-12 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

Logic Mo	Logic Module Propagation Delays ¹		–2 Speed ³		-1 Speed		Std. Speed	
Paramete	er/Description	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD1}	Single Module		3.8		4.3		5.0	ns
t _{CO}	Sequential Clock to Q		3.8		4.3		5.0	ns
t _{GO}	Latch G to Q		3.8		4.3		5.0	ns
t _{RS}	Flip-Flop (Latch) Reset to Q		3.8		4.3		5.0	ns
Predicted	Routing Delays ²							•
t _{RD1}	FO = 1 Routing Delay		1.1		1.2		1.4	ns
t _{RD2}	FO = 2 Routing Delay		1.7		1.9		2.2	ns
t _{RD3}	FO = 3 Routing Delay		2.3		2.6		3.0	ns
t _{RD4} FO = 4 Routing Delay			2.8		3.1		3.7	ns
t _{RD8}	FO = 8 Routing Delay		4.4		4.9		5.8	ns
Sequenti	al Timing Characteristics ^{3,4}				-		-	
t _{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		ns
t _{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t _{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.5		5.0		6.0		ns
t _{WASYN}	Flip-Flop (Latch) Clock Asynchronous Pulse Width	4.5		5.0		6.0		ns
t _A	Flip-Flop Clock Input Period	9.4		11.0		13.0		ns
t _{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t _{INSU}	Input Buffer Latch Setup	0.4		0.4		0.5		ns
t _{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t _{OUTSU}	Output Buffer Latch Setup	0.4		0.4		0.5		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency		105.0		90.0		75.0	MHz

Notes:

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$ —whichever is appropriate.

 Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.

4. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1280A Timing Characteristics (continued)

Table 2-19 • A1280A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module Input Propagation Delays			-2 S	-2 Speed		-1 Speed		Std. Speed	
Paramete	er/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t _{INYH}	Pad to Y High			2.9		3.3		3.8	ns
t _{INYL}	Pad to Y Low			2.7		3.0		3.5	ns
t _{INGH}	G to Y High			5.0		5.7		6.6	ns
t _{INGL}	G to Y Low			4.8		5.4		6.3	ns
Input Mo	dule Predicted Input Routing Del	ays [*]	•				•		
t _{IRD1}	FO = 1 Routing Delay			4.6		5.1		6.0	ns
t _{IRD2}	FO = 2 Routing Delay			5.2		5.9		6.9	ns
t _{IRD3}	FO = 3 Routing Delay			5.6		6.3		7.4	ns
t _{IRD4}	FO = 4 Routing Delay			6.5		7.3		8.6	ns
t _{IRD8}	FO = 8 Routing Delay			9.4		10.5		12.4	ns
Global C	lock Network				-	-	-	-	
t _{CKH}	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		13.1		14.6		17.2	
t _{CKL}	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		13.3		14.9		17.5	
t _{PWH}	Minimum Pulse Width High	FO = 32	5.0		5.5		6.6		ns
		FO = 256	5.8		6.4		7.6		
t _{PWL}	Minimum Pulse Width Low	FO = 32	5.0		5.5		6.6		ns
		FO = 256	5.8		6.4		7.6		
t _{CKSW}	Maximum Skew	FO = 32		0.5		0.5		0.5	ns
		FO = 256		2.5		2.5		2.5	
t _{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t _{HEXT}	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t _P	Minimum Period	FO = 32	9.6		11.2		13.3		ns
		FO = 256	10.6		12.6		15.3		
f _{MAX}	Maximum Frequency	FO = 32		105.0		90.0		75.0	ns
		FO = 256		95.0		80.0		65.0	

Note: *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1280A Timing Characteristics (continued)

Pin Descriptions

CLKA Clock A (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB Clock B (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

GND Ground

Low supply voltage.

I/O Input/Output (Input, Output)

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven Low by the ALS software.

MODE Mode (Input)

The MODE pin controls the use of multifunction pins (DCLK, PRA, PRB, SDI). When the MODE pin is High, the special functions are active. When the MODE pin is Low, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled High when required.

NC No Connection

This pin is not connected to circuitry within the device.

PRA Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

PRB Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

SDO Serial Data Output (Output)

Serial data output for diagnostic probe. SDO is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

VCC 5.0 V Supply Voltage

High supply voltage.



PL84			
Pin Number	A1225A Function	A1240A Function	A1280A Function
2	CLKB, I/O	CLKB, I/O	CLKB, I/O
4	PRB, I/O	PRB, I/O	PRB, I/O
6	GND	GND	GND
10	DCLK, I/O	DCLK, I/O	DCLK, I/O
12	MODE	MODE	MODE
22	VCC	VCC	VCC
23	VCC	VCC	VCC
28	GND	GND	GND
43	VCC	VCC	VCC
49	GND	GND	GND
52	SDO	SDO	SDO
63	GND	GND	GND
64	VCC	VCC	VCC
65	VCC	VCC	VCC
70	GND	GND	GND
76	SDI, I/O	SDI, I/O	SDI, I/O
81	PRA, I/O	PRA, I/O	PRA, I/O
83	CLKA, I/O	CLKA, I/O	CLKA, I/O
84	VCC	VCC	VCC

Notes:

1. All unlisted pin numbers are user I/Os.

2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.



PQ100		PQ100	
Pin Number	A1225A Function	Pin Number	A1225A Function
2	DCLK, I/O	65	VCC
4	MODE	66	VCC
9	GND	67	VCC
16	VCC	72	GND
17	VCC	79	SDI, I/O
22	GND	84	GND
34	GND	87	PRA, I/O
40	VCC	89	CLKA, I/O
46	GND	90	VCC
52	SDO	92	CLKB, I/O
57	GND	94	PRB, I/O
64	GND	96	GND

Notes:

- 1. All unlisted pin numbers are user I/Os.
- 2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.



	PQ160		PQ160
Pin Number	A1280A Function	Pin Number	A1280A Function
2	DCLK, I/O	69	GND
6	VCC	80	GND
11	GND	82	SDO
16	PRB, I/O	86	VCC
18	CLKB, I/O	89	GN
20	VCC	98	GND
21	CLKA, I/O	99	GND
23	PRA, I/O	109	GND
30	GND	114	VCC
35	VCC	120	GND
38	SDI, I/O	125	GND
40	GND	130	GND
44	GND	135	VCC
49	GND	138	VCC
54	VCC	139	VCC
57	VCC	140	GND
58	VCC	145	GND
59	GND	150	VCC
60	VCC	155	GND
61	GND	159	MODE
64	GND	160	GND

Notes:

- 1. All unlisted pin numbers are user I/Os.
- 2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.



TQ176			
Pin Number	A1240A Function	A1280A Function	
155	VCC	VCC	
156	GND	GND	
158	CLKB, I/O	CLKB, I/O	
160	PRB, I/O	PRB, I/O	
161	NC	I/O	
165	NC	NC	
166	NC	I/O	
168	NC	I/O	
170	NC	VCC	
173	NC	I/O	
175	DCLK, I/O	DCLK, I/O	

Notes:

- 1. NC denotes no connection.
- 2. All unlisted pin numbers are user I/Os.
- 3. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.



CQ172



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

CQ172			CQ172	
Pin Number	A1280A Function	Pin Number	A1280A Function	
1	MODE	107	VCC	
7	GND	108	GND	
12	VCC	109	VCC	
17	GND	110	VCC	
22	GND	113	VCC	
23	VCC	118	GND	
24	VCC	123	GND	
27	VCC	131	SDI, I/O	
32	GND	136	VCC	
37	GND	141	GND	
50	VCC	148	PRA, I/O	
55	GND	150	CLKA, I/O	
65	GND	151	VCC	
66	VCC	152	GND	
75	GND	154	CLKB, I/O	
80	VCC	156	PRB, I/O	
85	SDO	161	GND	
98	GND	166	VCC	
103	GND	171	DCLK, I/O	
106	GND			

Notes:

1. All unlisted pin numbers are user I/Os.

2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.



PG100



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx



PG132



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

4 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each version of the datasheet.

Revision	Changes	Page
Revision 8 (January 2012)	The ACT 2 datasheet was formatted newly in the style used for current datasheets. The same information is present (other than noted in the list of changes for this revision) but divided into chapters.	N/A
	Package names used in Table 1 • ACT 2 Product Family Profile and throughout the document were revised to match standards given in <i>Package Mechanical Drawings</i> (SAR 27395).	
	The description for SDO pins had earlier been removed from the datasheet and has now been included again, in the "Pin Descriptions" section (SAR 35819).	2-21
	SDO pin numbers had earlier been removed from package pin assignment tables in the datasheet, and have now been restored to the pin tables (SAR 35819).	3-2
Revision 7 (June 2006)	The "Ordering Information" section was revised to include RoHS information.	Π
Revision 6 (December 2000)	In the "PG176" package, pin A3 was incorrectly assigned as CLKA, I/O. A3 is a user I/O. Pin A9 is CLKA, I/O.	3-21



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