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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	451
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	83
Number of Gates	2500
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1225a-pqg100i

Product Plan

Device/Package	Speed Grade[1]			Application[1]			
	Std.	−1	−2	C	I	M	B
A1225A Device							
84-Pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–
100-Pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	✓	–	–
100-Pin Very Thin Quad Flatpack (VQ)	✓	✓	✓	✓	–	–	–
100-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	–	–	–
A1240A Device							
84-Pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–
132-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	–	✓	✓
144-Pin Plastic Quad Flat Pack (PQ)	✓	✓	✓	✓	✓	–	–
176-Pin Thin (1.4 mm) Quad Flat Pack (TQ)	✓	✓	✓	✓	–	–	–
A1280A Device							
160-Pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	✓	–	–
172-Pin Ceramic Quad Flatpack (CQ)	✓	✓	✓	✓	–	✓	✓
176-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	–	✓	✓
176-Pin Thin (1.4 mm) Quad Flat Pack (TQ)	✓	✓	✓	✓	–	–	–

Notes:

1. *Applications:*
   C = Commercial
   I = Industrial
   M = Military
   B = MIL-STD-883

Availability:
✓ = Available
P = Planned
– = Not planned

Speed Grade:
−1 = Approx. 15% faster than Std.
−2 = Approx. 25% faster than Std.

2. *Contact your Microsemi SoC Products Group sales representative for product availability.*

Device Resources

Device Series	Logic Modules	Gates	User I/Os									
			PG176	PG132	PG100	PQ160	PQ144	PQ100	PL84	CQ172	TQ176	VQ100
A1225A	451	2,500	–	–	83	–	–	83	72	–	–	83
A1240A	684	4,000	–	104	–	–	104	–	72	–	104	–
A1280A	1,232	8,000	140	–	–	125	–	–	72	140	140	–

Contact your local Microsemi SoC Products Group representative for device availability:

http://www.microsemi.com/soc/contact/default.aspx.

2 – Detailed Specifications

Operating Conditions

Table 2-1 • **Absolute Maximum Ratings**[1]

Symbol	Parameter	Limits	Units
VCC	DC supply voltage	–0.5 to +7.0	V
VI	Input voltage	–0.5 to VCC + 0.5	V
VO	Output voltage	–0.5 to VCC + 0.5	V
IIO	I/O source sink current[2]	±20	mA
T_{STG}	Storage temperature	–65 to +150	°C

Notes:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.
2. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND –0.5 V, the internal protection diodes will be forward biased and can draw excessive current.

Table 2-2 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature range*	0 to +70	–40 to +85	–55 to +125	°C
Power supply tolerance	±5	±10	±10	%VCC

Note: *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.

Table 2-3 • **Electrical Specifications**

Symbol	Parameter	Commercial		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
VOH[1]	(IOH = –10 mA)[2]	2.4	–	–	–	–	–	V
	(IOH = –6 mA)	3.84	–	–	–	–	–	V
	(IOH = –4 mA)	–	–	3.7	–	3.7	–	V
VOL[1]	(IOL = 10 mA)[2]	–	0.5	–	–	–	–	V
	(IOL = 6 mA)	–	0.33	–	0.40	–	0.40	V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
Input Transition Time t_R, t_F[2]		–	500	–	500	–	500	ns
C_{IO} I/O capacitance[2,3]		–	10	–	10	–	10	pF
Standby Current, ICC[4] (typical = 1 mA)		–	2	–	10	–	20	mA
Leakage Current[5]		–10	+10	–10	+10	–10	+10	µA
ICC(D)	Dynamic VCC supply current. See the Power Dissipation section.							

Notes:

1. *Only one output tested at a time. VCC = minimum.*
2. *Not tested, for information only.*
3. *Includes worst-case PG176 package capacitance. VOUT = 0 V, f = 1 MHz*
4. *All outputs unloaded. All inputs = VCC or GND, typical ICC = 1 mA. ICC limit includes IPP and ISV during normal operations.*
5. *VOUT, VIN = VCC or GND.*

Static Power Component

Microsemi FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated in Table 2-5 for commercial, worst case conditions.

Table 2-5 • **Standby Power Calculation**

ICC	VCC	Power
2 mA	5.25 V	10.5 mW

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs.

An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by EQ 3.

$$\text{Power } (\mu W) = C_{EQ} * VCC^2 * F$$

EQ 3

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

VCC is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring ICC active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown in Table 2-6.

Table 2-6 • **CEQ Values for Microsemi FPGAs**

Item	CEQ Value
Modules (C_{EQM})	5.8
Input Buffers (C_{EQI})	12.9
Output Buffers (C_{EQO})	23.8
Routed Array Clock Buffer Loads (C_{EQCR})	3.9

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. EQ 4 shows a piece-wise linear summation over all components.

Power $= VCC^2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs}$

$+ (p * (C_{EQO} + C_L) * fp)_{outputs}$

$+ 0.5 * (q1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r1 * f_{q1})_{routed\_Clk1}$

$+ 0.5 * (q2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2}$

EQ 4

Where:

m = Number of logic modules switching at f_m

n = Number of input buffers switching at f_n

p = Number of output buffers switching at f_p

q1 = Number of clock loads on the first routed array clock

q2 = Number of clock loads on the second routed array clock

r_1 = Fixed capacitance due to first routed array clock

r_2 = Fixed capacitance due to second routed array clock

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_L = Output lead capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz

f_{q2} = Average second routed array clock rate in MHz

Table 2-7 • **Fixed Capacitance Values for Microsemi FPGAs**

Device Type	r1, routed_Clk1	r2, routed_Clk2
A1225A	106	106.0
A1240A	134	134.2
A1280A	168	167.8

A1225A Timing Characteristics

Table 2-12 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C

Logic Module Propagation Delays[1]		–2 Speed[3]		–1 Speed		Std. Speed		Units
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{PD1}	Single Module		3.8		4.3		5.0	ns
t_{CO}	Sequential Clock to Q		3.8		4.3		5.0	ns
t_{GO}	Latch G to Q		3.8		4.3		5.0	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		3.8		4.3		5.0	ns
Predicted Routing Delays[2]								
t_{RD1}	FO = 1 Routing Delay		1.1		1.2		1.4	ns
t_{RD2}	FO = 2 Routing Delay		1.7		1.9		2.2	ns
t_{RD3}	FO = 3 Routing Delay		2.3		2.6		3.0	ns
t_{RD4}	FO = 4 Routing Delay		2.8		3.1		3.7	ns
t_{RD8}	FO = 8 Routing Delay		4.4		4.9		5.8	ns
Sequential Timing Characteristics[3,4]								
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.5		5.0		6.0		ns
t_{WASYN}	Flip-Flop (Latch) Clock Asynchronous Pulse Width	4.5		5.0		6.0		ns
t_A	Flip-Flop Clock Input Period	9.4		11.0		13.0		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.4		0.4		0.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.4		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		105.0		90.0		75.0	MHz

Notes:

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$—whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
4. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1225A Timing Characteristics (continued)

Table 2-13 • **A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

I/O Module Input Propagation Delays		–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t$_{INYH}$	Pad to Y High		2.9		3.3		3.8	ns
t$_{INYL}$	Pad to Y Low		2.6		3.0		3.5	ns
t$_{INGH}$	G to Y High		5.0		5.7		6.6	ns
t$_{INGL}$	G to Y Low		4.7		5.4		6.3	ns
Input Module Predicted Input Routing Delays[*]								
t$_{IRD1}$	FO = 1 Routing Delay		4.1		4.6		5.4	ns
t$_{IRD2}$	FO = 2 Routing Delay		4.6		5.2		6.1	ns
t$_{IRD3}$	FO = 3 Routing Delay		5.3		6.0		7.1	ns
t$_{IRD4}$	FO = 4 Routing Delay		5.7		6.4		7.6	ns
t$_{IRD8}$	FO = 8 Routing Delay		7.4		8.3		9.8	ns
Global Clock Network								
t$_{CKH}$	Input Low to High	FO = 32	10.2		11.0		12.8	ns
		FO = 256	11.8		13.0		15.7	
t$_{CKL}$	Input High to Low	FO = 32	10.2		11.0		12.8	ns
		FO = 256	12.0		13.2		15.9	
t$_{PWH}$	Minimum Pulse Width High	FO = 32	3.4		4.1		4.5		ns
		FO = 256	3.8		4.5		5.0		
t$_{PWL}$	Minimum Pulse Width Low	FO = 32	3.4		4.1		4.5		ns
		FO = 256	3.8		4.5		5.0		
t$_{CKSW}$	Maximum Skew	FO = 32		0.7		0.7		0.7	ns
		FO = 256		3.5		3.5		3.5	
t$_{SUEXT}$	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t$_{HEXT}$	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t$_P$	Minimum Period	FO = 32	7.7		8.3		9.1		ns
		FO = 256	8.1		8.8		10.0		
f$_{MAX}$	Maximum Frequency	FO = 32		130.0		120.0		110.0	ns
		FO = 256		125.0		115.0		100.0	

*Note: *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1225A Timing Characteristics (continued)

Table 2-14 • **A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

TTL Output Module Timing[1]		–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t$_{DLH}$	Data to Pad High		8.0		9.0		10.6	ns
t$_{DHL}$	Data to Pad Low		10.1		11.4		13.4	ns
t$_{ENZH}$	Enable Pad Z to High		8.9		10.0		11.8	ns
t$_{ENZL}$	Enable Pad Z to Low		11.6		13.2		15.5	ns
t$_{ENHZ}$	Enable Pad High to Z		7.1		8.0		9.4	ns
t$_{ENLZ}$	Enable Pad Low to Z		8.3		9.5		11.1	ns
t$_{GLH}$	G to Pad High		8.9		10.2		11.9	ns
t$_{GHL}$	G to Pad Low		11.2		12.7		14.9	ns
d$_{TLH}$	Delta Low to High		0.07		0.08		0.09	ns/pF
d$_{THL}$	Delta High to Low		0.12		0.13		0.16	ns/pF
CMOS Output Module Timing[1]								
t$_{DLH}$	Data to Pad High		10.1		11.5		13.5	ns
t$_{DHL}$	Data to Pad Low		8.4		9.6		11.2	ns
t$_{ENZH}$	Enable Pad Z to High		8.9		10.0		11.8	ns
t$_{ENZL}$	Enable Pad Z to Low		11.6		13.2		15.5	ns
t$_{ENHZ}$	Enable Pad High to Z		7.1		8.0		9.4	ns
t$_{ENLZ}$	Enable Pad Low to Z		8.3		9.5		11.1	ns
t$_{GLH}$	G to Pad High		8.9		10.2		11.9	ns
t$_{GHL}$	G to Pad Low		11.2		12.7		14.9	ns
d$_{TLH}$	Delta Low to High		0.12		0.13		0.16	ns/pF
d$_{THL}$	Delta High to Low		0.09		0.10		0.12	ns/pF

Notes:

1. Delays based on 50 pF loading.

2. SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.

A1240A Timing Characteristics (continued)

Table 2-17 • A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C

TTL Output Module Timing[1]		−2 Speed		−1 Speed		Std. Speed		Units
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t$_{DLH}$	Data to Pad High		8.0		9.0		10.6	ns
t$_{DHL}$	Data to Pad Low		10.1		11.4		13.4	ns
t$_{ENZH}$	Enable Pad Z to High		8.9		10.0		11.8	ns
t$_{ENZL}$	Enable Pad Z to Low		11.7		13.2		15.5	ns
t$_{ENHZ}$	Enable Pad High to Z		7.1		8.0		9.4	ns
t$_{ENLZ}$	Enable Pad Low to Z		8.4		9.5		11.1	ns
t$_{GLH}$	G to Pad High		9.0		10.2		11.9	ns
t$_{GHL}$	G to Pad Low		11.2		12.7		14.9	ns
d$_{TLH}$	Delta Low to High		0.07		0.08		0.09	ns/pF
d$_{THL}$	Delta High to Low		0.12		0.13		0.16	ns/pF
CMOS Output Module Timing[1]								
t$_{DLH}$	Data to Pad High		10.2		11.5		13.5	ns
t$_{DHL}$	Data to Pad Low		8.4		9.6		11.2	ns
t$_{ENZH}$	Enable Pad Z to High		8.9		10.0		11.8	ns
t$_{ENZL}$	Enable Pad Z to Low		11.7		13.2		15.5	ns
t$_{ENHZ}$	Enable Pad High to Z		7.1		8.0		9.4	ns
t$_{ENLZ}$	Enable Pad Low to Z		8.4		9.5		11.1	ns
t$_{GLH}$	G to Pad High		9.0		10.2		11.9	ns
t$_{GHL}$	G to Pad Low		11.2		12.7		14.9	ns
d$_{TLH}$	Delta Low to High		0.12		0.13		0.16	ns/pF
d$_{THL}$	Delta High to Low		0.09		0.10		0.12	ns/pF

Notes:

1. Delays based on 50 pF loading.

2. SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.

A1280A Timing Characteristics (continued)

Table 2-19 • **A1280A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

I/O Module Input Propagation Delays		–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t$_{INYH}$	Pad to Y High		2.9		3.3		3.8	ns
t$_{INYL}$	Pad to Y Low		2.7		3.0		3.5	ns
t$_{INGH}$	G to Y High		5.0		5.7		6.6	ns
t$_{INGL}$	G to Y Low		4.8		5.4		6.3	ns
Input Module Predicted Input Routing Delays[*]								
t$_{IRD1}$	FO = 1 Routing Delay		4.6		5.1		6.0	ns
t$_{IRD2}$	FO = 2 Routing Delay		5.2		5.9		6.9	ns
t$_{IRD3}$	FO = 3 Routing Delay		5.6		6.3		7.4	ns
t$_{IRD4}$	FO = 4 Routing Delay		6.5		7.3		8.6	ns
t$_{IRD8}$	FO = 8 Routing Delay		9.4		10.5		12.4	ns
Global Clock Network								
t$_{CKH}$	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		13.1		14.6		17.2	
t$_{CKL}$	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		13.3		14.9		17.5	
t$_{PWH}$	Minimum Pulse Width High	FO = 32	5.0		5.5		6.6		ns
		FO = 256	5.8		6.4		7.6		
t$_{PWL}$	Minimum Pulse Width Low	FO = 32	5.0		5.5		6.6		ns
		FO = 256	5.8		6.4		7.6		
t$_{CKSW}$	Maximum Skew	FO = 32		0.5		0.5		0.5	ns
		FO = 256		2.5		2.5		2.5	
t$_{SUEXT}$	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t$_{HEXT}$	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t$_P$	Minimum Period	FO = 32	9.6		11.2		13.3		ns
		FO = 256	10.6		12.6		15.3		
f$_{MAX}$	Maximum Frequency	FO = 32		105.0		90.0		75.0	ns
		FO = 256		95.0		80.0		65.0	

*Note: *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1280A Timing Characteristics (continued)

Pin Descriptions

CLKA **Clock A (Input)**

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB **Clock B (Input)**

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK **Diagnostic Clock (Input)**

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

GND **Ground**

Low supply voltage.

I/O **Input/Output (Input, Output)**

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven Low by the ALS software.

MODE **Mode (Input)**

The MODE pin controls the use of multifunction pins (DCLK, PRA, PRB, SDI). When the MODE pin is High, the special functions are active. When the MODE pin is Low, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled High when required.

NC **No Connection**

This pin is not connected to circuitry within the device.

PRA **Probe A (Output)**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

PRB **Probe B (Output)**

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

SDI **Serial Data Input (Input)**

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

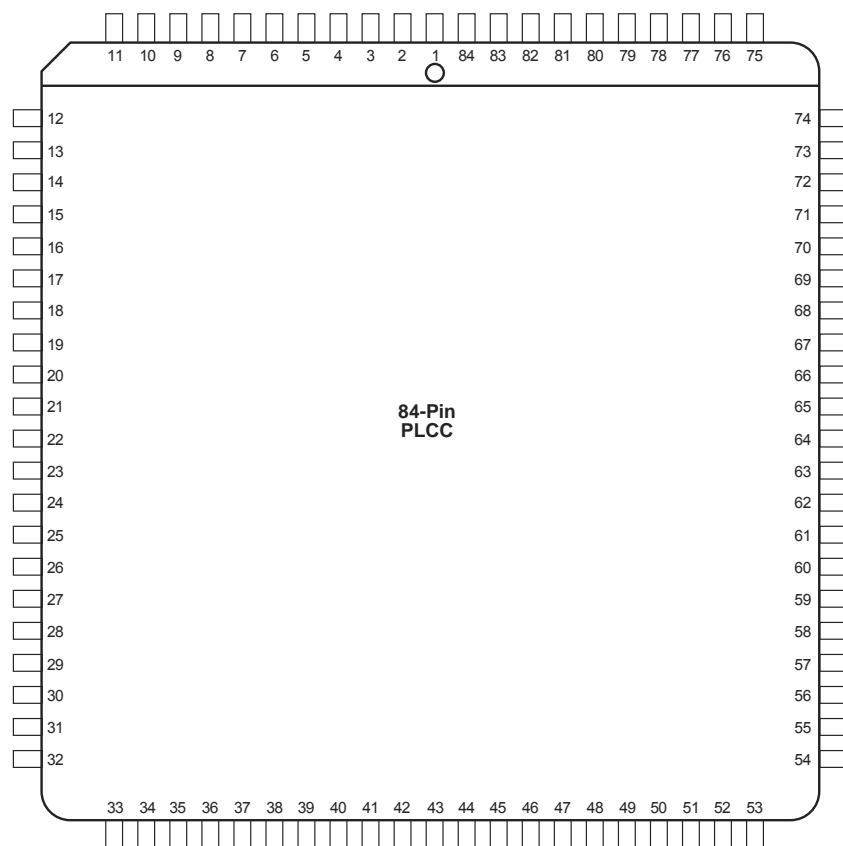**SDO** **Serial Data Output (Output)**

Serial data output for diagnostic probe. SDO is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

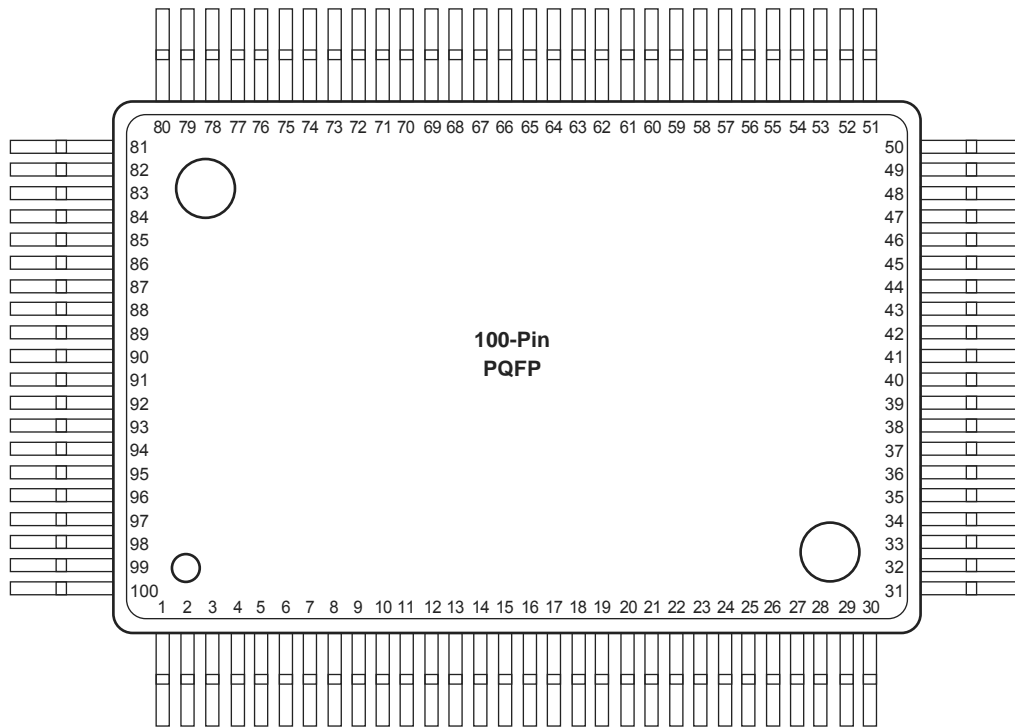**VCC** **5.0 V Supply Voltage**

High supply voltage.

Microsemi

3 – Package Pin Assignments

PL84

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.
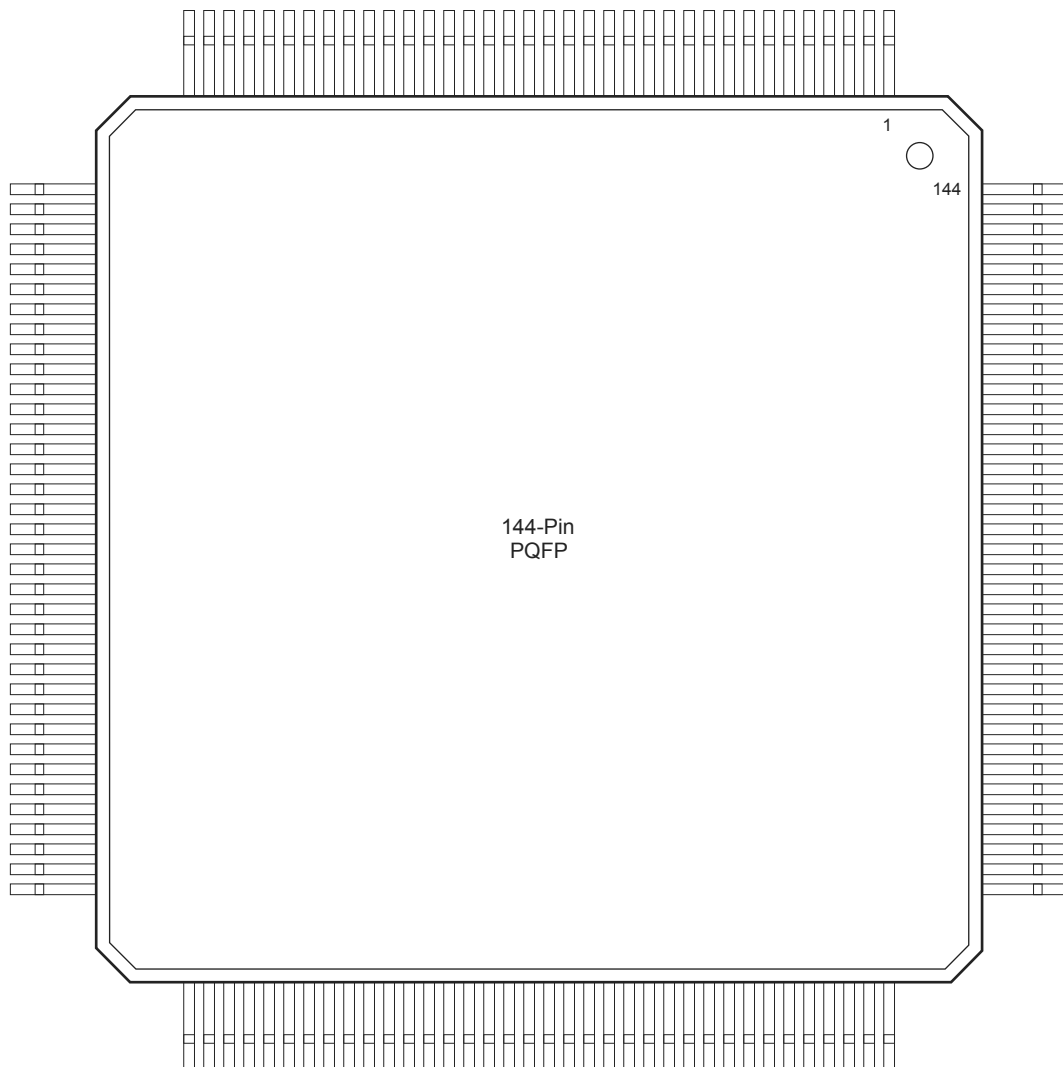
PQ100

100-Pin
PQFP

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

PQ144

144-Pin
PQFP

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

PQ144	
Pin Number	**A1240A Function**
2	MODE
9	GND
10	GND
11	GND
18	VCC
19	VCC
20	VCC
21	VCC
28	GND
29	GND
30	GND
44	GND
45	GND
46	GND
54	VCC
55	VCC
56	VCC
64	GND
65	GND
71	SDO
79	GND
80	GND
81	GND
88	GND

PQ144	
Pin Number	**A1240A Function**
89	VCC
90	VCC
91	VCC
92	VCC
93	VCC
100	GND
101	GND
102	GND
110	SDI, I/O
116	GND
117	GND
118	GND
123	PRA, I/O
125	CLKA, I/O
126	VCC
127	VCC
128	VCC
130	CLKB, I/O
132	PRB, I/O
136	GND
137	GND
138	GND
144	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.

2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PQ160
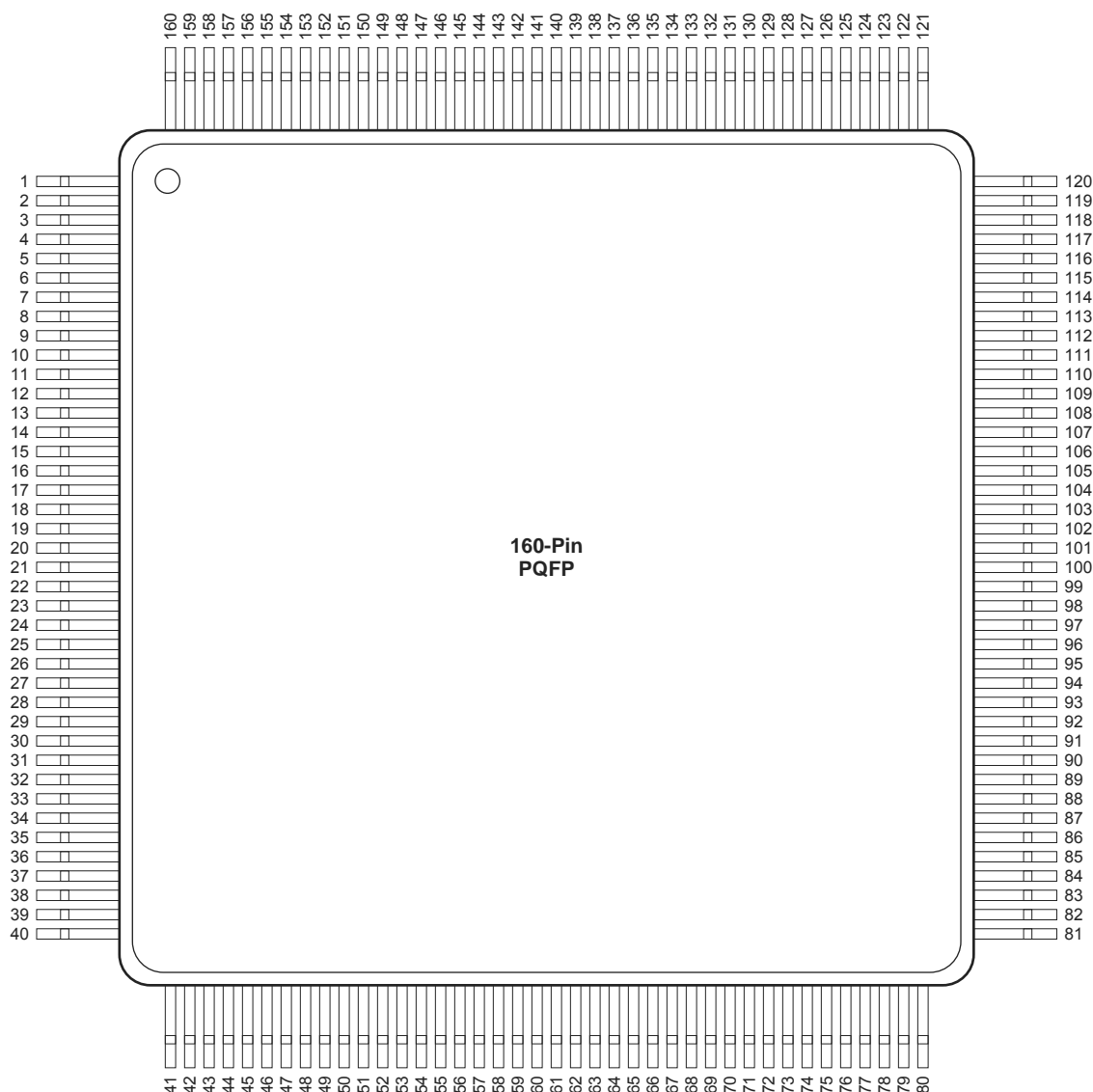
Note: This is the top view of the package

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

| CQ172		CQ172	
Pin Number	**A1280A Function**	**Pin Number**	**A1280A Function**
1	MODE	107	VCC
7	GND	108	GND
12	VCC	109	VCC
17	GND	110	VCC
22	GND	113	VCC
23	VCC	118	GND
24	VCC	123	GND
27	VCC	131	SDI, I/O
32	GND	136	VCC
37	GND	141	GND
50	VCC	148	PRA, I/O
55	GND	150	CLKA, I/O
65	GND	151	VCC
66	VCC	152	GND
75	GND	154	CLKB, I/O
80	VCC	156	PRB, I/O
85	SDO	161	GND
98	GND	166	VCC
103	GND	171	DCLK, I/O
106	GND		

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG100		PG100	
Pin Number	**A1225A Function**	**Pin Number**	**A1225A Function**
A4	PRB, I/O	E11	VCC
A7	PRA, I/O	F3	VCC
B6	VCC	F9	VCC
C2	MODE	F10	VCC
C3	DCLK, I/O	F11	GND
C5	GND	G1	VCC
C6	CLKA, I/O	G3	GND
C7	GND	G9	GND
C8	SDI, I/O	J5	GND
D6	CLKB, I/O	J7	GND
D10	GND	J9	SDO
E3	GND	K6	VCC

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG132
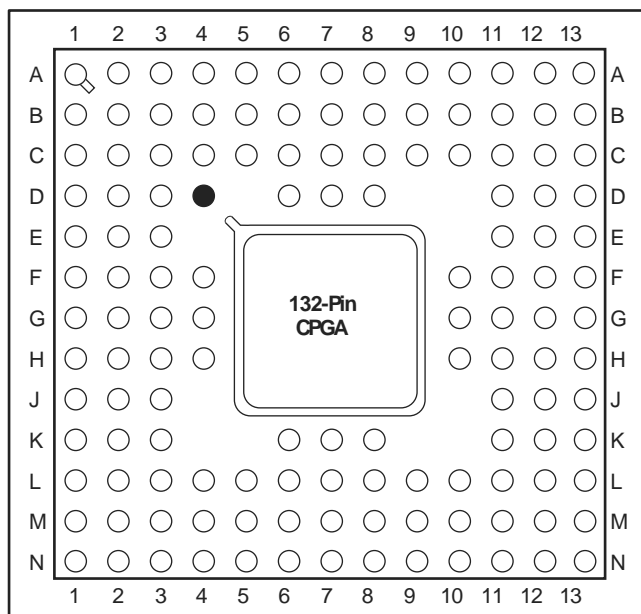
● Orientation Pin

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

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4 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each version of the datasheet.

Revision	Changes	Page
Revision 8 (January 2012)	The ACT 2 datasheet was formatted newly in the style used for current datasheets. The same information is present (other than noted in the list of changes for this revision) but divided into chapters.	N/A
	Package names used in Table 1 • ACT 2 Product Family Profile and throughout the document were revised to match standards given in *Package Mechanical Drawings* (SAR 27395).	I
	The description for SDO pins had earlier been removed from the datasheet and has now been included again, in the "Pin Descriptions" section (SAR 35819).	2-21
	SDO pin numbers had earlier been removed from package pin assignment tables in the datasheet, and have now been restored to the pin tables (SAR 35819).	3-2
Revision 7 (June 2006)	The "Ordering Information" section was revised to include RoHS information.	II
Revision 6 (December 2000)	In the "PG176" package, pin A3 was incorrectly assigned as CLKA, I/O. A3 is a user I/O. Pin A9 is CLKA, I/O.	3-21