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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	684
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	72
Number of Gates	4000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1240a-pl84c

Product Plan

Device/Package	Speed Grade ¹			Application ¹			
	Std.	-1	-2	C	I	M	B
A1225A Device							
84-Pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–
100-Pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	✓	–	–
100-Pin Very Thin Quad Flatpack (VQ)	✓	✓	✓	✓	–	–	–
100-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	–	–	–
A1240A Device							
84-Pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–
132-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	–	✓	✓
144-Pin Plastic Quad Flat Pack (PQ)	✓	✓	✓	✓	✓	–	–
176-Pin Thin (1.4 mm) Quad Flat Pack (TQ)	✓	✓	✓	✓	–	–	–
A1280A Device							
160-Pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	✓	–	–
172-Pin Ceramic Quad Flatpack (CQ)	✓	✓	✓	✓	–	✓	✓
176-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	–	✓	✓
176-Pin Thin (1.4 mm) Quad Flat Pack (TQ)	✓	✓	✓	✓	–	–	–

Notes:

1. **Applications:**
 C = Commercial
 I = Industrial
 M = Military
 B = MIL-STD-883

Availability:
 ✓ = Available
 P = Planned
 – = Not planned

Speed Grade:
 -1 = Approx. 15% faster than Std.
 -2 = Approx. 25% faster than Std.

2. Contact your Microsemi SoC Products Group sales representative for product availability.

Device Resources

Device Series	Logic Modules	Gates	User I/Os									
			PG176	PG132	PG100	PQ160	PQ144	PQ100	PL84	CQ172	TQ176	VQ100
A1225A	451	2,500	–	–	83	–	–	83	72	–	–	83
A1240A	684	4,000	–	104	–	–	104	–	72	–	104	–
A1280A	1,232	8,000	140	–	–	125	–	–	72	140	140	–

Contact your local Microsemi SoC Products Group representative for device availability:

<http://www.microsemi.com/soc/contact/default.aspx>.

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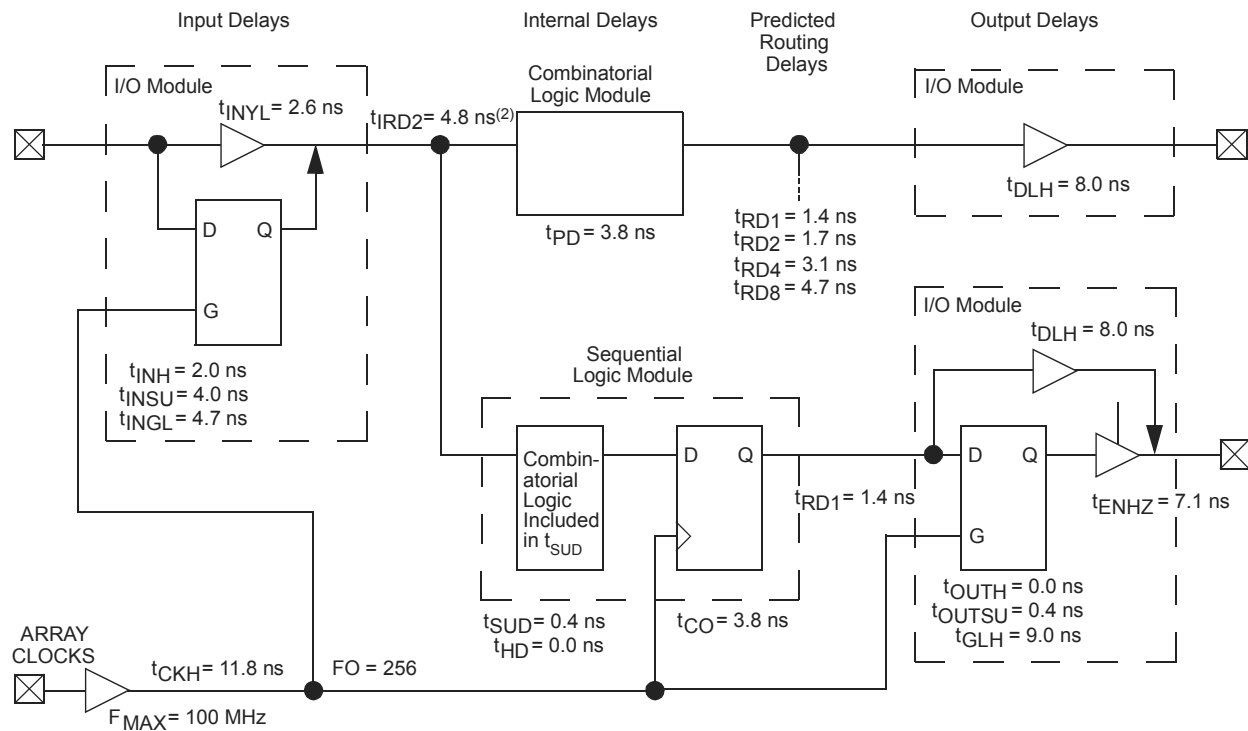
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ACT 2 Timing Model¹



Notes:

1. Values shown for A1240A-2 at worst-case commercial conditions.
2. Input module predicted routing delay

Figure 2-1 • Timing Model

Parameter Measurement

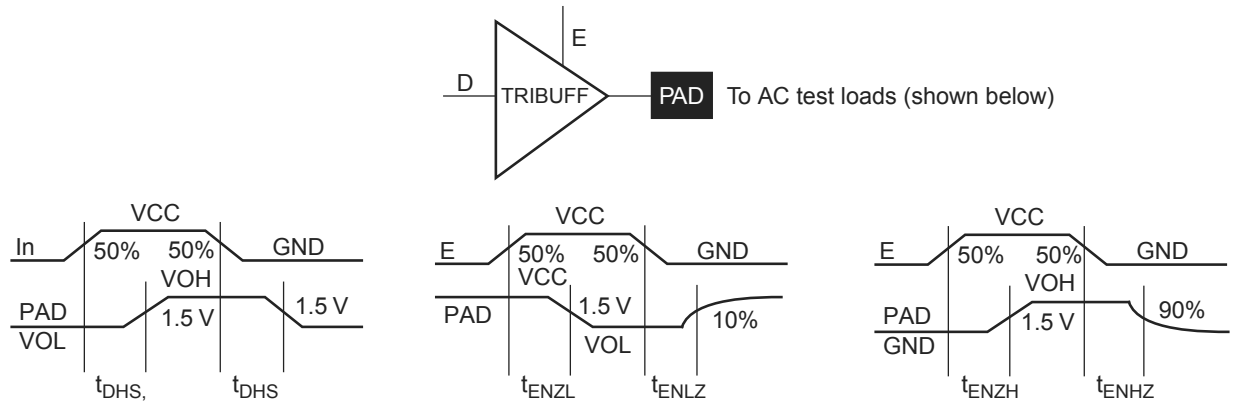


Figure 2-2 • Output Buffer Delays

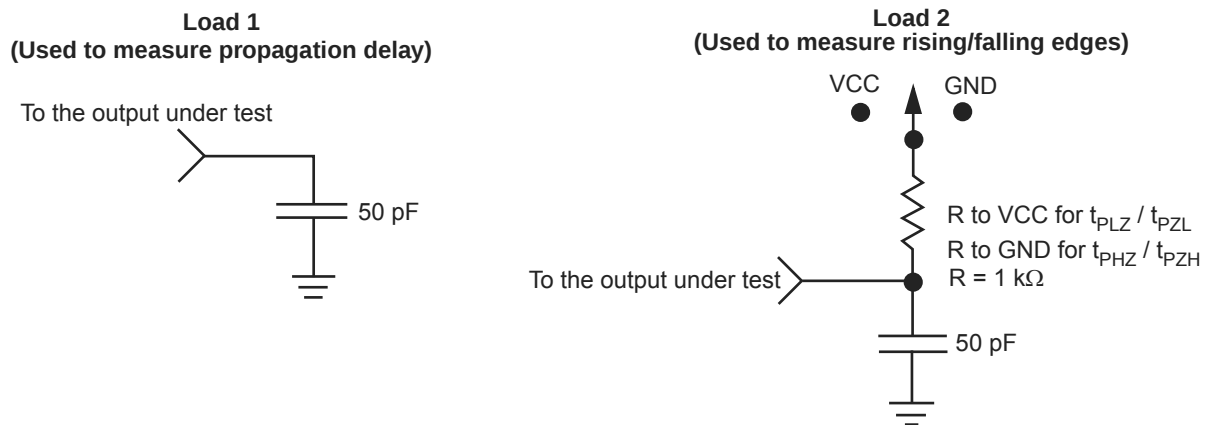


Figure 2-3 • AC Test Loads

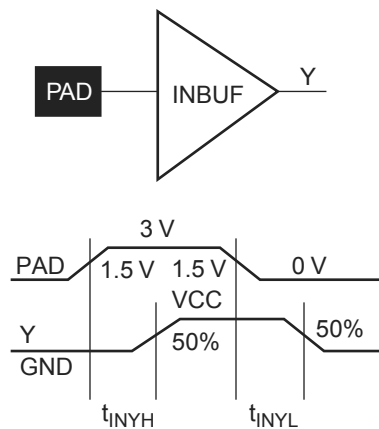


Figure 2-4 • Input Buffer Delays

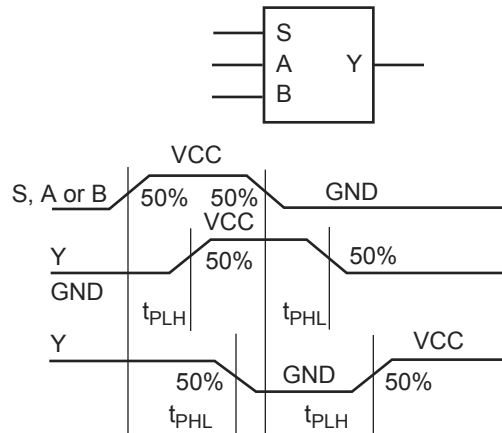
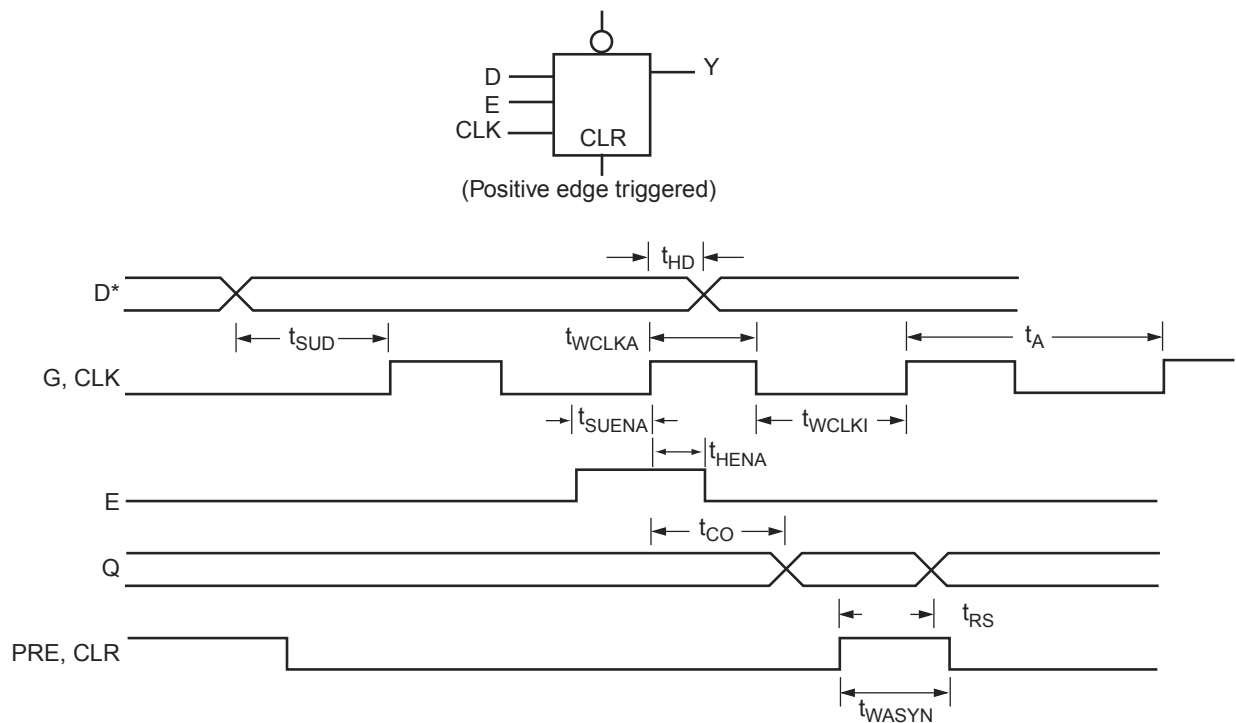


Figure 2-5 • Module Delays

Sequential Module Timing Characteristics



Note: D represents all data functions involving A, B, and S for multiplexed flip-flops.

Figure 2-6 • Flip-Flops and Latches

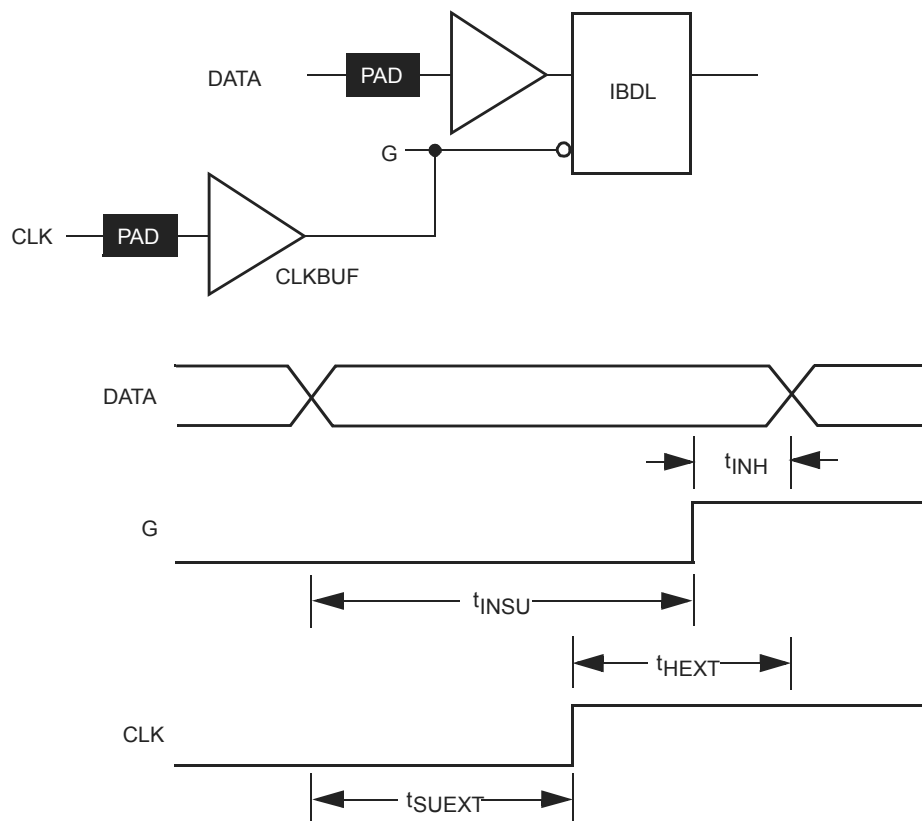


Figure 2-7 • Input Buffer Latches

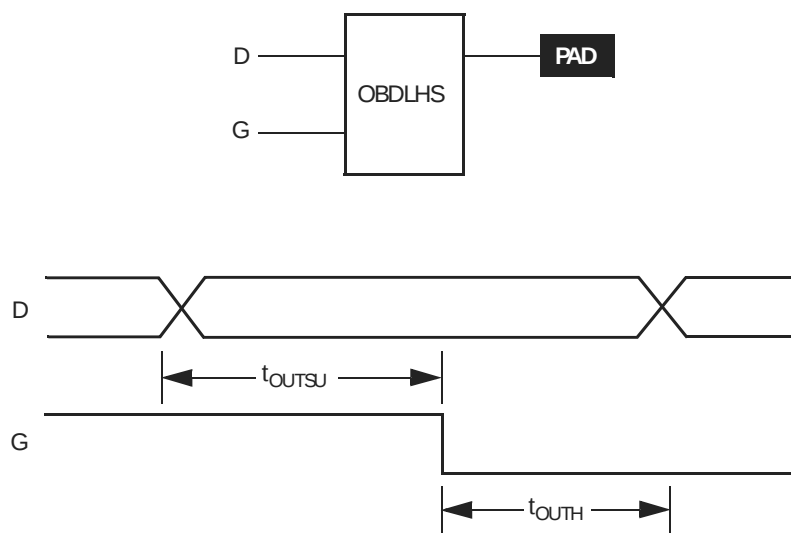


Figure 2-8 • Output Buffer Latches

A1225A Timing Characteristics

Table 2-12 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

Logic Module Propagation Delays ¹		–2 Speed ³		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD1}	Single Module		3.8		4.3		5.0	ns
t _{CO}	Sequential Clock to Q		3.8		4.3		5.0	ns
t _{GO}	Latch G to Q		3.8		4.3		5.0	ns
t _{RS}	Flip-Flop (Latch) Reset to Q		3.8		4.3		5.0	ns
Predicted Routing Delays²								
t _{RD1}	FO = 1 Routing Delay		1.1		1.2		1.4	ns
t _{RD2}	FO = 2 Routing Delay		1.7		1.9		2.2	ns
t _{RD3}	FO = 3 Routing Delay		2.3		2.6		3.0	ns
t _{RD4}	FO = 4 Routing Delay		2.8		3.1		3.7	ns
t _{RD8}	FO = 8 Routing Delay		4.4		4.9		5.8	ns
Sequential Timing Characteristics^{3,4}								
t _{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		ns
t _{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t _{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.5		5.0		6.0		ns
t _{WASYN}	Flip-Flop (Latch) Clock Asynchronous Pulse Width	4.5		5.0		6.0		ns
t _A	Flip-Flop Clock Input Period	9.4		11.0		13.0		ns
t _{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t _{INSU}	Input Buffer Latch Setup	0.4		0.4		0.5		ns
t _{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t _{OUTSU}	Output Buffer Latch Setup	0.4		0.4		0.5		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency		105.0		90.0		75.0	MHz

Notes:

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}—whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
4. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1225A Timing Characteristics (continued)

Table 2-13 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module Input Propagation Delays			–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description			Min.	Max.	Min.	Max.	Min.	Max.	
t _{INYH}	Pad to Y High			2.9		3.3		3.8	ns
t _{INYL}	Pad to Y Low			2.6		3.0		3.5	ns
t _{INGH}	G to Y High			5.0		5.7		6.6	ns
t _{INGL}	G to Y Low			4.7		5.4		6.3	ns
Input Module Predicted Input Routing Delays*									
t _{IRD1}	FO = 1 Routing Delay			4.1		4.6		5.4	ns
t _{IRD2}	FO = 2 Routing Delay			4.6		5.2		6.1	ns
t _{IRD3}	FO = 3 Routing Delay			5.3		6.0		7.1	ns
t _{IRD4}	FO = 4 Routing Delay			5.7		6.4		7.6	ns
t _{IRD8}	FO = 8 Routing Delay			7.4		8.3		9.8	ns
Global Clock Network									
t _{CKH}	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		11.8		13.0		15.7	
t _{CKL}	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		12.0		13.2		15.9	
t _{PWH}	Minimum Pulse Width High	FO = 32	3.4		4.1		4.5		ns
		FO = 256	3.8		4.5		5.0		
t _{PWL}	Minimum Pulse Width Low	FO = 32	3.4		4.1		4.5		ns
		FO = 256	3.8		4.5		5.0		
t _{CKSW}	Maximum Skew	FO = 32		0.7		0.7		0.7	ns
		FO = 256		3.5		3.5		3.5	
t _{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t _{HEXT}	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t _P	Minimum Period	FO = 32	7.7		8.3		9.1		ns
		FO = 256	8.1		8.8		10.0		
f _{MAX}	Maximum Frequency	FO = 32		130.0		120.0		110.0	ns
		FO = 256		125.0		115.0		100.0	

Note: *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1240A Timing Characteristics (continued)

Table 2-16 • A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module Input Propagation Delays			–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description			Min.	Max.	Min.	Max.	Min.	Max.	
t _{INYH}	Pad to Y High			2.9		3.3		3.8	ns
t _{INYL}	Pad to Y Low			2.6		3.0		3.5	ns
t _{INGH}	G to Y High			5.0		5.7		6.6	ns
t _{INGL}	G to Y Low			4.7		5.4		6.3	ns
Input Module Predicted Input Routing Delays*									
t _{IRD1}	FO = 1 Routing Delay			4.2		4.8		5.6	ns
t _{IRD2}	FO = 2 Routing Delay			4.8		5.4		6.4	ns
t _{IRD3}	FO = 3 Routing Delay			5.4		6.1		7.2	ns
t _{IRD4}	FO = 4 Routing Delay			5.9		6.7		7.9	ns
t _{IRD8}	FO = 8 Routing Delay			7.9		8.9		10.5	ns
Global Clock Network									
t _{CKH}	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		11.8		13.0		15.7	
t _{CKL}	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		12.0		13.2		15.9	
t _{PWH}	Minimum Pulse Width High	FO = 32	3.8		4.5		5.5		ns
		FO = 256	4.1		5.0		5.8		
t _{PWL}	Minimum Pulse Width Low	FO = 32	3.8		4.5		5.5		ns
		FO = 256	4.1		5.0		5.8		
t _{CKSW}	Maximum Skew	FO = 32		0.5		0.5		0.5	ns
		FO = 256		2.5		2.5		2.5	
t _{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t _{HEXT}	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t _P	Minimum Period	FO = 32	8.1		9.1		11.1		ns
		FO = 256	8.8		10.0		11.7		
f _{MAX}	Maximum Frequency	FO = 32		125.0		110.0		90.0	ns
		FO = 256		115.0		100.0		85.0	

Note: *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

Pin Descriptions

CLKA Clock A (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB Clock B (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

GND Ground

Low supply voltage.

I/O Input/Output (Input, Output)

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven Low by the ALS software.

MODE Mode (Input)

The MODE pin controls the use of multifunction pins (DCLK, PRA, PRB, SDI). When the MODE pin is High, the special functions are active. When the MODE pin is Low, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled High when required.

NC No Connection

This pin is not connected to circuitry within the device.

PRA Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

PRB Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

SDO Serial Data Output (Output)

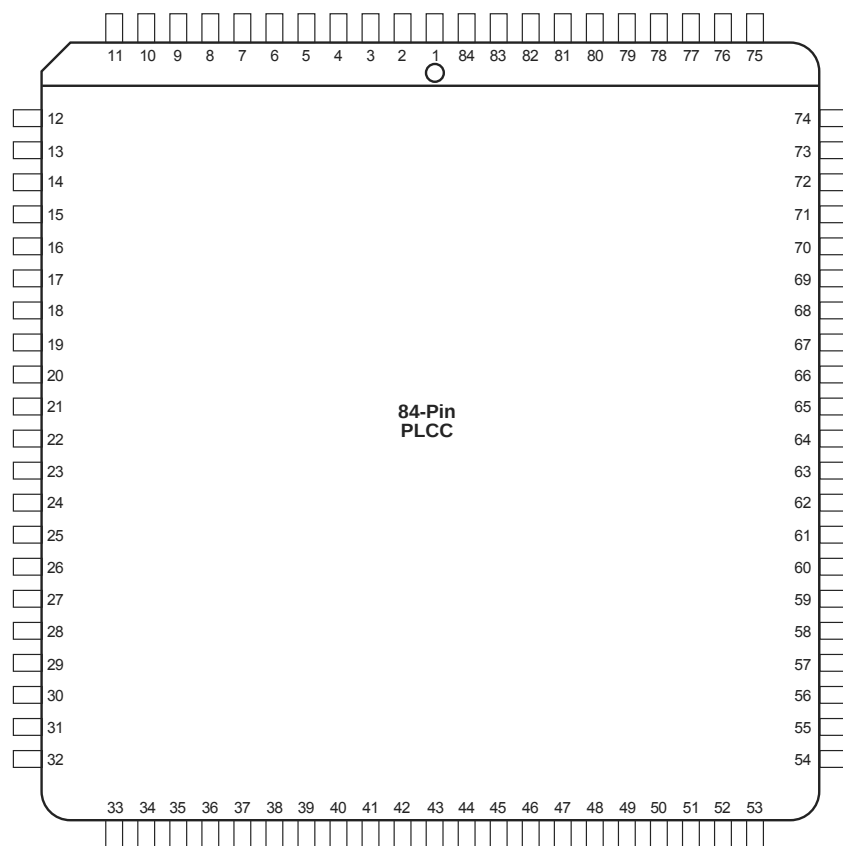
Serial data output for diagnostic probe. SDO is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

VCC 5.0 V Supply Voltage

High supply voltage.

3 – Package Pin Assignments

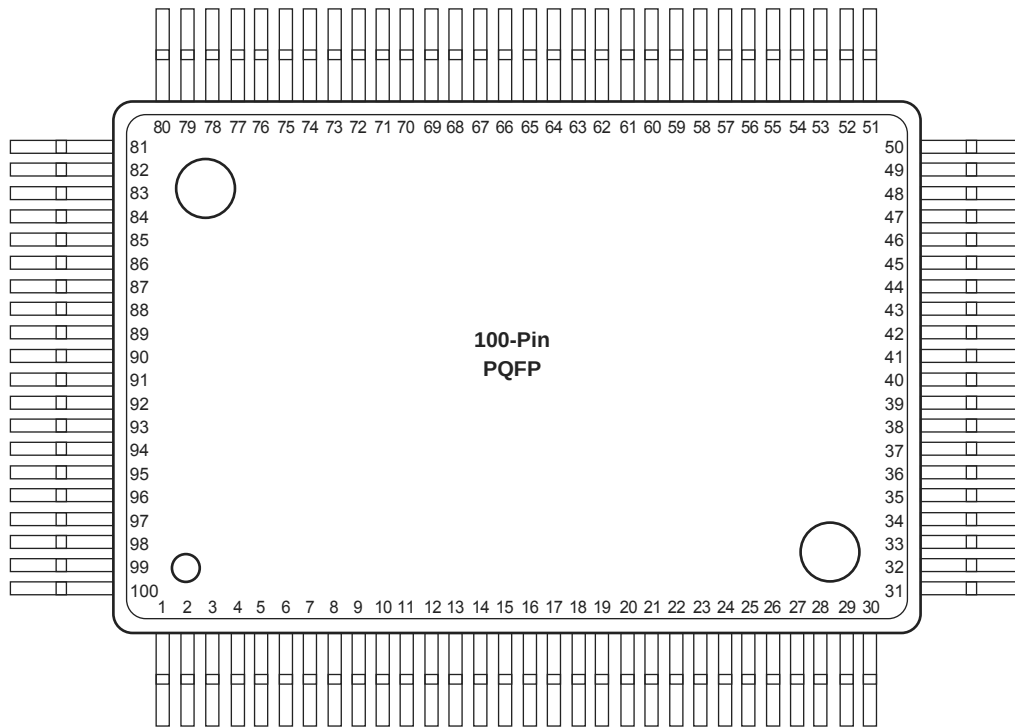
PL84



Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

PQ100



Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

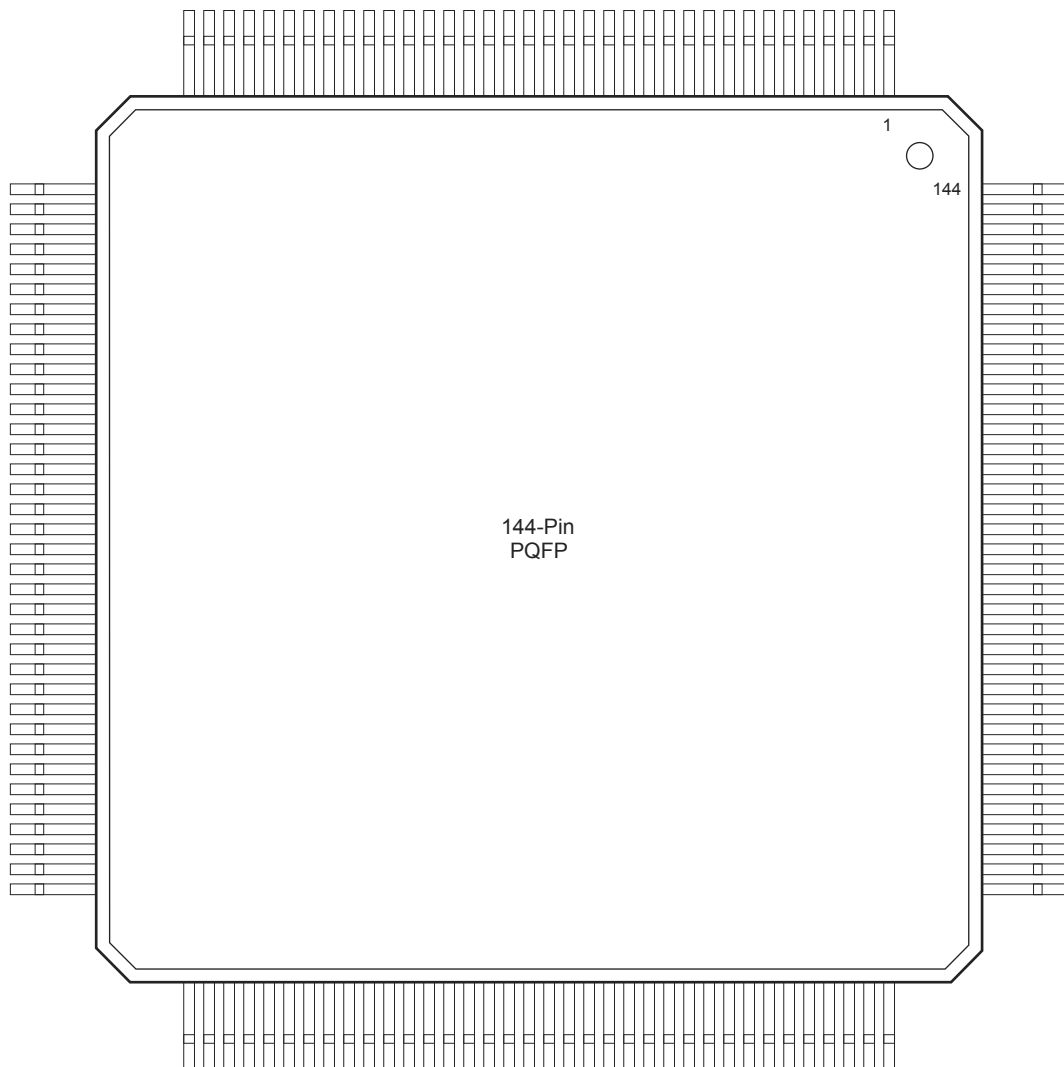
PQ100	
Pin Number	A1225A Function
2	DCLK, I/O
4	MODE
9	GND
16	VCC
17	VCC
22	GND
34	GND
40	VCC
46	GND
52	SDO
57	GND
64	GND

PQ100	
Pin Number	A1225A Function
65	VCC
66	VCC
67	VCC
72	GND
79	SDI, I/O
84	GND
87	PRA, I/O
89	CLKA, I/O
90	VCC
92	CLKB, I/O
94	PRB, I/O
96	GND

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PQ144



Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

PQ160	
Pin Number	A1280A Function
2	DCLK, I/O
6	VCC
11	GND
16	PRB, I/O
18	CLKB, I/O
20	VCC
21	CLKA, I/O
23	PRA, I/O
30	GND
35	VCC
38	SDI, I/O
40	GND
44	GND
49	GND
54	VCC
57	VCC
58	VCC
59	GND
60	VCC
61	GND
64	GND

PQ160	
Pin Number	A1280A Function
69	GND
80	GND
82	SDO
86	VCC
89	GN
98	GND
99	GND
109	GND
114	VCC
120	GND
125	GND
130	GND
135	VCC
138	VCC
139	VCC
140	GND
145	GND
150	VCC
155	GND
159	MODE
160	GND

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

TQ176		
Pin Number	A1240A Function	A1280A Function
1	GND	GND
2	MODE	MODE
8	NC	NC
10	NC	I/O
11	NC	I/O
13	NC	VCC
18	GND	GND
19	NC	I/O
20	NC	I/O
22	NC	I/O
23	GND	GND
24	NC	VCC
25	VCC	VCC
26	NC	I/O
27	NC	I/O
28	VCC	VCC
29	NC	I/O
33	NC	NC
37	NC	I/O
38	NC	NC
45	GND	GND
52	NC	VCC
54	NC	I/O
55	NC	I/O
57	NC	NC
61	NC	I/O
64	NC	I/O
66	NC	I/O
67	GND	GND
68	VCC	VCC
74	NC	I/O
77	NC	NC
78	NC	I/O
80	NC	I/O

TQ176		
Pin Number	A1240A Function	A1280A Function
82	NC	VCC
86	NC	I/O
87	SDO	SDO
89	GND	GND
96	NC	I/O
97	NC	I/O
101	NC	NC
103	NC	I/O
106	GND	GND
107	NC	I/O
108	NC	I/O
109	GND	GND
110	VCC	VCC
111	GND	GND
112	VCC	VCC
113	VCC	VCC
114	NC	I/O
115	NC	I/O
116	NC	VCC
121	NC	NC
124	NC	I/O
125	NC	I/O
126	NC	NC
133	GND	GND
135	SDI, I/O	SDI, I/O
136	NC	I/O
140	NC	VCC
143	NC	I/O
144	NC	I/O
145	NC	NC
147	NC	I/O
151	NC	I/O
152	PRA, I/O	PRA, I/O
154	CLKA, I/O	CLKA, I/O

TQ176		
Pin Number	A1240A Function	A1280A Function
155	VCC	VCC
156	GND	GND
158	CLKB, I/O	CLKB, I/O
160	PRB, I/O	PRB, I/O
161	NC	I/O
165	NC	NC
166	NC	I/O
168	NC	I/O
170	NC	VCC
173	NC	I/O
175	DCLK, I/O	DCLK, I/O

Notes:

1. NC denotes no connection.
2. All unlisted pin numbers are user I/Os.
3. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG132	
Pin Number	A1240A Function
A1	MODE
B5	GND
B6	CLKB, I/O
B7	CLKA, I/O
B8	PRA, I/O
B9	GND
B12	SDI, I/O
C3	DCLK, I/O
C5	GND
C6	PRB, I/O
C7	VCC
C9	GND
D7	VCC
E3	GND
E11	GND
E12	GND
F4	GND
G2	VCC

PG132	
Pin Number	A1240A Function
G3	VCC
G4	VCC
G10	VCC
G11	VCC
G12	VCC
G13	VCC
H13	GND
J2	GND
J3	GND
J11	GND
K7	VCC
K12	GND
L5	GND
L7	VCC
L9	GND
M9	GND
N12	SDO

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG176	
Pin Number	A1280A Function
A9	CLKA, I/O
B3	DCLK, I/O
B8	CLKB, I/O
B14	SDI, I/O
C3	MODE
C8	GND
C9	PRA, I/O
D4	GND
D5	VCC
D6	GND
D7	PRB, I/O
D8	VCC
D10	GND
D11	VCC
D12	GND
E4	GND
E12	GND
F4	VCC
F12	GND
G4	GND
G12	VCC
H2	VCC

PG176	
Pin Number	A1280A Function
H3	VCC
H4	GND
H12	GND
H13	VCC
H14	VCC
J4	VCC
J12	GND
J13	GND
J14	VCC
K4	GND
K12	GND
L4	GND
M4	GND
M5	VCC
M6	GND
M8	GND
M10	GND
M11	VCC
M12	GND
N8	VCC
P13	SDO

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.



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