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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	684
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	104
Number of Gates	4000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-BQFP
Supplier Device Package	144-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1240a-pq144c

Product Plan

Device/Package	Speed Grade ¹			Application ¹			
	Std.	–1	–2	C	I	M	B
A1225A Device							
84-Pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–
100-Pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	✓	–	–
100-Pin Very Thin Quad Flatpack (VQ)	✓	✓	✓	✓	–	–	–
100-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	–	–	–
A1240A Device							
84-Pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–
132-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	–	✓	✓
144-Pin Plastic Quad Flat Pack (PQ)	✓	✓	✓	✓	✓	–	–
176-Pin Thin (1.4 mm) Quad Flat Pack (TQ)	✓	✓	✓	✓	–	–	–
A1280A Device							
160-Pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	✓	–	–
172-Pin Ceramic Quad Flatpack (CQ)	✓	✓	✓	✓	–	✓	✓
176-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	–	✓	✓
176-Pin Thin (1.4 mm) Quad Flat Pack (TQ)	✓	✓	✓	✓	–	–	–

Notes:

1. **Applications:**
 C = Commercial
 I = Industrial
 M = Military
 B = MIL-STD-883

Availability:
 ✓ = Available
 P = Planned
 – = Not planned

Speed Grade:
 –1 = Approx. 15% faster than Std.
 –2 = Approx. 25% faster than Std.

2. Contact your Microsemi SoC Products Group sales representative for product availability.

Device Resources

Device Series	Logic Modules	Gates	User I/Os									
			PG176	PG132	PG100	PQ160	PQ144	PQ100	PL84	CQ172	TQ176	VQ100
A1225A	451	2,500	–	–	83	–	–	83	72	–	–	83
A1240A	684	4,000	–	104	–	–	104	–	72	–	104	–
A1280A	1,232	8,000	140	–	–	125	–	–	72	140	140	–

Contact your local Microsemi SoC Products Group representative for device availability:

<http://www.microsemi.com/soc/contact/default.aspx>.

Table 2-3 • Electrical Specifications

Symbol	Parameter	Commercial		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
VOH ¹	(IOH = –10 mA) ²	2.4	–	–	–	–	–	V
	(IOH = –6 mA)	3.84	–	–	–	–	–	V
	(IOH = –4 mA)	–	–	3.7	–	3.7	–	V
VOL ¹	(IOL = 10 mA) ²	–	0.5	–	–	–	–	V
	(IOL = 6 mA)	–	0.33	–	0.40	–	0.40	V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
Input Transition Time t _R , t _F ²		–	500	–	500	–	500	ns
C _{IO} I/O capacitance ^{2,3}		–	10	–	10	–	10	pF
Standby Current, ICC ⁴ (typical = 1 mA)		–	2	–	10	–	20	mA
Leakage Current ⁵		–10	+10	–10	+10	–10	+10	μA
ICC(D)	Dynamic VCC supply current. See the Power Dissipation section.							

Notes:

1. Only one output tested at a time. VCC = minimum.
2. Not tested, for information only.
3. Includes worst-case PG176 package capacitance. VOUT = 0 V, f = 1 MHz
4. All outputs unloaded. All inputs = VCC or GND, typical ICC = 1 mA. ICC limit includes IPP and ISV during normal operations.
5. VOUT, VIN = VCC or GND.

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. EQ 4 shows a piece-wise linear summation over all components.

$$\begin{aligned}
 \text{Power} = & VCC^2 * [(m * C_{EQM} * f_m)_{\text{modules}} + (n * C_{EQI} * f_n)_{\text{inputs}} \\
 & + (p * (C_{EQO} + C_L) * f_p)_{\text{outputs}} \\
 & + 0.5 * (q1 * C_{EQCR} * f_{q1})_{\text{routed_Clk1}} + (r1 * f_{q1})_{\text{routed_Clk1}} \\
 & + 0.5 * (q2 * C_{EQCR} * f_{q2})_{\text{routed_Clk2}} + (r2 * f_{q2})_{\text{routed_Clk2}}
 \end{aligned}$$

EQ 4

Where:

m = Number of logic modules switching at f_m

n = Number of input buffers switching at f_n

p = Number of output buffers switching at f_p

q1 = Number of clock loads on the first routed array clock

q2 = Number of clock loads on the second routed array clock

r_1 = Fixed capacitance due to first routed array clock

r_2 = Fixed capacitance due to second routed array clock

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_L = Output lead capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz

f_{q2} = Average second routed array clock rate in MHz

Table 2-7 • Fixed Capacitance Values for Microsemi FPGAs

Device Type	r_1 , routed_Clk1	r_2 , routed_Clk2
A1225A	106	106.0
A1240A	134	134.2
A1280A	168	167.8

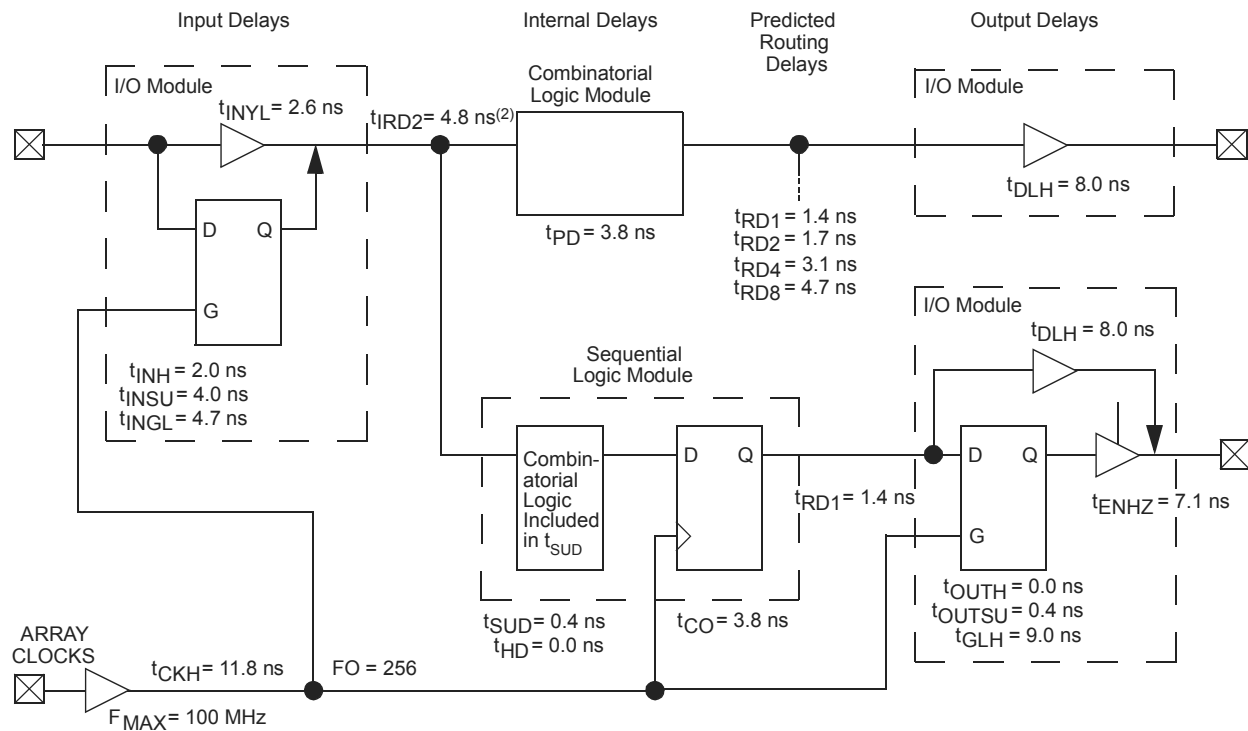
Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are given in Table 2-8.

Table 2-8 • Guidelines for Predicting Power Dissipation

Data	Value
Logic Modules (m)	80% of modules
Inputs switching (n)	# inputs/4
Outputs switching (p)	# output/4
First routed array clock loads (q1)	40% of sequential modules
Second routed array clock loads (q2)	40% of sequential modules
Load capacitance (C_L)	35 pF
Average logic module switching rate (f_m)	F/10
Average input switching rate (f_n)	F/5
Average output switching rate (f_p)	F/10
Average first routed array clock rate (f_{q1})	F
Average second routed array clock rate (f_{q2})	F/2

ACT 2 Timing Model¹



Notes:

1. Values shown for A1240A-2 at worst-case commercial conditions.
2. Input module predicted routing delay

Figure 2-1 • Timing Model

Timing Derating Factor (Temperature and Voltage)

Table 2-9 • Timing Derating Factor (Temperature and Voltage)

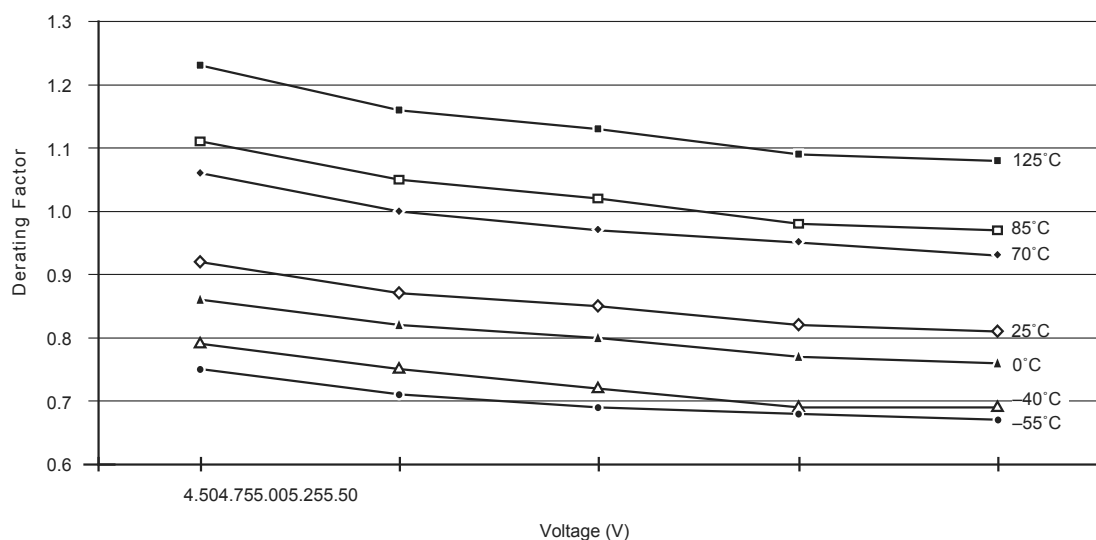
(Commercial Minimum/Maximum Specification) x	Industrial		Military	
	Min.	Max.	Min.	Max.
	0.69	1.11	0.67	1.23

Table 2-10 • Timing Derating Factor for Designs at Typical Temperature ($T_J = 25^\circ\text{C}$) and Voltage (5.0 V)

(Commercial Maximum Specification) x	0.85
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**Table 2-11 • Temperature and Voltage Derating Factors
(normalized to Worst-Case Commercial, $T_J = 4.75\text{ V}$, 70°C)**

	-55	-40	0	25	70	85	125
4.50	0.75	0.79	0.86	0.92	1.06	1.11	1.23
4.75	0.71	0.75	0.82	0.87	1.00	1.05	1.13
5.00	0.69	0.72	0.80	0.85	0.97	1.02	1.13
5.25	0.68	0.69	0.77	0.82	0.95	0.98	1.09
5.50	0.67	0.69	0.76	0.81	0.93	0.97	1.08



Note: This derating factor applies to all routing and propagation delays.

**Figure 2-9 • Junction Temperature and Voltage Derating Curves
(normalized to Worst-Case Commercial, $T_J = 4.75\text{ V}$, 70°C)**

A1225A Timing Characteristics

Table 2-12 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

Logic Module Propagation Delays ¹		–2 Speed ³		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD1}	Single Module		3.8		4.3		5.0	ns
t _{CO}	Sequential Clock to Q		3.8		4.3		5.0	ns
t _{GO}	Latch G to Q		3.8		4.3		5.0	ns
t _{RS}	Flip-Flop (Latch) Reset to Q		3.8		4.3		5.0	ns
Predicted Routing Delays²								
t _{RD1}	FO = 1 Routing Delay		1.1		1.2		1.4	ns
t _{RD2}	FO = 2 Routing Delay		1.7		1.9		2.2	ns
t _{RD3}	FO = 3 Routing Delay		2.3		2.6		3.0	ns
t _{RD4}	FO = 4 Routing Delay		2.8		3.1		3.7	ns
t _{RD8}	FO = 8 Routing Delay		4.4		4.9		5.8	ns
Sequential Timing Characteristics^{3,4}								
t _{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		ns
t _{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t _{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.5		5.0		6.0		ns
t _{WASYN}	Flip-Flop (Latch) Clock Asynchronous Pulse Width	4.5		5.0		6.0		ns
t _A	Flip-Flop Clock Input Period	9.4		11.0		13.0		ns
t _{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t _{INSU}	Input Buffer Latch Setup	0.4		0.4		0.5		ns
t _{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t _{OUTSU}	Output Buffer Latch Setup	0.4		0.4		0.5		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency		105.0		90.0		75.0	MHz

Notes:

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}—whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
4. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1240A Timing Characteristics (continued)

Table 2-17 • A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

TTL Output Module Timing ¹		–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t _{DLH}	Data to Pad High		8.0		9.0		10.6	ns
t _{DHL}	Data to Pad Low		10.1		11.4		13.4	ns
t _{ENZH}	Enable Pad Z to High		8.9		10.0		11.8	ns
t _{ENZL}	Enable Pad Z to Low		11.7		13.2		15.5	ns
t _{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t _{ENLZ}	Enable Pad Low to Z		8.4		9.5		11.1	ns
t _{GLH}	G to Pad High		9.0		10.2		11.9	ns
t _{GHL}	G to Pad Low		11.2		12.7		14.9	ns
d _{TLH}	Delta Low to High		0.07		0.08		0.09	ns/pF
d _{THL}	Delta High to Low		0.12		0.13		0.16	ns/pF
CMOS Output Module Timing ¹								
t _{DLH}	Data to Pad High		10.2		11.5		13.5	ns
t _{DHL}	Data to Pad Low		8.4		9.6		11.2	ns
t _{ENZH}	Enable Pad Z to High		8.9		10.0		11.8	ns
t _{ENZL}	Enable Pad Z to Low		11.7		13.2		15.5	ns
t _{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t _{ENLZ}	Enable Pad Low to Z		8.4		9.5		11.1	ns
t _{GLH}	G to Pad High		9.0		10.2		11.9	ns
t _{GHL}	G to Pad Low		11.2		12.7		14.9	ns
d _{TLH}	Delta Low to High		0.12		0.13		0.16	ns/pF
d _{THL}	Delta High to Low		0.09		0.10		0.12	ns/pF

Notes:

1. Delays based on 50 pF loading.
2. SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.

A1280A Timing Characteristics (continued)

Table 2-19 • A1280A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module Input Propagation Delays			–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description			Min.	Max.	Min.	Max.	Min.	Max.	
t _{INYH}	Pad to Y High			2.9		3.3		3.8	ns
t _{INYL}	Pad to Y Low			2.7		3.0		3.5	ns
t _{INGH}	G to Y High			5.0		5.7		6.6	ns
t _{INGL}	G to Y Low			4.8		5.4		6.3	ns
Input Module Predicted Input Routing Delays*									
t _{IRD1}	FO = 1 Routing Delay			4.6		5.1		6.0	ns
t _{IRD2}	FO = 2 Routing Delay			5.2		5.9		6.9	ns
t _{IRD3}	FO = 3 Routing Delay			5.6		6.3		7.4	ns
t _{IRD4}	FO = 4 Routing Delay			6.5		7.3		8.6	ns
t _{IRD8}	FO = 8 Routing Delay			9.4		10.5		12.4	ns
Global Clock Network									
t _{CKH}	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		13.1		14.6		17.2	
t _{CKL}	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		13.3		14.9		17.5	
t _{PWH}	Minimum Pulse Width High	FO = 32	5.0		5.5		6.6		ns
		FO = 256	5.8		6.4		7.6		
t _{PWL}	Minimum Pulse Width Low	FO = 32	5.0		5.5		6.6		ns
		FO = 256	5.8		6.4		7.6		
t _{CKSW}	Maximum Skew	FO = 32		0.5		0.5		0.5	ns
		FO = 256		2.5		2.5		2.5	
t _{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t _{HEXT}	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t _P	Minimum Period	FO = 32	9.6		11.2		13.3		ns
		FO = 256	10.6		12.6		15.3		
f _{MAX}	Maximum Frequency	FO = 32		105.0		90.0		75.0	ns
		FO = 256		95.0		80.0		65.0	

Note: *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1280A Timing Characteristics (continued)

Table 2-20 • A1280A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

TTL Output Module Timing ¹		–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t _{DLH}	Data to Pad High		8.1		9.0		10.6	ns
t _{DHL}	Data to Pad Low		10.2		11.4		13.4	ns
t _{ENZH}	Enable Pad Z to High		9.0		10.0		11.8	ns
t _{ENZL}	Enable Pad Z to Low		11.8		13.2		15.5	ns
t _{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t _{ENLZ}	Enable Pad Low to Z		8.4		9.5		11.1	ns
t _{GLH}	G to Pad High		9.0		10.2		11.9	ns
t _{GHL}	G to Pad Low		11.3		12.7		14.9	ns
d _{TLH}	Delta Low to High		0.07		0.08		0.09	ns/pF
d _{THL}	Delta High to Low		0.12		0.13		0.16	ns/pF
CMOS Output Module Timing ¹								
t _{DLH}	Data to Pad High		10.3		11.5		13.5	ns
t _{DHL}	Data to Pad Low		8.5		9.6		11.2	ns
t _{ENZH}	Enable Pad Z to High		9.0		10.0		11.8	ns
t _{ENZL}	Enable Pad Z to Low		11.8		13.2		15.5	ns
t _{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t _{ENLZ}	Enable Pad Low to Z		8.4		9.5		11.1	ns
t _{GLH}	G to Pad High		9.0		10.2		11.9	ns
t _{GHL}	G to Pad Low		11.3		12.7		14.9	ns
d _{TLH}	Delta Low to High		0.12		0.13		0.16	ns/pF
d _{THL}	Delta High to Low		0.09		0.10		0.12	ns/pF

Notes:

1. Delays based on 50 pF loading.
2. SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.

Pin Descriptions

CLKA Clock A (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB Clock B (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

GND Ground

Low supply voltage.

I/O Input/Output (Input, Output)

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven Low by the ALS software.

MODE Mode (Input)

The MODE pin controls the use of multifunction pins (DCLK, PRA, PRB, SDI). When the MODE pin is High, the special functions are active. When the MODE pin is Low, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled High when required.

NC No Connection

This pin is not connected to circuitry within the device.

PRA Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

PRB Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

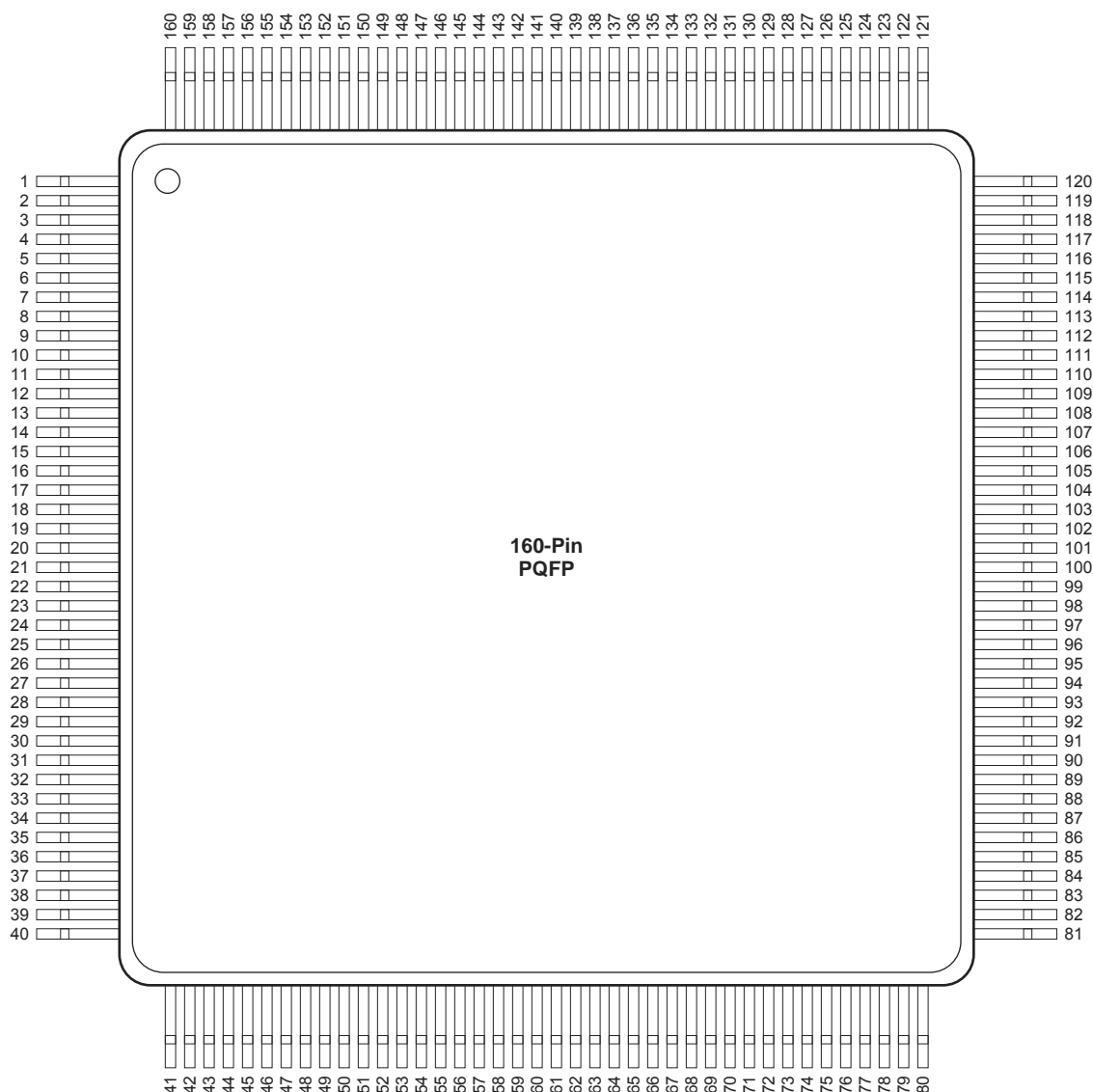
SDO Serial Data Output (Output)

Serial data output for diagnostic probe. SDO is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

VCC 5.0 V Supply Voltage

High supply voltage.

PQ160



Note: This is the top view of the package

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

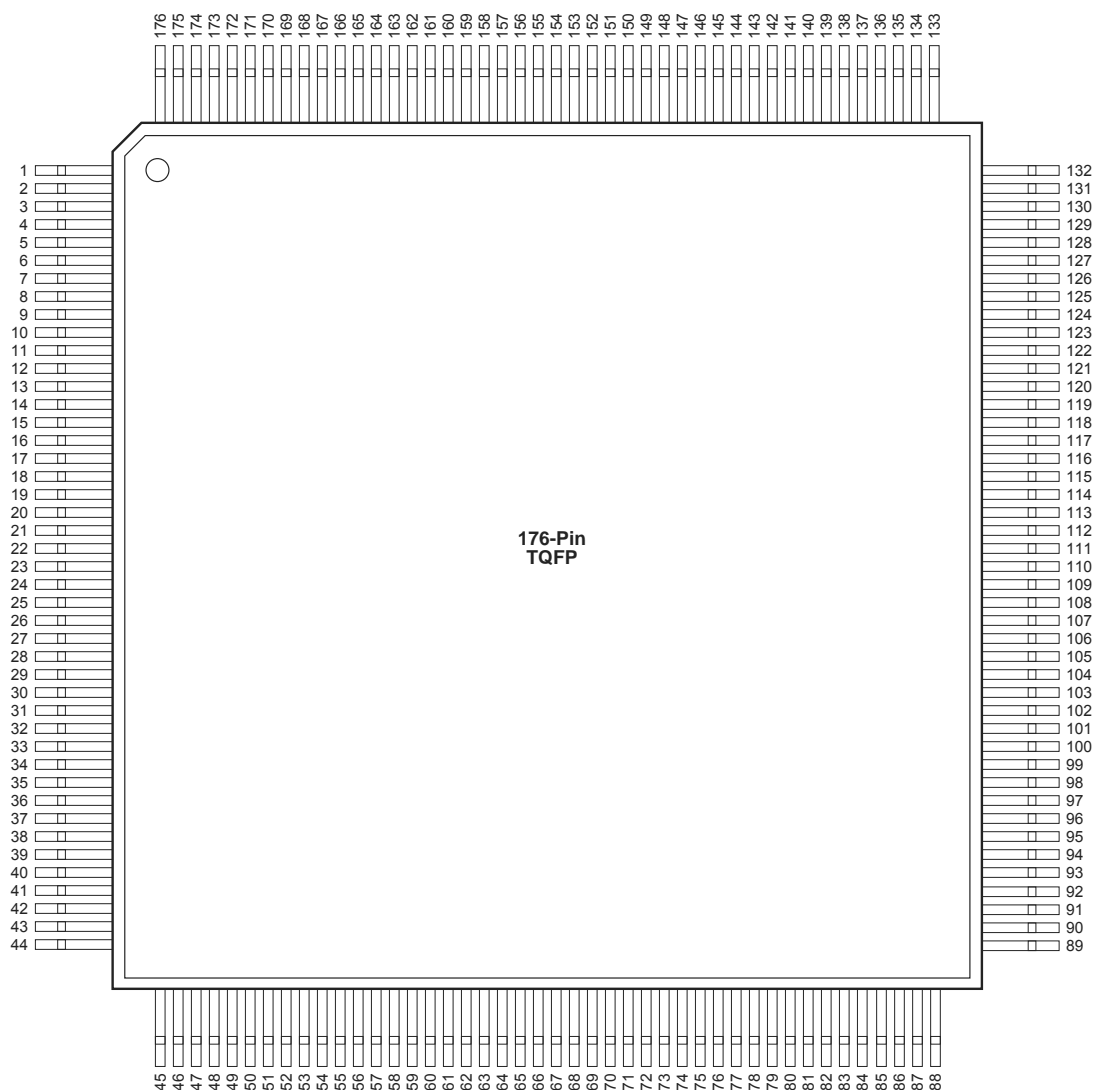
PQ160	
Pin Number	A1280A Function
2	DCLK, I/O
6	VCC
11	GND
16	PRB, I/O
18	CLKB, I/O
20	VCC
21	CLKA, I/O
23	PRA, I/O
30	GND
35	VCC
38	SDI, I/O
40	GND
44	GND
49	GND
54	VCC
57	VCC
58	VCC
59	GND
60	VCC
61	GND
64	GND

PQ160	
Pin Number	A1280A Function
69	GND
80	GND
82	SDO
86	VCC
89	GN
98	GND
99	GND
109	GND
114	VCC
120	GND
125	GND
130	GND
135	VCC
138	VCC
139	VCC
140	GND
145	GND
150	VCC
155	GND
159	MODE
160	GND

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

TQ176



Note

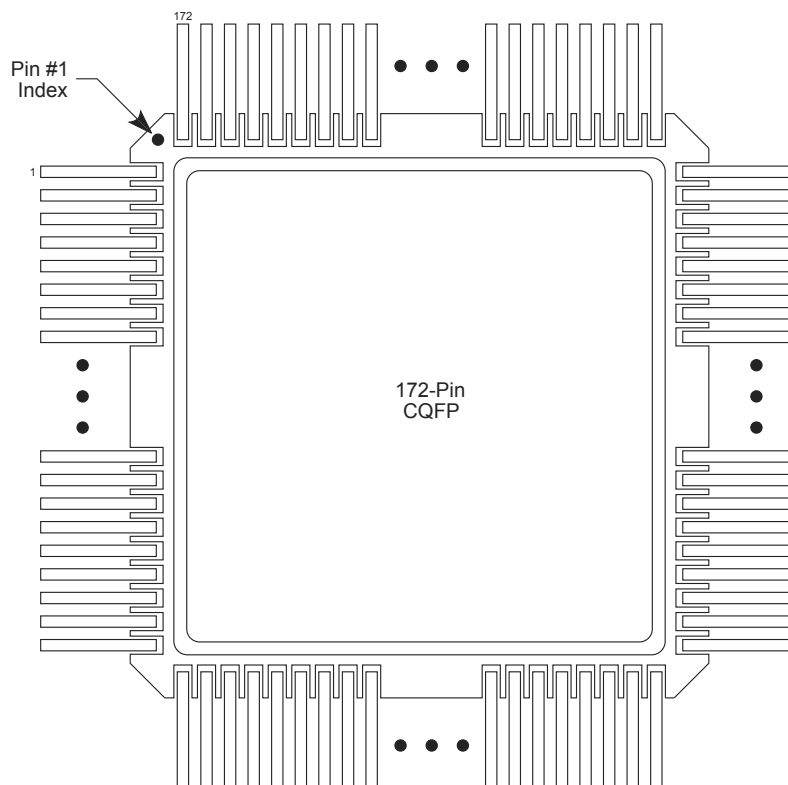
For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

TQ176		
Pin Number	A1240A Function	A1280A Function
155	VCC	VCC
156	GND	GND
158	CLKB, I/O	CLKB, I/O
160	PRB, I/O	PRB, I/O
161	NC	I/O
165	NC	NC
166	NC	I/O
168	NC	I/O
170	NC	VCC
173	NC	I/O
175	DCLK, I/O	DCLK, I/O

Notes:

1. NC denotes no connection.
2. All unlisted pin numbers are user I/Os.
3. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

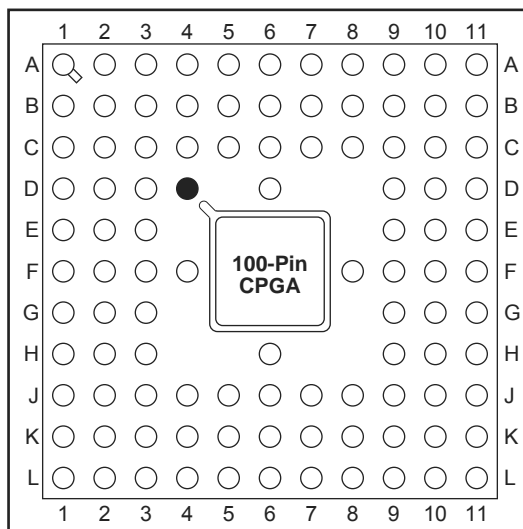
CQ172



Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

PG100



● Orientation Pin

Note

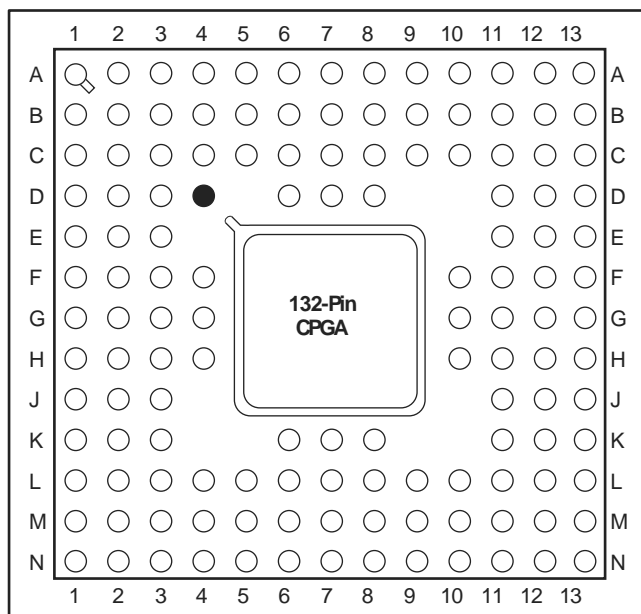
For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

PG100		PG100	
Pin Number	A1225A Function	Pin Number	A1225A Function
A4	PRB, I/O	E11	VCC
A7	PRA, I/O	F3	VCC
B6	VCC	F9	VCC
C2	MODE	F10	VCC
C3	DCLK, I/O	F11	GND
C5	GND	G1	VCC
C6	CLKA, I/O	G3	GND
C7	GND	G9	GND
C8	SDI, I/O	J5	GND
D6	CLKB, I/O	J7	GND
D10	GND	J9	SDO
E3	GND	K6	VCC

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG132



● Orientation Pin

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>



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