Microsemi Corporation - A1240A-TQ176C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	684
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	104
Number of Gates	4000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	176-LQFP
Supplier Device Package	176-TQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1240a-tq176c

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2 – Detailed Specifications

Operating Conditions

Table 2-1 • **Absolute Maximum Ratings[1]**

Symbol	Parameter	Limits	Units
VCC	DC supply voltage	–0.5 to +7.0	V
VI	Input voltage	–0.5 to VCC + 0.5	V
VO	Output voltage	–0.5 to VCC + 0.5	V
IIO	I/O source sink current[2]	±20	mA
T_{STG}	Storage temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND –0.5 V, the internal protection diodes will be forward biased and can draw excessive current.*

Table 2-2 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature range*	0 to +70	–40 to +85	–55 to +125	°C
Power supply tolerance	±5	±10	±10	%VCC

*Note: *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a PQ160 package at commercial temperature and still air is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}\text{°C/W}} = \frac{150\text{°C} - 70\text{°C}}{33\text{°C/W}} = 2.4\text{ W}$$

EQ 1

Table 2-4 • **Package Thermal Characteristics**

Package Type*	**Pin Count**	θ_{jc}	θ_{ja} **Still Air**	θ_{ja} **300 ft./min.**	**Units**
Ceramic Pin Grid Array	100	5	35	17	°C/W
	132	5	30	15	°C/W
	176	8	23	12	°C/W
Ceramic Quad Flatpack	172	8	25	15	°C/W
Plastic Quad Flatpack[1]	100	13	48	40	°C/W
	144	15	40	32	°C/W
	160	15	38	30	°C/W
Plastic Leaded Chip Carrier	84	12	37	28	°C/W
Very Thin Quad Flatpack	100	12	43	35	°C/W
Thin Quad Flatpack	176	15	32	25	°C/W

Notes: (Maximum Power in Still Air)

1. *Maximum power dissipation values for PQFP packages are 1.9 W (PQ100), 2.3 W (PQ144), and 2.4 W (PQ160).*
2. *Maximum power dissipation for PLCC packages is 2.7 W.*
3. *Maximum power dissipation for VQFP packages is 2.3 W.*
4. *Maximum power dissipation for TQFP packages is 3.1 W.*

Power Dissipation

P = [ICC standby + ICCactive] * VCC + IOL * VOL * N + IOH* (VCC – VOH) * M

EQ 2

where:

ICC standby is the current flowing when no inputs or outputs are changing

ICCactive is the current flowing due to CMOS switching.

IOL and IOH are TTL sink/source currents.

VOL and VOH are TTL level output voltages.

N is the number of outputs driving TTL loads to VOL.

M is the number of outputs driving TTL loads to VOH.

An accurate determination of N and M is problematical because their values depend on the family type, design details, and on the system I/O. The power can be divided into two components: static and active.

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. EQ 4 shows a piece-wise linear summation over all components.

$$\text{Power} = VCC^2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs}$$
$$+ (p * (C_{EQO} + C_L) * fp)_{outputs}$$
$$+ 0.5 * (q1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r1 * f_{q1})_{routed\_Clk1}$$
$$+ 0.5 * (q2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2}$$

EQ 4

Where:

m = Number of logic modules switching at f_m

n = Number of input buffers switching at f_n

p = Number of output buffers switching at f_p

q1 = Number of clock loads on the first routed array clock

q2 = Number of clock loads on the second routed array clock

r_1 = Fixed capacitance due to first routed array clock

r_2 = Fixed capacitance due to second routed array clock

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_L = Output lead capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz

f_{q2} = Average second routed array clock rate in MHz

Table 2-7 • **Fixed Capacitance Values for Microsemi FPGAs**

Device Type	r1, routed_Clk1	r2, routed_Clk2
A1225A	106	106.0
A1240A	134	134.2
A1280A	168	167.8

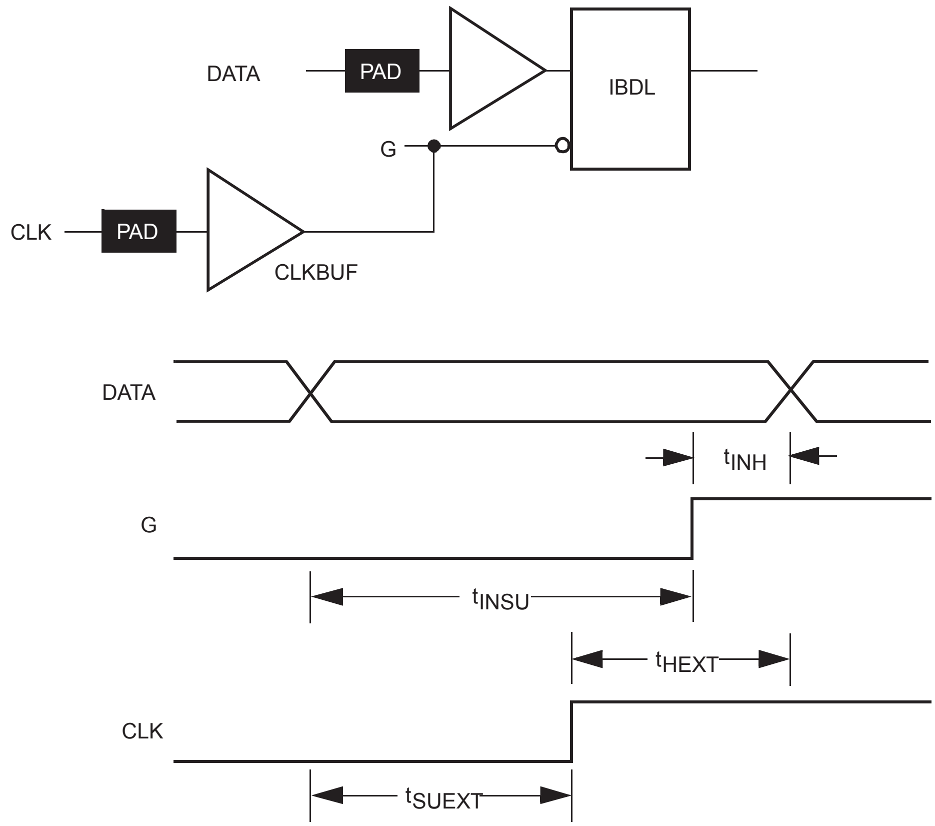


Figure 2-7 • **Input Buffer Latches**

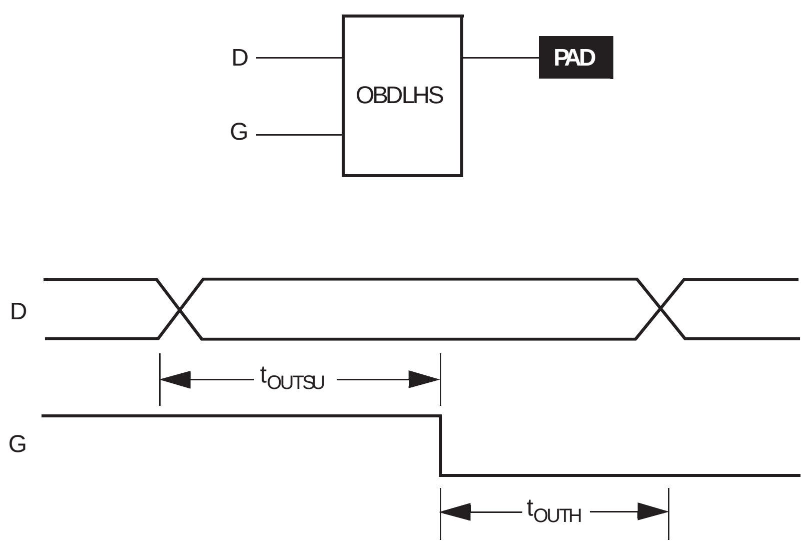


Figure 2-8 • **Output Buffer Latches**

A1225A Timing Characteristics

***Table 2-12* • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

Logic Module Propagation Delays[1]		**–2 Speed**[3]		**–1 Speed**		**Std. Speed**		**Units**
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{PD1}	Single Module		3.8		4.3		5.0	ns
t_{CO}	Sequential Clock to Q		3.8		4.3		5.0	ns
t_{GO}	Latch G to Q		3.8		4.3		5.0	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		3.8		4.3		5.0	ns
Predicted Routing Delays[2]								
t_{RD1}	FO = 1 Routing Delay		1.1		1.2		1.4	ns
t_{RD2}	FO = 2 Routing Delay		1.7		1.9		2.2	ns
t_{RD3}	FO = 3 Routing Delay		2.3		2.6		3.0	ns
t_{RD4}	FO = 4 Routing Delay		2.8		3.1		3.7	ns
t_{RD8}	FO = 8 Routing Delay		4.4		4.9		5.8	ns
Sequential Timing Characteristics[3,4]								
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.5		5.0		6.0		ns
t_{WASYN}	Flip-Flop (Latch) Clock Asynchronous Pulse Width	4.5		5.0		6.0		ns
t_A	Flip-Flop Clock Input Period	9.4		11.0		13.0		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.4		0.4		0.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.4		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		105.0		90.0		75.0	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$—whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A1240A Timing Characteristics (continued)

***Table 2-16* • A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

I/O Module Input Propagation Delays			–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description			**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{INYH}	Pad to Y High			2.9		3.3		3.8	ns
t_{INYL}	Pad to Y Low			2.6		3.0		3.5	ns
t_{INGH}	G to Y High			5.0		5.7		6.6	ns
t_{INGL}	G to Y Low			4.7		5.4		6.3	ns
Input Module Predicted Input Routing Delays*									
t_{IRD1}	FO = 1 Routing Delay			4.2		4.8		5.6	ns
t_{IRD2}	FO = 2 Routing Delay			4.8		5.4		6.4	ns
t_{IRD3}	FO = 3 Routing Delay			5.4		6.1		7.2	ns
t_{IRD4}	FO = 4 Routing Delay			5.9		6.7		7.9	ns
t_{IRD8}	FO = 8 Routing Delay			7.9		8.9		10.5	ns
Global Clock Network									
t_{CKH}	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		11.8		13.0		15.7	
t_{CKL}	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		12.0		13.2		15.9	
t_{PWH}	Minimum Pulse Width High	FO = 32	3.8		4.5		5.5		ns
		FO = 256	4.1		5.0		5.8		
t_{PWL}	Minimum Pulse Width Low	FO = 32	3.8		4.5		5.5		ns
		FO = 256	4.1		5.0		5.8		
t_{CKSW}	Maximum Skew	FO = 32		0.5		0.5		0.5	ns
		FO = 256		2.5		2.5		2.5	
t_{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t_{HEXT}	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t_P	Minimum Period	FO = 32	8.1		9.1		11.1		ns
		FO = 256	8.8		10.0		11.7		
f_{MAX}	Maximum Frequency	FO = 32		125.0		110.0		90.0	ns
		FO = 256		115.0		100.0		85.0	

Note: **These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1280A Timing Characteristics (continued)

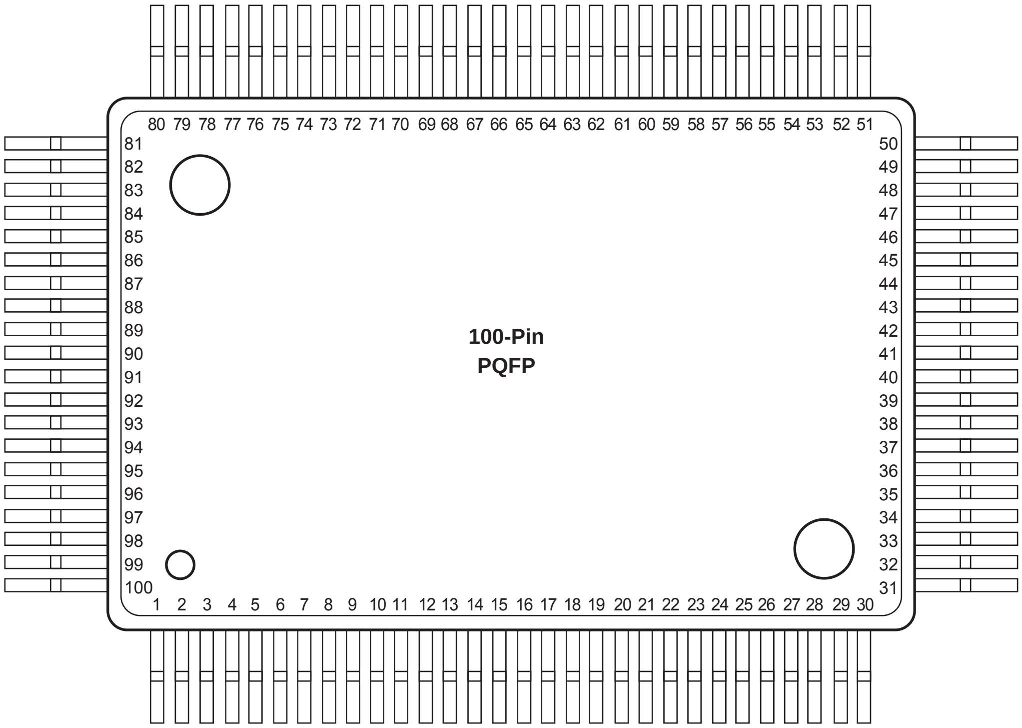
Table 2-19 **• A1280A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

I/O Module Input Propagation Delays			–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description			**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{INYH}	Pad to Y High			2.9		3.3		3.8	ns
t_{INYL}	Pad to Y Low			2.7		3.0		3.5	ns
t_{INGH}	G to Y High			5.0		5.7		6.6	ns
t_{INGL}	G to Y Low			4.8		5.4		6.3	ns
Input Module Predicted Input Routing Delays*									
t_{IRD1}	FO = 1 Routing Delay			4.6		5.1		6.0	ns
t_{IRD2}	FO = 2 Routing Delay			5.2		5.9		6.9	ns
t_{IRD3}	FO = 3 Routing Delay			5.6		6.3		7.4	ns
t_{IRD4}	FO = 4 Routing Delay			6.5		7.3		8.6	ns
t_{IRD8}	FO = 8 Routing Delay			9.4		10.5		12.4	ns
Global Clock Network									
t_{CKH}	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		13.1		14.6		17.2	
t_{CKL}	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		13.3		14.9		17.5	
t_{PWH}	Minimum Pulse Width High	FO = 32	5.0		5.5		6.6		ns
		FO = 256	5.8		6.4		7.6		
t_{PWL}	Minimum Pulse Width Low	FO = 32	5.0		5.5		6.6		ns
		FO = 256	5.8		6.4		7.6		
t_{CKSW}	Maximum Skew	FO = 32		0.5		0.5		0.5	ns
		FO = 256		2.5		2.5		2.5	
t_{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t_{HEXT}	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t_P	Minimum Period	FO = 32	9.6		11.2		13.3		ns
		FO = 256	10.6		12.6		15.3		
f_{MAX}	Maximum Frequency	FO = 32		105.0		90.0		75.0	ns
		FO = 256		95.0		80.0		65.0	

Note: **These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1280A Timing Characteristics (continued)

PQ100



Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

PQ100	
Pin Number	A1225A Function
2	DCLK, I/O
4	MODE
9	GND
16	VCC
17	VCC
22	GND
34	GND
40	VCC
46	GND
52	SDO
57	GND
64	GND

PQ100	
Pin Number	A1225A Function
65	VCC
66	VCC
67	VCC
72	GND
79	SDI, I/O
84	GND
87	PRA, I/O
89	CLKA, I/O
90	VCC
92	CLKB, I/O
94	PRB, I/O
96	GND

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

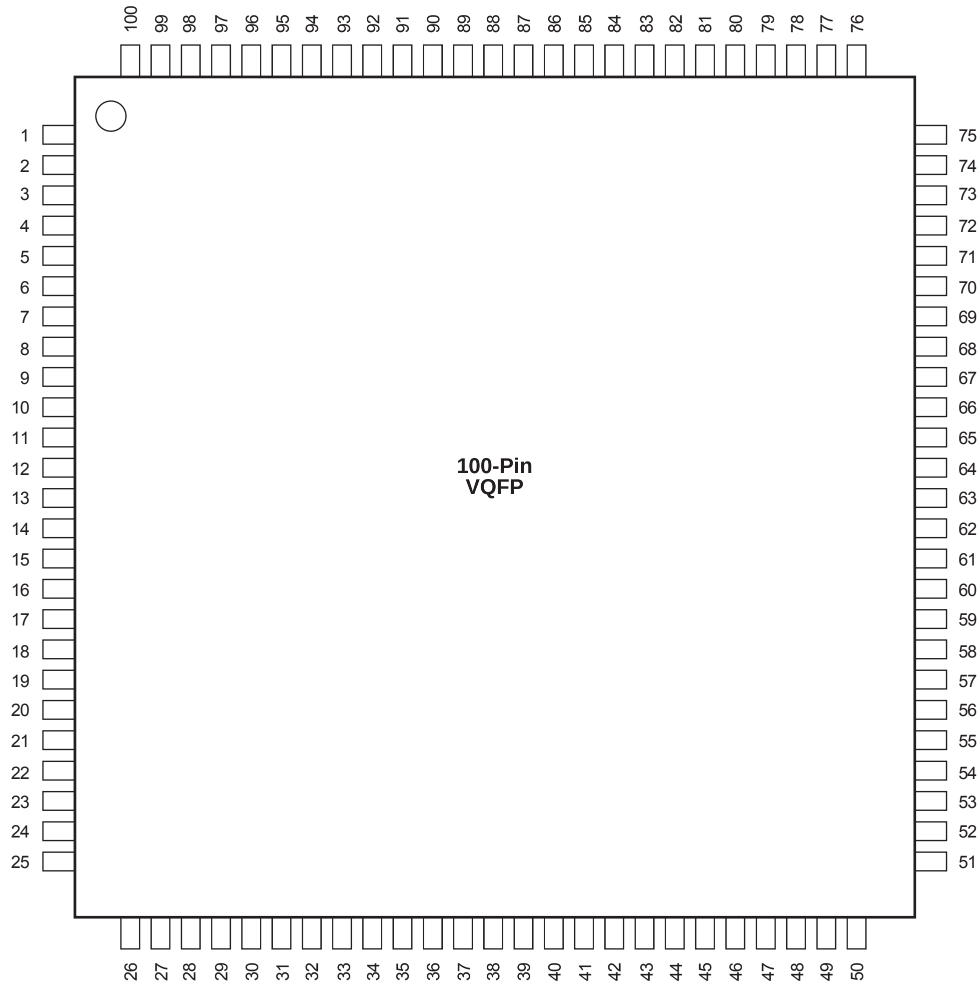
PQ160	
Pin Number	**A1280A Function**
2	DCLK, I/O
6	VCC
11	GND
16	PRB, I/O
18	CLKB, I/O
20	VCC
21	CLKA, I/O
23	PRA, I/O
30	GND
35	VCC
38	SDI, I/O
40	GND
44	GND
49	GND
54	VCC
57	VCC
58	VCC
59	GND
60	VCC
61	GND
64	GND

PQ160	
Pin Number	**A1280A Function**
69	GND
80	GND
82	SDO
86	VCC
89	GN
98	GND
99	GND
109	GND
114	VCC
120	GND
125	GND
130	GND
135	VCC
138	VCC
139	VCC
140	GND
145	GND
150	VCC
155	GND
159	MODE
160	GND

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

VQ100



Note

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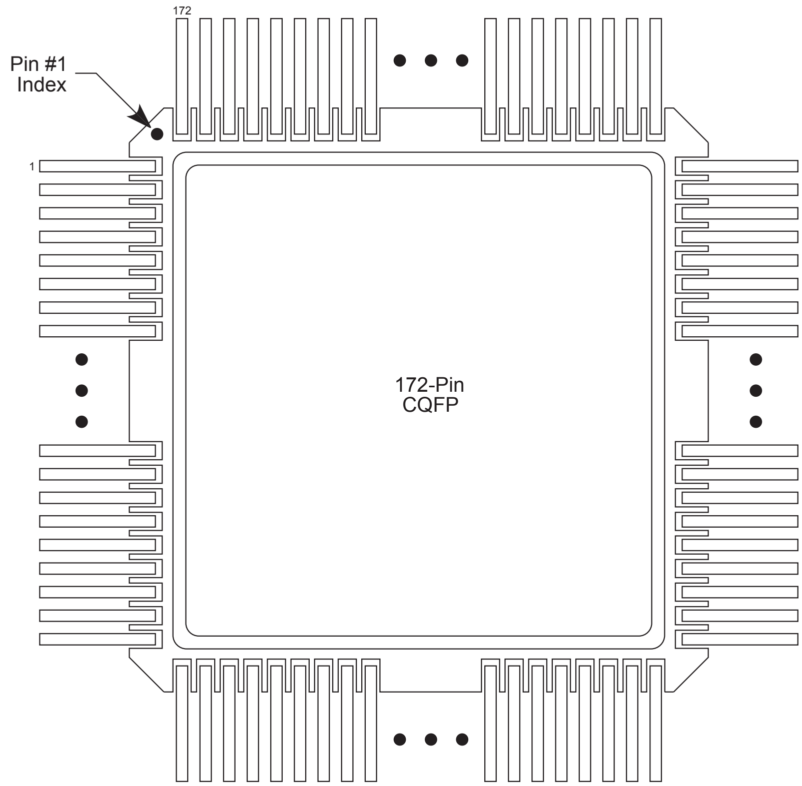
VQ100	
Pin Number	A1225A Function
2	MODE
7	GND
14	VCC
15	VCC
20	GND
32	GND
38	VCC
44	GND
50	SDO
55	GND
62	GND
63	VCC

VQ100	
Pin Number	A1225A Function
64	VCC
65	VCC
70	GND
77	SDI, I/O
82	GND
85	PRA, I/O
87	CLKA, I/O
88	VCC
90	CLKB, I/O
92	PRB, I/O
94	GND
100	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

CQ172



Note

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http://www.microsemi.com/soc/products/solutions/package/docs.aspx

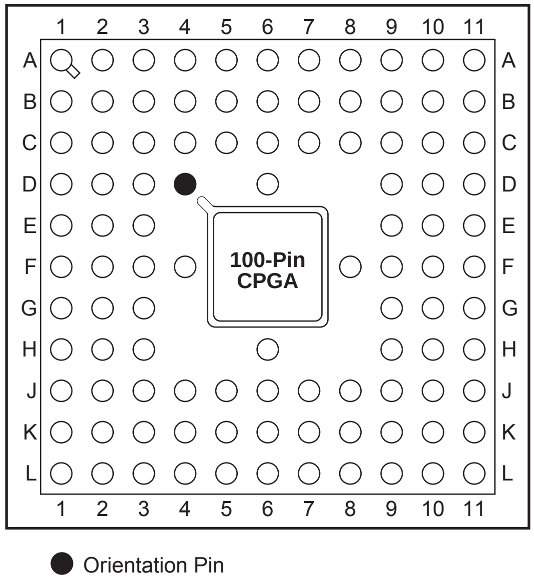
CQ172	
Pin Number	**A1280A Function**
1	MODE
7	GND
12	VCC
17	GND
22	GND
23	VCC
24	VCC
27	VCC
32	GND
37	GND
50	VCC
55	GND
65	GND
66	VCC
75	GND
80	VCC
85	SDO
98	GND
103	GND
106	GND

CQ172	
Pin Number	**A1280A Function**
107	VCC
108	GND
109	VCC
110	VCC
113	VCC
118	GND
123	GND
131	SDI, I/O
136	VCC
141	GND
148	PRA, I/O
150	CLKA, I/O
151	VCC
152	GND
154	CLKB, I/O
156	PRB, I/O
161	GND
166	VCC
171	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG100



Note

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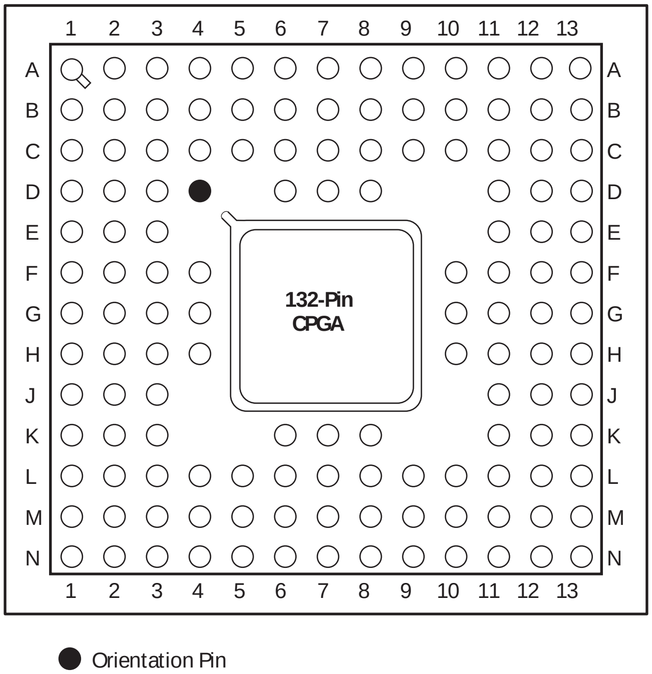
PG100		PG100	
Pin Number	**A1225A Function**	**Pin Number**	**A1225A Function**
A4	PRB, I/O	E11	VCC
A7	PRA, I/O	F3	VCC
B6	VCC	F9	VCC
C2	MODE	F10	VCC
C3	DCLK, I/O	F11	GND
C5	GND	G1	VCC
C6	CLKA, I/O	G3	GND
C7	GND	G9	GND
C8	SDI, I/O	J5	GND
D6	CLKB, I/O	J7	GND
D10	GND	J9	SDO
E3	GND	K6	VCC

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG132



Note

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Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

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The products described in this advance status document may not have completed the Microsemi qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the Microsemi SoC Products Group Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the SoC Products Group's products is available at http://www.microsemi.com/soc/documents/ORT_Report.pdf. Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local sales office for additional reliability information.