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Understanding Embedded - FPGAs (Field Programmable Gate Array)

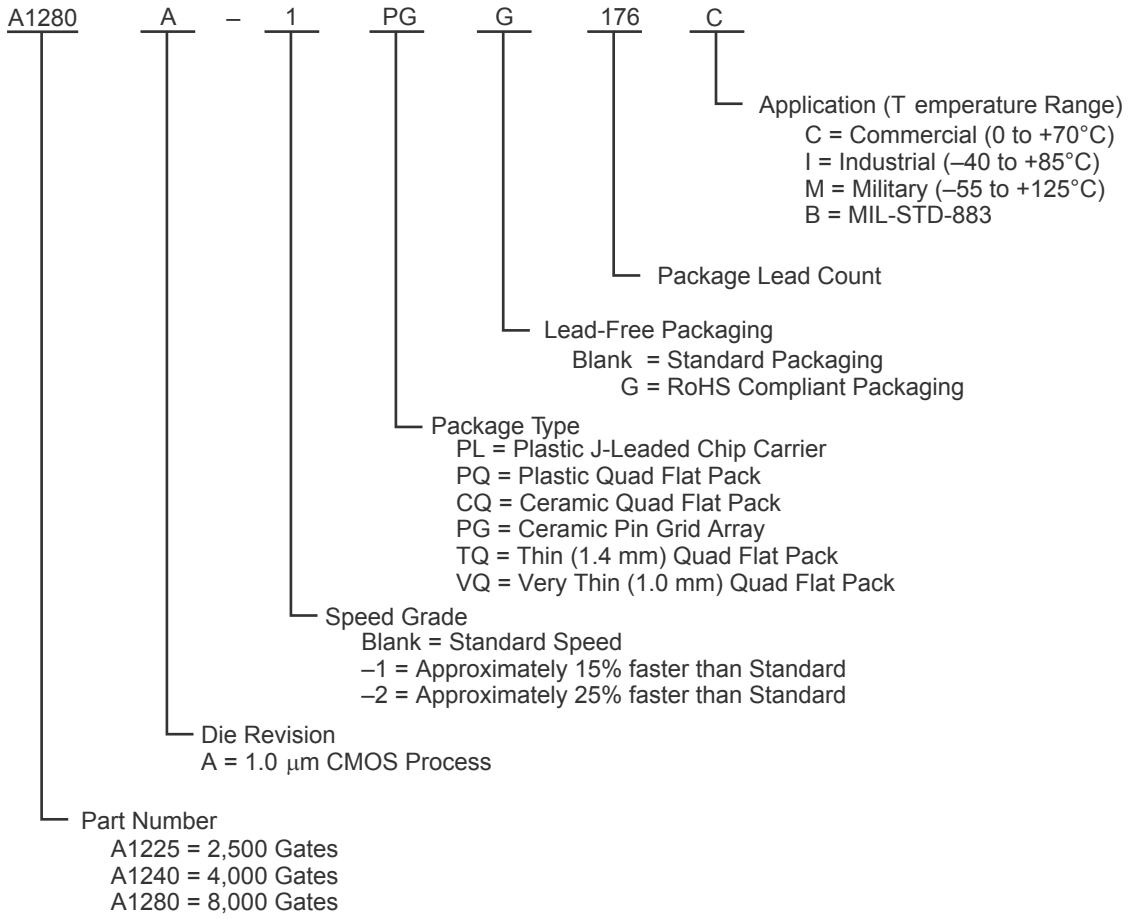
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	140
Number of Gates	8000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	172-CQFP with Tie Bar
Supplier Device Package	172-CQFP (63.37x63.37)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1280a-1cq172m

Ordering Information



Product Plan

Device/Package	Speed Grade[1]			Application[1]			
	Std.	–1	–2	C	I	M	B
A1225A Device							
84-Pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–
100-Pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	✓	–	–
100-Pin Very Thin Quad Flatpack (VQ)	✓	✓	✓	✓	–	–	–
100-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	–	–	–
A1240A Device							
84-Pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–
132-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	–	✓	✓
144-Pin Plastic Quad Flat Pack (PQ)	✓	✓	✓	✓	✓	–	–
176-Pin Thin (1.4 mm) Quad Flat Pack (TQ)	✓	✓	✓	✓	–	–	–
A1280A Device							
160-Pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	✓	–	–
172-Pin Ceramic Quad Flatpack (CQ)	✓	✓	✓	✓	–	✓	✓
176-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	–	✓	✓
176-Pin Thin (1.4 mm) Quad Flat Pack (TQ)	✓	✓	✓	✓	–	–	–

Notes:

1. *Applications:*
   C = Commercial
   I = Industrial
   M = Military
   B = MIL-STD-883

   Availability:
   ✓ = Available
   P = Planned
   – = Not planned

   Speed Grade:
   –1 = Approx. 15% faster than Std.
   –2 = Approx. 25% faster than Std.

2. *Contact your Microsemi SoC Products Group sales representative for product availability.*

Device Resources

Device Series	Logic Modules	Gates	User I/Os									
			PG176	PG132	PG100	PQ160	PQ144	PQ100	PL84	CQ172	TQ176	VQ100
A1225A	451	2,500	–	–	83	–	–	83	72	–	–	83
A1240A	684	4,000	–	104	–	–	104	–	72	–	104	–
A1280A	1,232	8,000	140	–	–	125	–	–	72	140	140	–

Contact your local Microsemi SoC Products Group representative for device availability:
http://www.microsemi.com/soc/contact/default.aspx.

1 – ACT 2 Family Overview

General Description

The ACT 2 family represents Actel's second generation of field programmable gate arrays (FPGAs). The ACT 2 family presents a two-module architecture, consisting of C-modules and S-modules. These modules are optimized for both combinatorial and sequential designs. Based on Actel's patented channeled array architecture, the ACT 2 family provides significant enhancements to gate density and performance while maintaining downward compatibility with the ACT 1 design environment and upward compatibility with the ACT 3 design environment. The devices are implemented in silicon gate, 1.0-µm, two-level metal CMOS, and employ Actel's PLICE® antifuse technology. This revolutionary architecture offers gate array design flexibility, high performance, and fast time-to-production with user programming. The ACT 2 family is supported by the Designer and Designer Advantage Systems, which offers automatic pin assignment, validation of electrical and design rules, automatic placement and routing, timing analysis, user programming, and diagnostic probe capabilities. The systems are supported on the following platforms: 386/486™ PC, Sun™, and HP™ workstations. The systems provide CAE interfaces to the following design environments: Cadence, Viewlogic®, Mentor Graphics®, and OrCAD™.

2 – Detailed Specifications

Operating Conditions

Table 2-1 • **Absolute Maximum Ratings[1]**

Symbol	Parameter	Limits	Units
VCC	DC supply voltage	–0.5 to +7.0	V
VI	Input voltage	–0.5 to VCC + 0.5	V
VO	Output voltage	–0.5 to VCC + 0.5	V
IIO	I/O source sink current[2]	±20	mA
T_{STG}	Storage temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND –0.5 V, the internal protection diodes will be forward biased and can draw excessive current.*

Table 2-2 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature range*	0 to +70	–40 to +85	–55 to +125	°C
Power supply tolerance	±5	±10	±10	%VCC

*Note: *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Table 2-3 • **Electrical Specifications**

Symbol	Parameter	Commercial		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
VOH[1]	(IOH = –10 mA)[2]	2.4	–	–	–	–	–	V
	(IOH = –6 mA)	3.84	–	–	–	–	–	V
	(IOH = –4 mA)	–	–	3.7	–	3.7	–	V
VOL[1]	(IOL = 10 mA)[2]	–	0.5	–	–	–	–	V
	(IOL = 6 mA)	–	0.33	–	0.40	–	0.40	V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
Input Transition Time t_R, t_F[2]		–	500	–	500	–	500	ns
C_{IO} I/O capacitance[2,3]		–	10	–	10	–	10	pF
Standby Current, ICC[4] (typical = 1 mA)		–	2	–	10	–	20	mA
Leakage Current[5]		–10	+10	–10	+10	–10	+10	µA
ICC(D)	Dynamic VCC supply current. See the Power Dissipation section.							

Notes:

1. *Only one output tested at a time. VCC = minimum.*
2. *Not tested, for information only.*
3. *Includes worst-case PG176 package capacitance. VOUT = 0 V, f = 1 MHz*
4. *All outputs unloaded. All inputs = VCC or GND, typical ICC = 1 mA. ICC limit includes IPP and ISV during normal operations.*
5. *VOUT, VIN = VCC or GND.*

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a PQ160 package at commercial temperature and still air is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}\text{°C/W}} = \frac{150\text{°C} - 70\text{°C}}{33\text{°C/W}} = 2.4\ \text{W}$$

EQ 1

Table 2-4 • **Package Thermal Characteristics**

Package Type*	**Pin Count**	θ_{jc}	θ_{ja} **Still Air**	θ_{ja} **300 ft./min.**	**Units**
Ceramic Pin Grid Array	100	5	35	17	°C/W
	132	5	30	15	°C/W
	176	8	23	12	°C/W
Ceramic Quad Flatpack	172	8	25	15	°C/W
Plastic Quad Flatpack[1]	100	13	48	40	°C/W
	144	15	40	32	°C/W
	160	15	38	30	°C/W
Plastic Leaded Chip Carrier	84	12	37	28	°C/W
Very Thin Quad Flatpack	100	12	43	35	°C/W
Thin Quad Flatpack	176	15	32	25	°C/W

Notes: (Maximum Power in Still Air)

1. *Maximum power dissipation values for PQFP packages are 1.9 W (PQ100), 2.3 W (PQ144), and 2.4 W (PQ160).*
2. *Maximum power dissipation for PLCC packages is 2.7 W.*
3. *Maximum power dissipation for VQFP packages is 2.3 W.*
4. *Maximum power dissipation for TQFP packages is 3.1 W.*

Power Dissipation

$$P = [I_{CC\ standby} + I_{CCactive}] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M$$

EQ 2

where:

$I_{CC\ standby}$ is the current flowing when no inputs or outputs are changing

$I_{CCactive}$ is the current flowing due to CMOS switching.

I_{OL} and I_{OH} are TTL sink/source currents.

V_{OL} and V_{OH} are TTL level output voltages.

N is the number of outputs driving TTL loads to V_{OL}.

M is the number of outputs driving TTL loads to V_{OH}.

An accurate determination of N and M is problematical because their values depend on the family type, design details, and on the system I/O. The power can be divided into two components: static and active.

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are given in Table 2-8.

Table 2-8 • **Guidelines for Predicting Power Dissipation**

Data	Value
Logic Modules (m)	80% of modules
Inputs switching (n)	# inputs/4
Outputs switching (p)	# output/4
First routed array clock loads (q1)	40% of sequential modules
Second routed array clock loads (q2)	40% of sequential modules
Load capacitance (C_L)	35 pF
Average logic module switching rate (f_m)	F/10
Average input switching rate (f_n)	F/5
Average output switching rate (f_p)	F/10
Average first routed array clock rate (f_{q1})	F
Average second routed array clock rate (f_{q2})	F/2

Parameter Measurement

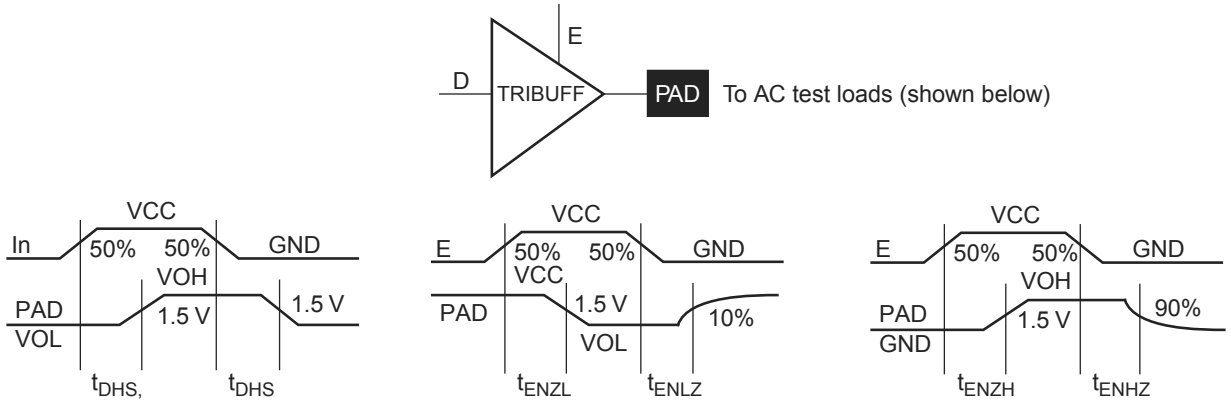


Figure 2-2 • **Output Buffer Delays**

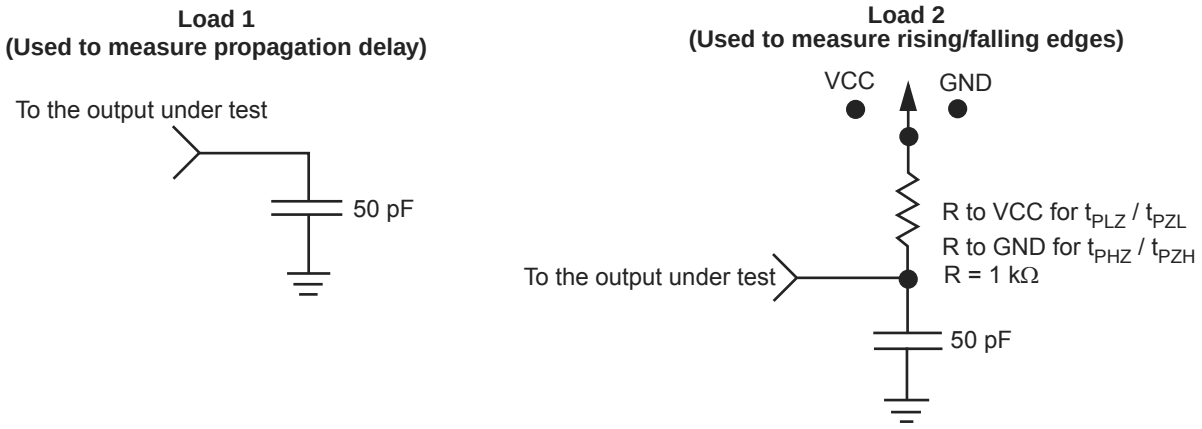


Figure 2-3 • **AC Test Loads**

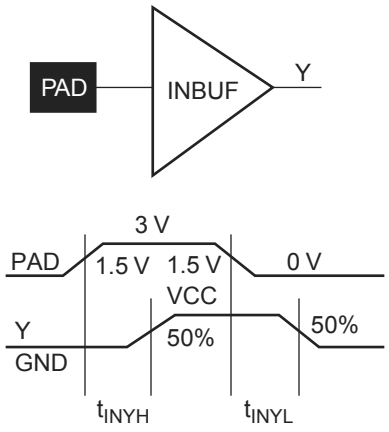


Figure 2-4 • **Input Buffer Delays**

A1225A Timing Characteristics (continued)

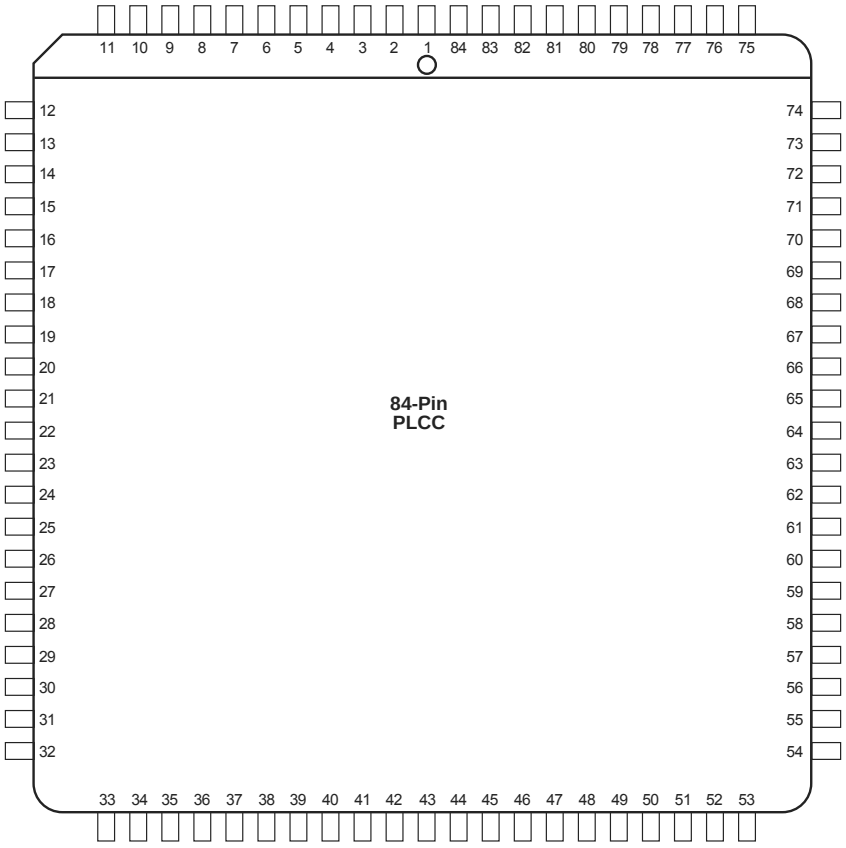
***Table 2-13* • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

I/O Module Input Propagation Delays			–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description			**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{INYH}	Pad to Y High			2.9		3.3		3.8	ns
t_{INYL}	Pad to Y Low			2.6		3.0		3.5	ns
t_{INGH}	G to Y High			5.0		5.7		6.6	ns
t_{INGL}	G to Y Low			4.7		5.4		6.3	ns
Input Module Predicted Input Routing Delays*									
t_{IRD1}	FO = 1 Routing Delay			4.1		4.6		5.4	ns
t_{IRD2}	FO = 2 Routing Delay			4.6		5.2		6.1	ns
t_{IRD3}	FO = 3 Routing Delay			5.3		6.0		7.1	ns
t_{IRD4}	FO = 4 Routing Delay			5.7		6.4		7.6	ns
t_{IRD8}	FO = 8 Routing Delay			7.4		8.3		9.8	ns
Global Clock Network									
t_{CKH}	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		11.8		13.0		15.7	
t_{CKL}	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		12.0		13.2		15.9	
t_{PWH}	Minimum Pulse Width High	FO = 32	3.4		4.1		4.5		ns
		FO = 256	3.8		4.5		5.0		
t_{PWL}	Minimum Pulse Width Low	FO = 32	3.4		4.1		4.5		ns
		FO = 256	3.8		4.5		5.0		
t_{CKSW}	Maximum Skew	FO = 32		0.7		0.7		0.7	ns
		FO = 256		3.5		3.5		3.5	
t_{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t_{HEXT}	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t_P	Minimum Period	FO = 32	7.7		8.3		9.1		ns
		FO = 256	8.1		8.8		10.0		
f_{MAX}	Maximum Frequency	FO = 32		130.0		120.0		110.0	ns
		FO = 256		125.0		115.0		100.0	

*Note: *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

3 – Package Pin Assignments

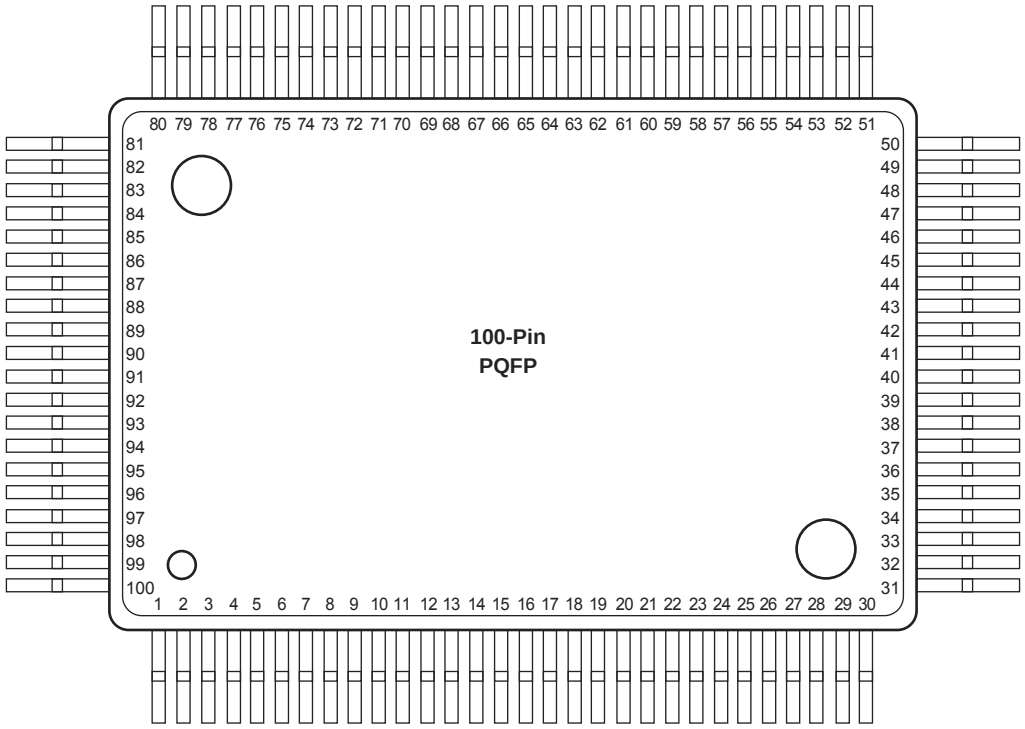
PL84



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

PQ100



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

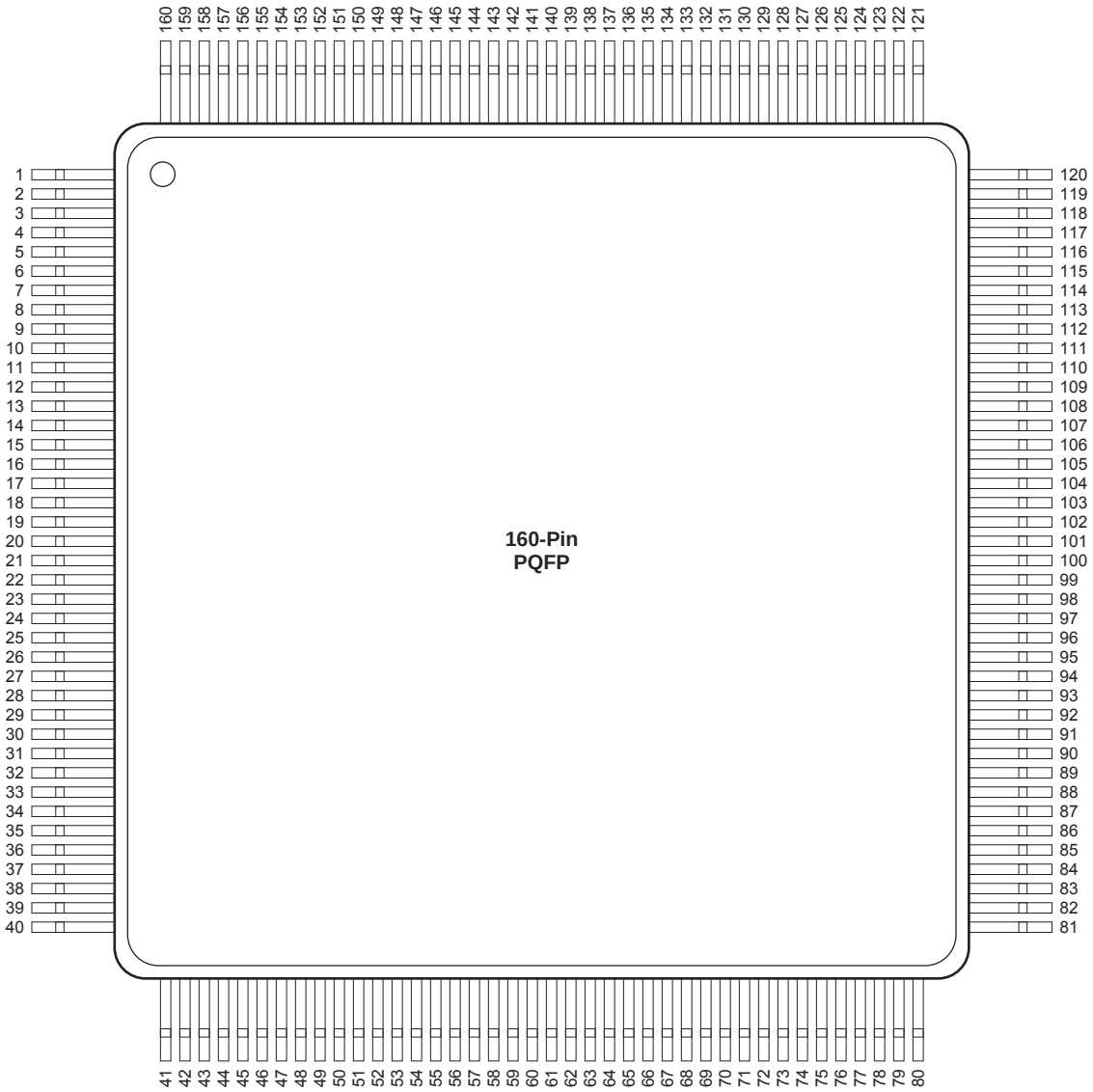
PQ144	
Pin Number	**A1240A Function**
2	MODE
9	GND
10	GND
11	GND
18	VCC
19	VCC
20	VCC
21	VCC
28	GND
29	GND
30	GND
44	GND
45	GND
46	GND
54	VCC
55	VCC
56	VCC
64	GND
65	GND
71	SDO
79	GND
80	GND
81	GND
88	GND

PQ144	
Pin Number	**A1240A Function**
89	VCC
90	VCC
91	VCC
92	VCC
93	VCC
100	GND
101	GND
102	GND
110	SDI, I/O
116	GND
117	GND
118	GND
123	PRA, I/O
125	CLKA, I/O
126	VCC
127	VCC
128	VCC
130	CLKB, I/O
132	PRB, I/O
136	GND
137	GND
138	GND
144	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PQ160

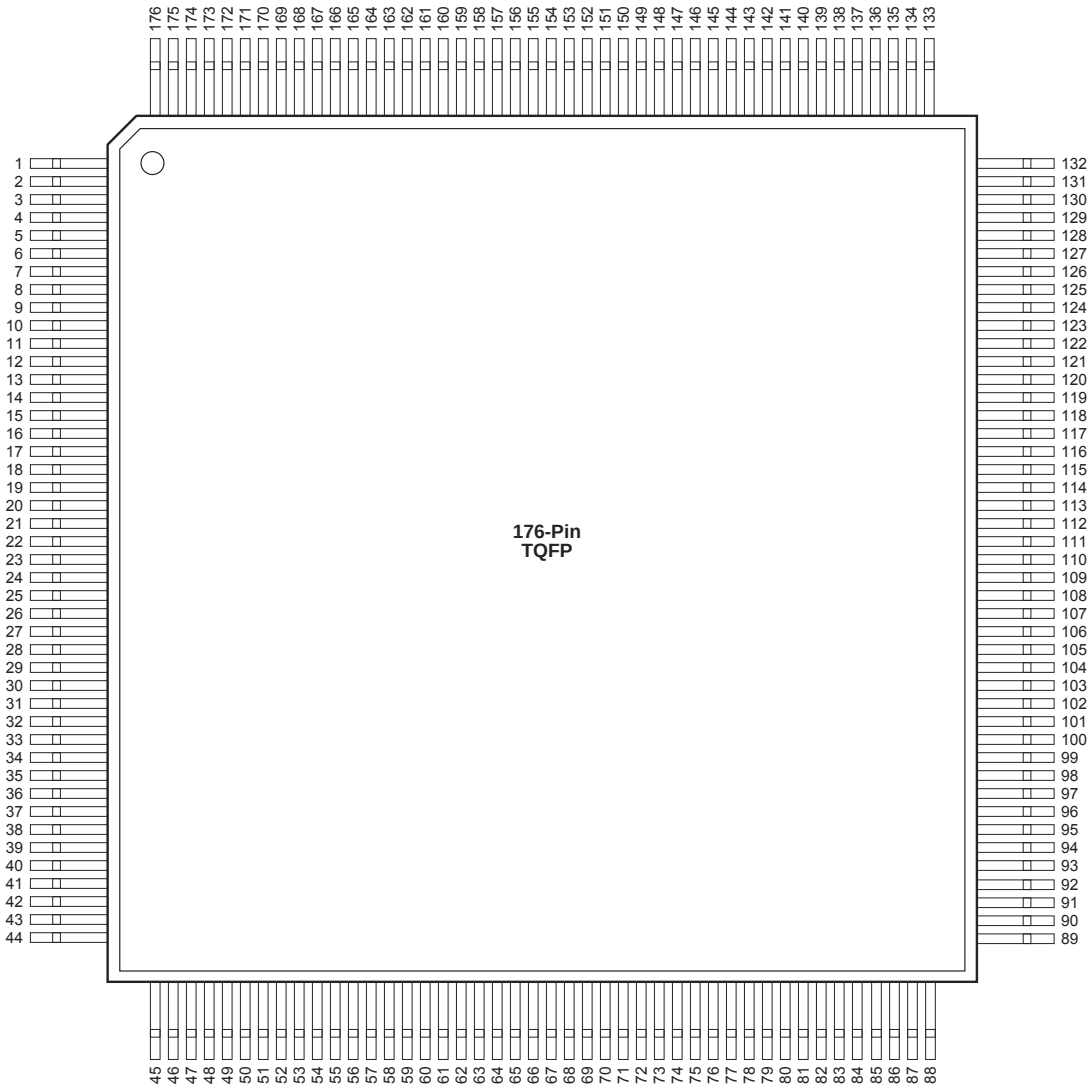


Note: This is the top view of the package

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

TQ176



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

TQ176		
Pin Number	**A1240A Function**	**A1280A Function**
1	GND	GND
2	MODE	MODE
8	NC	NC
10	NC	I/O
11	NC	I/O
13	NC	VCC
18	GND	GND
19	NC	I/O
20	NC	I/O
22	NC	I/O
23	GND	GND
24	NC	VCC
25	VCC	VCC
26	NC	I/O
27	NC	I/O
28	VCC	VCC
29	NC	I/O
33	NC	NC
37	NC	I/O
38	NC	NC
45	GND	GND
52	NC	VCC
54	NC	I/O
55	NC	I/O
57	NC	NC
61	NC	I/O
64	NC	I/O
66	NC	I/O
67	GND	GND
68	VCC	VCC
74	NC	I/O
77	NC	NC
78	NC	I/O
80	NC	I/O

TQ176		
Pin Number	**A1240A Function**	**A1280A Function**
82	NC	VCC
86	NC	I/O
87	SDO	SDO
89	GND	GND
96	NC	I/O
97	NC	I/O
101	NC	NC
103	NC	I/O
106	GND	GND
107	NC	I/O
108	NC	I/O
109	GND	GND
110	VCC	VCC
111	GND	GND
112	VCC	VCC
113	VCC	VCC
114	NC	I/O
115	NC	I/O
116	NC	VCC
121	NC	NC
124	NC	I/O
125	NC	I/O
126	NC	NC
133	GND	GND
135	SDI, I/O	SDI, I/O
136	NC	I/O
140	NC	VCC
143	NC	I/O
144	NC	I/O
145	NC	NC
147	NC	I/O
151	NC	I/O
152	PRA, I/O	PRA, I/O
154	CLKA, I/O	CLKA, I/O

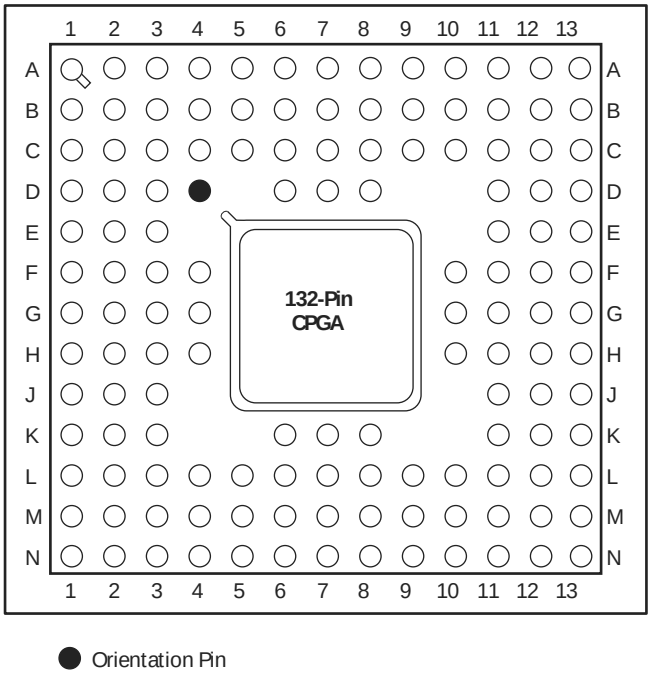
PG100	
Pin Number	**A1225A Function**
A4	PRB, I/O
A7	PRA, I/O
B6	VCC
C2	MODE
C3	DCLK, I/O
C5	GND
C6	CLKA, I/O
C7	GND
C8	SDI, I/O
D6	CLKB, I/O
D10	GND
E3	GND

PG100	
Pin Number	**A1225A Function**
E11	VCC
F3	VCC
F9	VCC
F10	VCC
F11	GND
G1	VCC
G3	GND
G9	GND
J5	GND
J7	GND
J9	SDO
K6	VCC

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG132



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

4 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each version of the datasheet.

Revision	Changes	Page
Revision 8 (January 2012)	The ACT 2 datasheet was formatted newly in the style used for current datasheets. The same information is present (other than noted in the list of changes for this revision) but divided into chapters.	N/A
	Package names used in Table 1 • ACT 2 Product Family Profile and throughout the document were revised to match standards given in *Package Mechanical Drawings* (SAR 27395).	I
	The description for SDO pins had earlier been removed from the datasheet and has now been included again, in the "Pin Descriptions" section (SAR 35819).	2-21
	SDO pin numbers had earlier been removed from package pin assignment tables in the datasheet, and have now been restored to the pin tables (SAR 35819).	3-2
Revision 7 (June 2006)	The "Ordering Information" section was revised to include RoHS information.	II
Revision 6 (December 2000)	In the "PG176" package, pin A3 was incorrectly assigned as CLKA, I/O. A3 is a user I/O. Pin A9 is CLKA, I/O.	3-21

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