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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	140
Number of Gates	8000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Through Hole
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	176-BCPGA
Supplier Device Package	176-CPGA (39.88x39.88)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microsemi/a1280a-1pg176b">https://www.e-xfl.com/product-detail/microsemi/a1280a-1pg176b</a>

## Ordering Information





## Static Power Component

Microsemi FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated in Table 2-5 for commercial, worst case conditions.

**Table 2-5 • Standby Power Calculation**

ICC	VCC	Power
2 mA	5.25 V	10.5 mW

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

## Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs.

An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

## Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by EQ 3.

$$\text{Power } (\mu\text{W}) = C_{\text{EQ}} * V_{\text{CC}}^2 * F$$

EQ 3

Where:

$C_{\text{EQ}}$  is the equivalent capacitance expressed in pF.

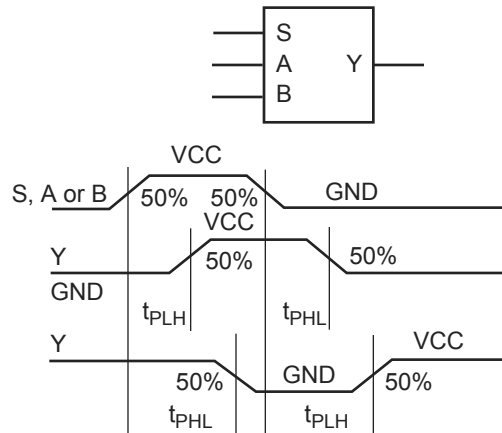
VCC is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring ICC active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown in Table 2-6.

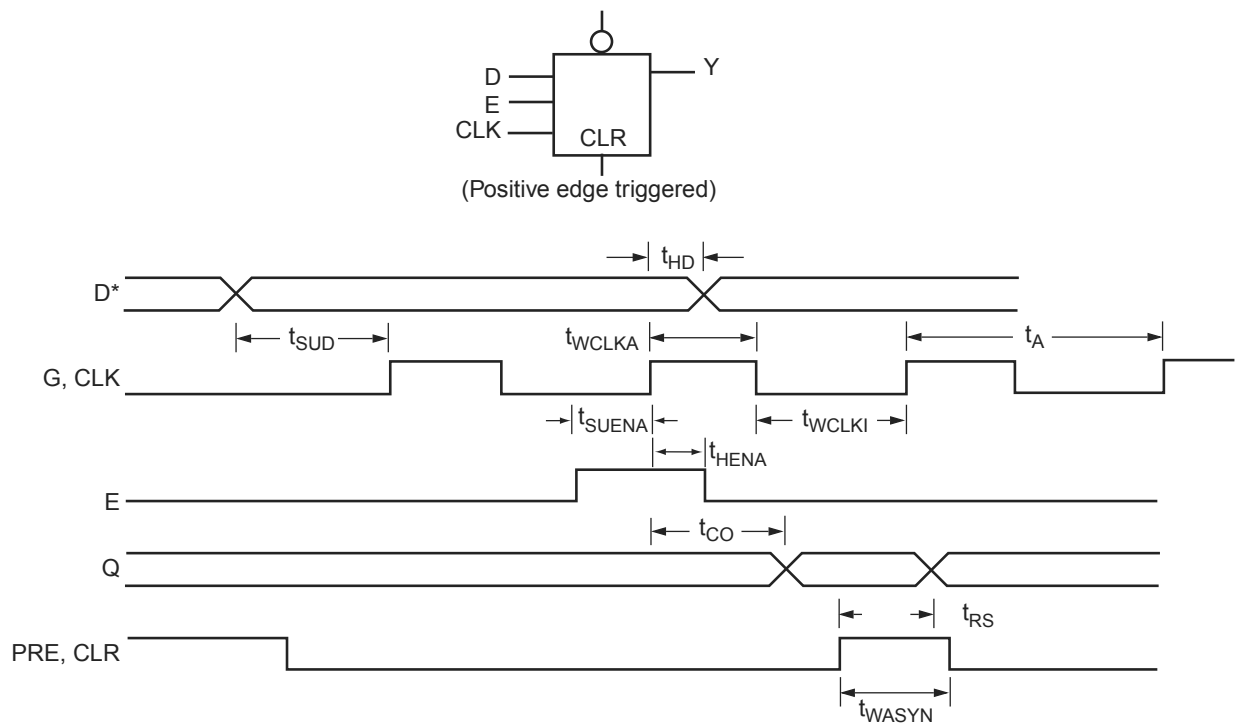
**Table 2-6 • CEQ Values for Microsemi FPGAs**

Item	CEQ Value
Modules ( $C_{\text{EQM}}$ )	5.8
Input Buffers ( $C_{\text{EQI}}$ )	12.9
Output Buffers ( $C_{\text{EQO}}$ )	23.8
Routed Array Clock Buffer Loads ( $C_{\text{EQCR}}$ )	3.9



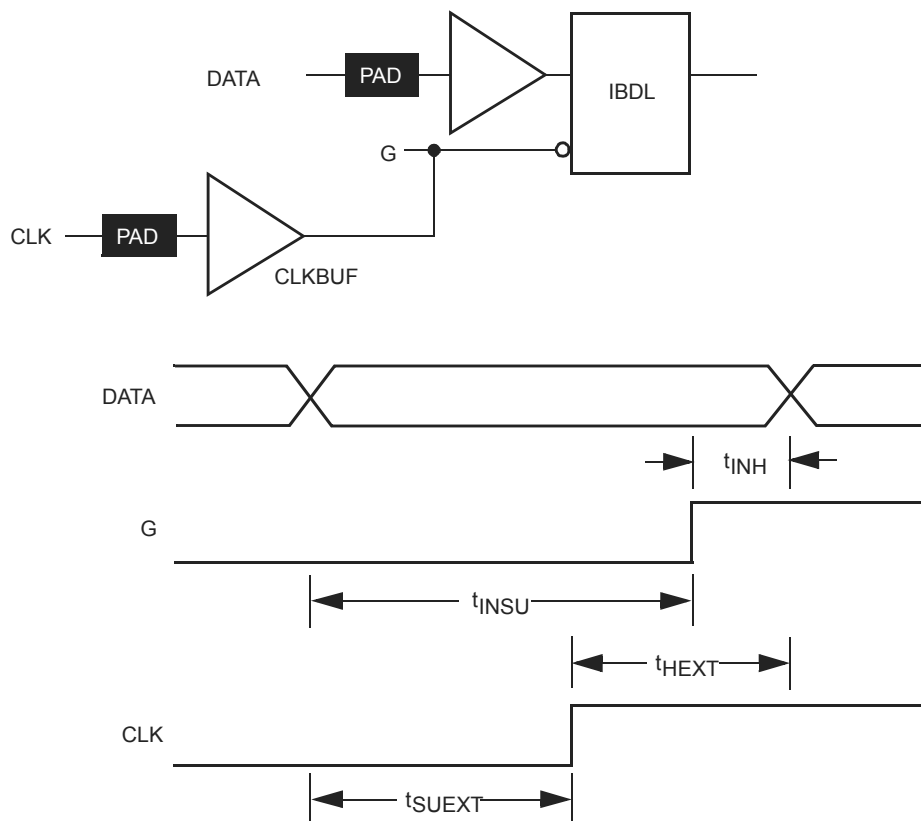
**Figure 2-5 • Module Delays**

## Sequential Module Timing Characteristics

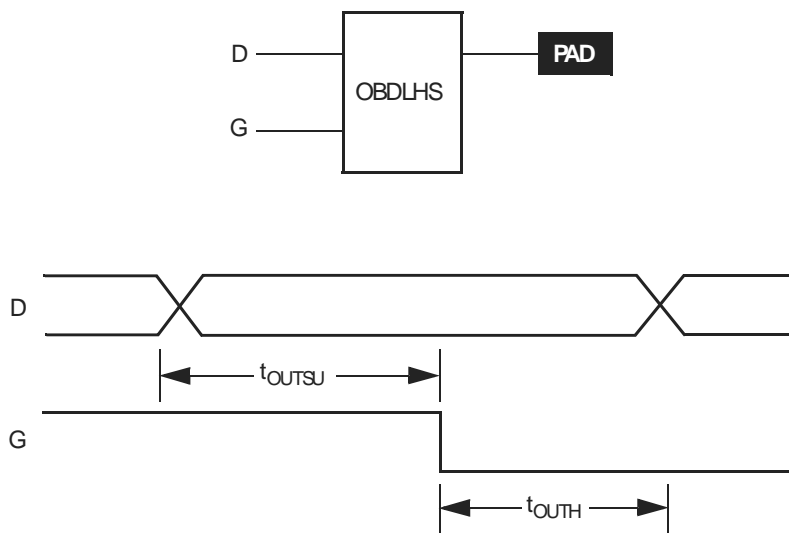


*Note: D represents all data functions involving A, B, and S for multiplexed flip-flops.*

**Figure 2-6 • Flip-Flops and Latches**



**Figure 2-7 • Input Buffer Latches**



**Figure 2-8 • Output Buffer Latches**

## A1225A Timing Characteristics

**Table 2-12 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C**

Logic Module Propagation Delays <sup>1</sup>		–2 Speed <sup>3</sup>		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PD1</sub>	Single Module		3.8		4.3		5.0	ns
t <sub>CO</sub>	Sequential Clock to Q		3.8		4.3		5.0	ns
t <sub>GO</sub>	Latch G to Q		3.8		4.3		5.0	ns
t <sub>RS</sub>	Flip-Flop (Latch) Reset to Q		3.8		4.3		5.0	ns
<b>Predicted Routing Delays<sup>2</sup></b>								
t <sub>RD1</sub>	FO = 1 Routing Delay		1.1		1.2		1.4	ns
t <sub>RD2</sub>	FO = 2 Routing Delay		1.7		1.9		2.2	ns
t <sub>RD3</sub>	FO = 3 Routing Delay		2.3		2.6		3.0	ns
t <sub>RD4</sub>	FO = 4 Routing Delay		2.8		3.1		3.7	ns
t <sub>RD8</sub>	FO = 8 Routing Delay		4.4		4.9		5.8	ns
<b>Sequential Timing Characteristics<sup>3,4</sup></b>								
t <sub>SUD</sub>	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		ns
t <sub>HD</sub>	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t <sub>SUENA</sub>	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		ns
t <sub>HENA</sub>	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t <sub>WCLKA</sub>	Flip-Flop (Latch) Clock Active Pulse Width	4.5		5.0		6.0		ns
t <sub>WASYN</sub>	Flip-Flop (Latch) Clock Asynchronous Pulse Width	4.5		5.0		6.0		ns
t <sub>A</sub>	Flip-Flop Clock Input Period	9.4		11.0		13.0		ns
t <sub>INH</sub>	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t <sub>INSU</sub>	Input Buffer Latch Setup	0.4		0.4		0.5		ns
t <sub>OUTH</sub>	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t <sub>OUTSU</sub>	Output Buffer Latch Setup	0.4		0.4		0.5		ns
f <sub>MAX</sub>	Flip-Flop (Latch) Clock Frequency		105.0		90.0		75.0	MHz

**Notes:**

1. For dual-module macros, use t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, t<sub>CO</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, or t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>SUD</sub>—whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
4. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

## A1225A Timing Characteristics (continued)

Table 2-13 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C

I/O Module Input Propagation Delays			–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description			Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>INYH</sub>	Pad to Y High			2.9		3.3		3.8	ns
t <sub>INYL</sub>	Pad to Y Low			2.6		3.0		3.5	ns
t <sub>INGH</sub>	G to Y High			5.0		5.7		6.6	ns
t <sub>INGL</sub>	G to Y Low			4.7		5.4		6.3	ns
<b>Input Module Predicted Input Routing Delays*</b>									
t <sub>IRD1</sub>	FO = 1 Routing Delay			4.1		4.6		5.4	ns
t <sub>IRD2</sub>	FO = 2 Routing Delay			4.6		5.2		6.1	ns
t <sub>IRD3</sub>	FO = 3 Routing Delay			5.3		6.0		7.1	ns
t <sub>IRD4</sub>	FO = 4 Routing Delay			5.7		6.4		7.6	ns
t <sub>IRD8</sub>	FO = 8 Routing Delay			7.4		8.3		9.8	ns
<b>Global Clock Network</b>									
t <sub>CKH</sub>	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		11.8		13.0		15.7	
t <sub>CKL</sub>	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		12.0		13.2		15.9	
t <sub>PWH</sub>	Minimum Pulse Width High	FO = 32	3.4		4.1		4.5		ns
		FO = 256	3.8		4.5		5.0		
t <sub>PWL</sub>	Minimum Pulse Width Low	FO = 32	3.4		4.1		4.5		ns
		FO = 256	3.8		4.5		5.0		
t <sub>CKSW</sub>	Maximum Skew	FO = 32		0.7		0.7		0.7	ns
		FO = 256		3.5		3.5		3.5	
t <sub>SUEXT</sub>	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t <sub>HEXT</sub>	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t <sub>P</sub>	Minimum Period	FO = 32	7.7		8.3		9.1		ns
		FO = 256	8.1		8.8		10.0		
f <sub>MAX</sub>	Maximum Frequency	FO = 32		130.0		120.0		110.0	ns
		FO = 256		125.0		115.0		100.0	

Note: \*These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.



## A1225A Timing Characteristics (continued)

Table 2-14 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C

TTL Output Module Timing <sup>1</sup>		–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>DLH</sub>	Data to Pad High		8.0		9.0		10.6	ns
t <sub>DHL</sub>	Data to Pad Low		10.1		11.4		13.4	ns
t <sub>ENZH</sub>	Enable Pad Z to High		8.9		10.0		11.8	ns
t <sub>ENZL</sub>	Enable Pad Z to Low		11.6		13.2		15.5	ns
t <sub>ENHZ</sub>	Enable Pad High to Z		7.1		8.0		9.4	ns
t <sub>ENLZ</sub>	Enable Pad Low to Z		8.3		9.5		11.1	ns
t <sub>GLH</sub>	G to Pad High		8.9		10.2		11.9	ns
t <sub>GHL</sub>	G to Pad Low		11.2		12.7		14.9	ns
d <sub>TLH</sub>	Delta Low to High		0.07		0.08		0.09	ns/pF
d <sub>THL</sub>	Delta High to Low		0.12		0.13		0.16	ns/pF
CMOS Output Module Timing <sup>1</sup>								
t <sub>DLH</sub>	Data to Pad High		10.1		11.5		13.5	ns
t <sub>DHL</sub>	Data to Pad Low		8.4		9.6		11.2	ns
t <sub>ENZH</sub>	Enable Pad Z to High		8.9		10.0		11.8	ns
t <sub>ENZL</sub>	Enable Pad Z to Low		11.6		13.2		15.5	ns
t <sub>ENHZ</sub>	Enable Pad High to Z		7.1		8.0		9.4	ns
t <sub>ENLZ</sub>	Enable Pad Low to Z		8.3		9.5		11.1	ns
t <sub>GLH</sub>	G to Pad High		8.9		10.2		11.9	ns
t <sub>GHL</sub>	G to Pad Low		11.2		12.7		14.9	ns
d <sub>TLH</sub>	Delta Low to High		0.12		0.13		0.16	ns/pF
d <sub>THL</sub>	Delta High to Low		0.09		0.10		0.12	ns/pF

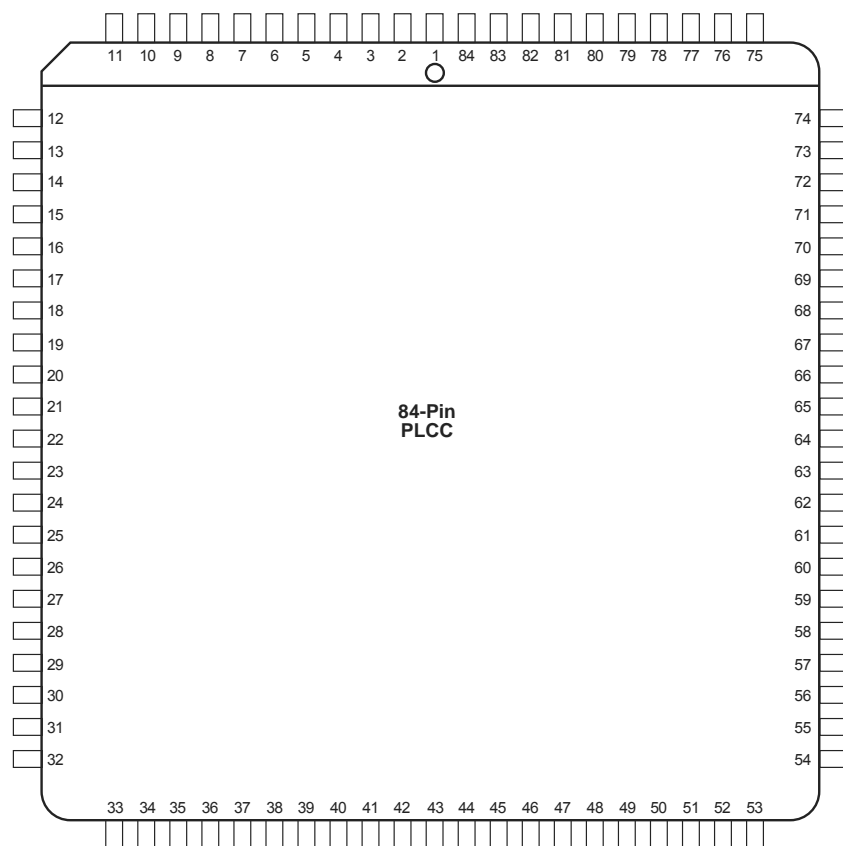
Notes:

1. Delays based on 50 pF loading.
2. SSO information can be found at [www.microsemi.com/soc/techdocs/appnotes/board\\_consideration.aspx](http://www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx).



## 3 – Package Pin Assignments

### PL84



#### **Note**

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

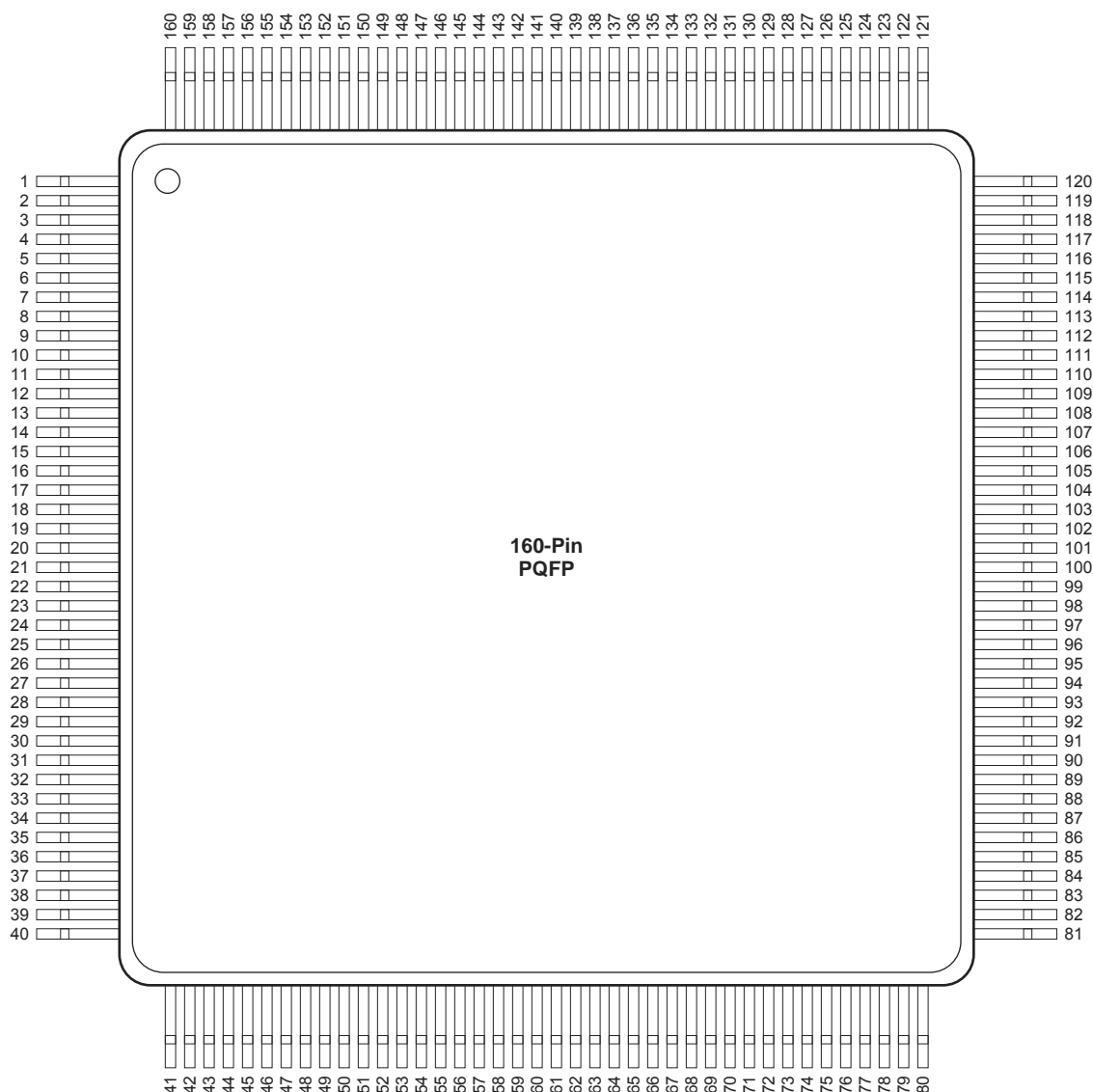
PQ100	
Pin Number	A1225A Function
2	DCLK, I/O
4	MODE
9	GND
16	VCC
17	VCC
22	GND
34	GND
40	VCC
46	GND
52	SDO
57	GND
64	GND

PQ100	
Pin Number	A1225A Function
65	VCC
66	VCC
67	VCC
72	GND
79	SDI, I/O
84	GND
87	PRA, I/O
89	CLKA, I/O
90	VCC
92	CLKB, I/O
94	PRB, I/O
96	GND

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

## PQ160



*Note:* This is the top view of the package

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

VQ100	
Pin Number	A1225A Function
2	MODE
7	GND
14	VCC
15	VCC
20	GND
32	GND
38	VCC
44	GND
50	SDO
55	GND
62	GND
63	VCC

VQ100	
Pin Number	A1225A Function
64	VCC
65	VCC
70	GND
77	SDI, I/O
82	GND
85	PRA, I/O
87	CLKA, I/O
88	VCC
90	CLKB, I/O
92	PRB, I/O
94	GND
100	DCLK, I/O

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

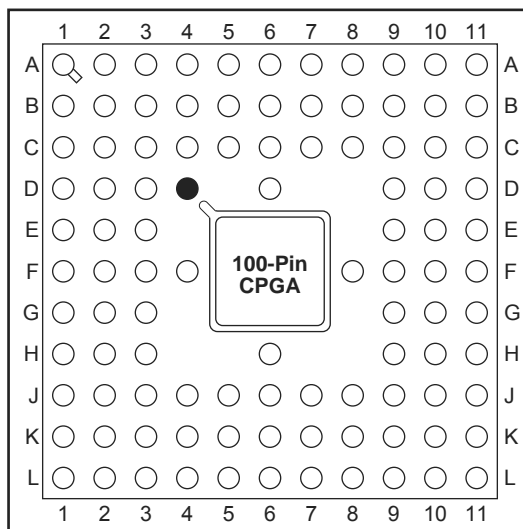
CQ172	
Pin Number	A1280A Function
1	MODE
7	GND
12	VCC
17	GND
22	GND
23	VCC
24	VCC
27	VCC
32	GND
37	GND
50	VCC
55	GND
65	GND
66	VCC
75	GND
80	VCC
85	SDO
98	GND
103	GND
106	GND

CQ172	
Pin Number	A1280A Function
107	VCC
108	GND
109	VCC
110	VCC
113	VCC
118	GND
123	GND
131	SDI, I/O
136	VCC
141	GND
148	PRA, I/O
150	CLKA, I/O
151	VCC
152	GND
154	CLKB, I/O
156	PRB, I/O
161	GND
166	VCC
171	DCLK, I/O

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

## PG100



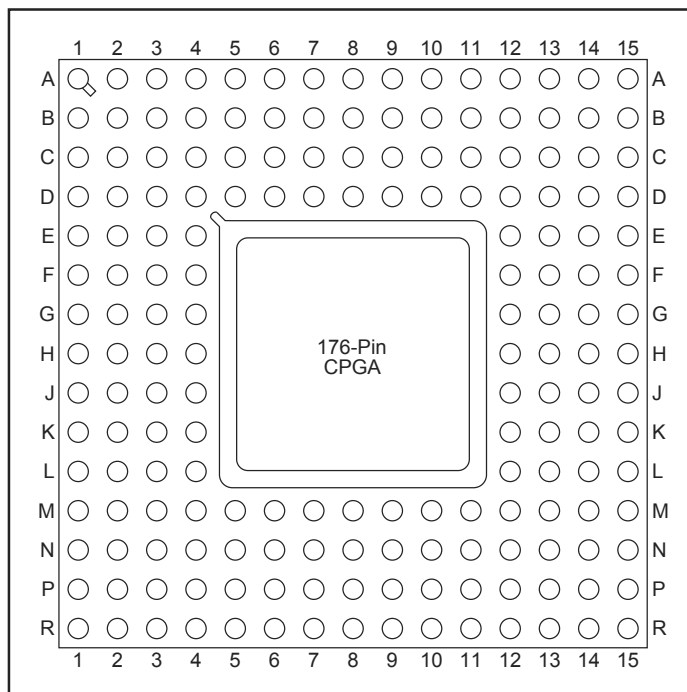
● Orientation Pin

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>



## PG176



### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>



## Datasheet Categories

### **Categories**

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

#### **Product Brief**

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

#### **Advance**

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

#### **Preliminary**

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

#### **Production**

This version contains information that is considered to be final.

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