E·XFL

Microsemi Corporation - A1280A-1PL84C Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

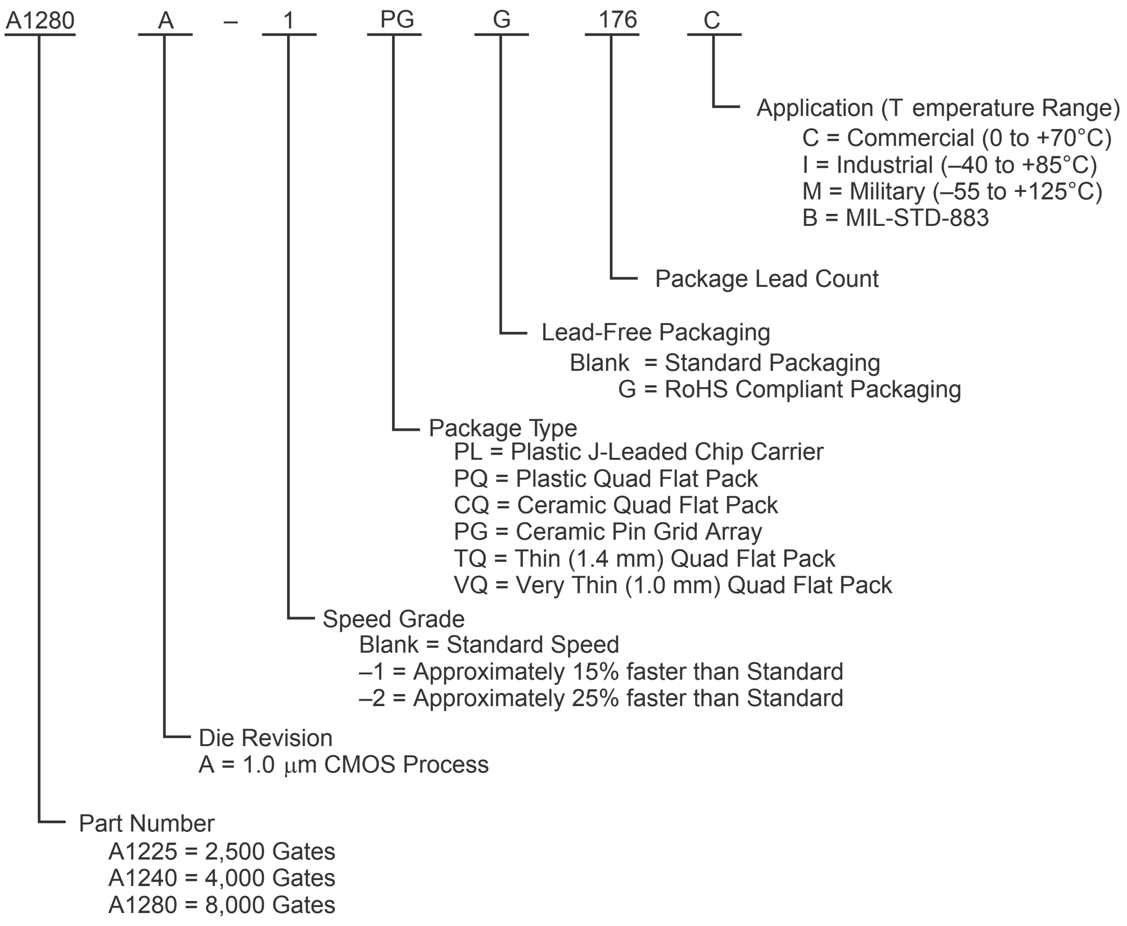
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	72
Number of Gates	8000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1280a-1pl84c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Ordering Information



Application (Temperature Range)
C = Commercial (0 to +70°C)
I = Industrial (–40 to +85°C)
M = Military (–55 to +125°C)
B = MIL-STD-883

Package Lead Count

Lead-Free Packaging
Blank = Standard Packaging
G = RoHS Compliant Packaging

Package Type
PL = Plastic J-Leaded Chip Carrier
PQ = Plastic Quad Flat Pack
CQ = Ceramic Quad Flat Pack
PG = Ceramic Pin Grid Array
TQ = Thin (1.4 mm) Quad Flat Pack
VQ = Very Thin (1.0 mm) Quad Flat Pack

Speed Grade
Blank = Standard Speed
–1 = Approximately 15% faster than Standard
–2 = Approximately 25% faster than Standard

Die Revision
A = 1.0 µm CMOS Process

Part Number
A1225 = 2,500 Gates
A1240 = 4,000 Gates
A1280 = 8,000 Gates

Product Plan

Device/Package	Speed Grade[1]			Application[1]			
	Std.	–1	–2	C	I	M	B
A1225A Device							
84-Pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–
100-Pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	✓	–	–
100-Pin Very Thin Quad Flatpack (VQ)	✓	✓	✓	✓	–	–	–
100-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	–	–	–
A1240A Device							
84-Pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–
132-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	–	✓	✓
144-Pin Plastic Quad Flat Pack (PQ)	✓	✓	✓	✓	✓	–	–
176-Pin Thin (1.4 mm) Quad Flat Pack (TQ)	✓	✓	✓	✓	–	–	–
A1280A Device							
160-Pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	✓	–	–
172-Pin Ceramic Quad Flatpack (CQ)	✓	✓	✓	✓	–	✓	✓
176-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	–	✓	✓
176-Pin Thin (1.4 mm) Quad Flat Pack (TQ)	✓	✓	✓	✓	–	–	–

Notes:

1. *Applications:*
   C = Commercial
   I = Industrial
   M = Military
   B = MIL-STD-883

Availability:
✓ = Available
P = Planned
– = Not planned

Speed Grade:
–1 = Approx. 15% faster than Std.
–2 = Approx. 25% faster than Std.

2. *Contact your Microsemi SoC Products Group sales representative for product availability.*

Device Resources

Device Series	Logic Modules	Gates	User I/Os									
			PG176	PG132	PG100	PQ160	PQ144	PQ100	PL84	CQ172	TQ176	VQ100
A1225A	451	2,500	–	–	83	–	–	83	72	–	–	83
A1240A	684	4,000	–	104	–	–	104	–	72	–	104	–
A1280A	1,232	8,000	140	–	–	125	–	–	72	140	140	–

Contact your local Microsemi SoC Products Group representative for device availability:
http://www.microsemi.com/soc/contact/default.aspx.

Static Power Component

Microsemi FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated in Table 2-5 for commercial, worst case conditions.

Table 2-5 • **Standby Power Calculation**

ICC	VCC	Power
2 mA	5.25 V	10.5 mW

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs.

An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by EQ 3.

$$\text{Power } (\mu W) = C_{EQ} * VCC^2 * F$$

EQ 3

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

VCC is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring ICC active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown in Table 2-6.

Table 2-6 • **CEQ Values for Microsemi FPGAs**

Item	CEQ Value
Modules (C_{EQM})	5.8
Input Buffers (C_{EQI})	12.9
Output Buffers (C_{EQO})	23.8
Routed Array Clock Buffer Loads (C_{EQCR})	3.9

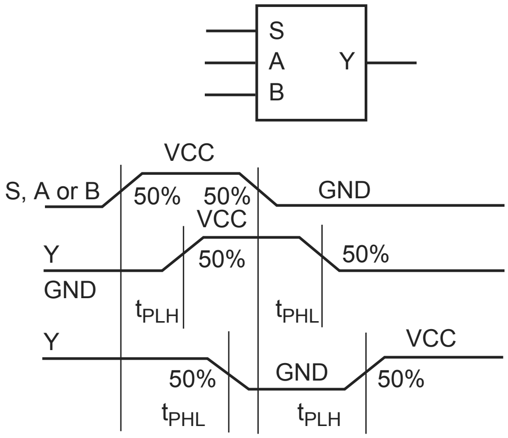
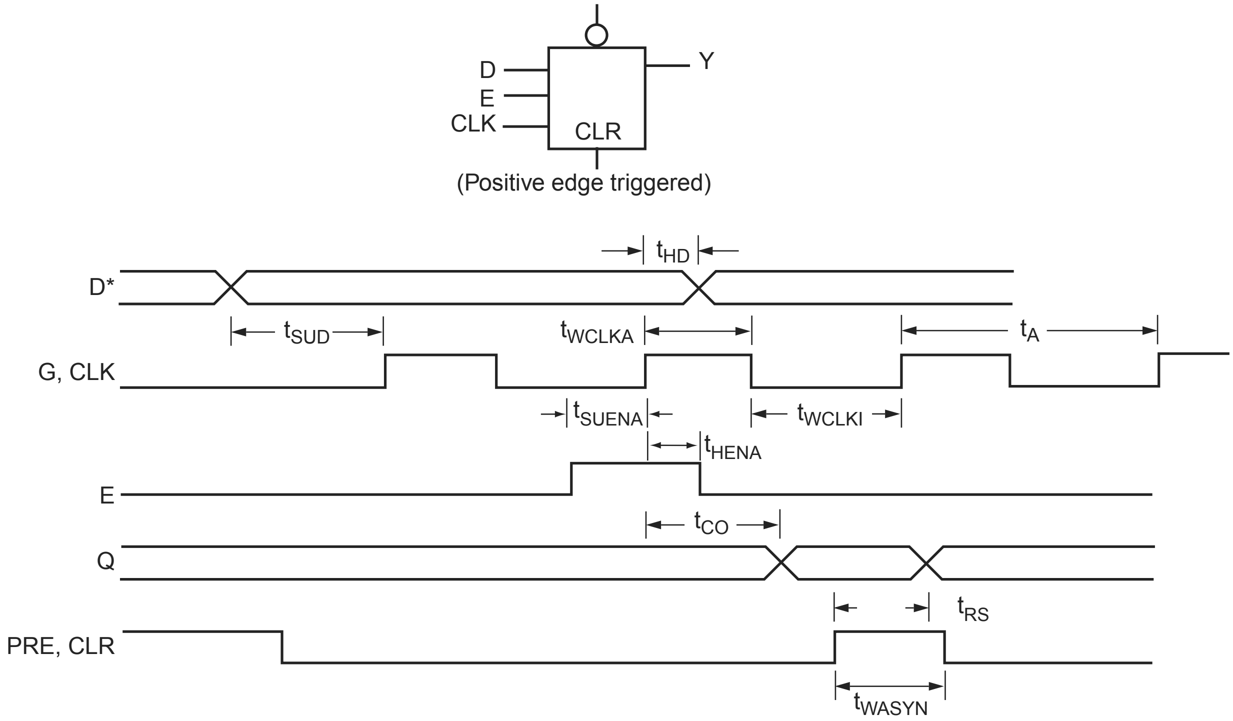


Figure 2-5 • **Module Delays**

Sequential Module Timing Characteristics



Note: D represents all data functions involving A, B, and S for multiplexed flip-flops.

Figure 2-6 • **Flip-Flops and Latches**

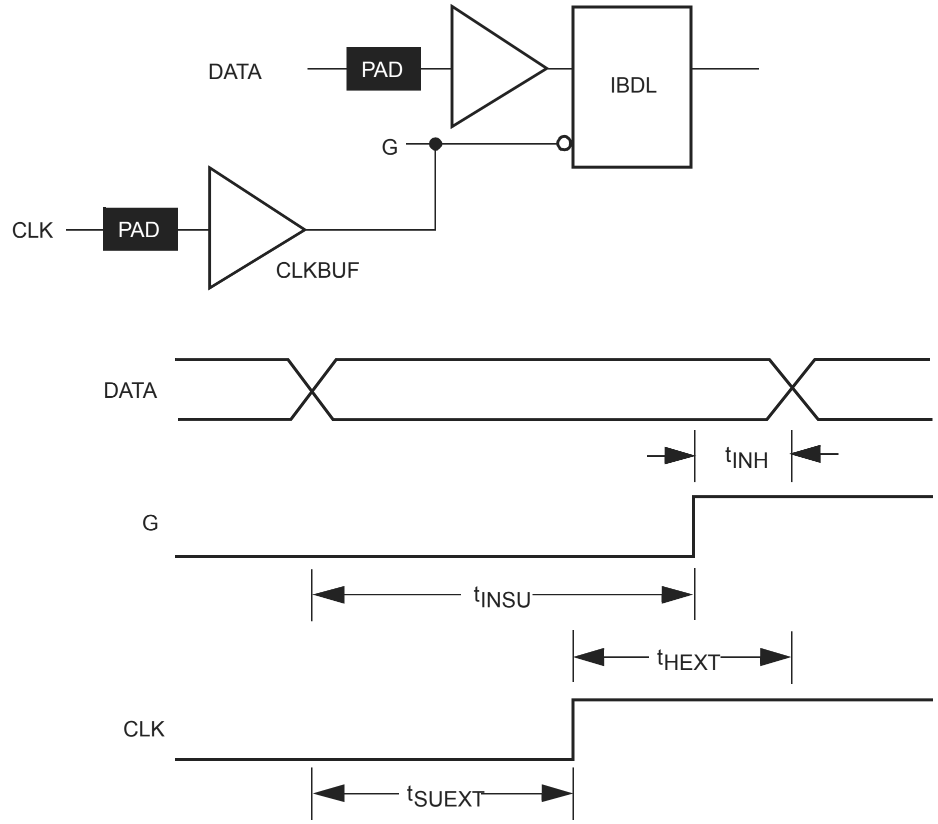


Figure 2-7 • **Input Buffer Latches**

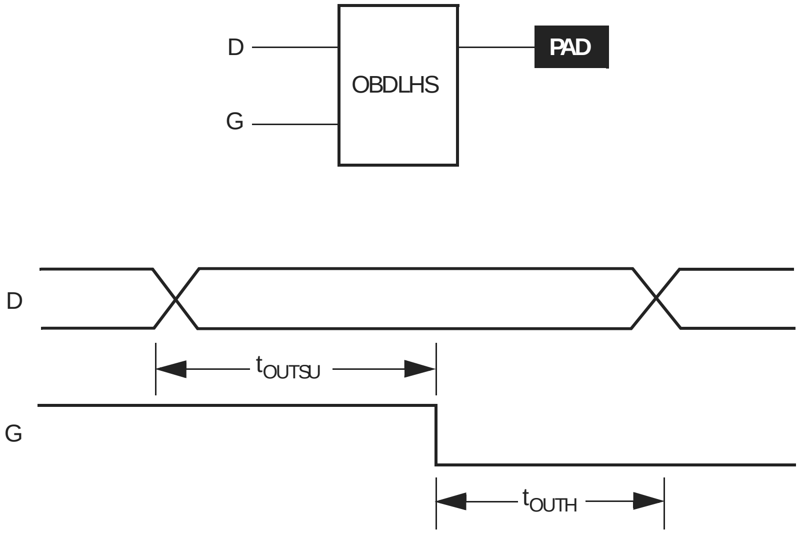


Figure 2-8 • **Output Buffer Latches**

Timing Derating Factor (Temperature and Voltage)

***Table 2-9* • Timing Derating Factor (Temperature and Voltage)**

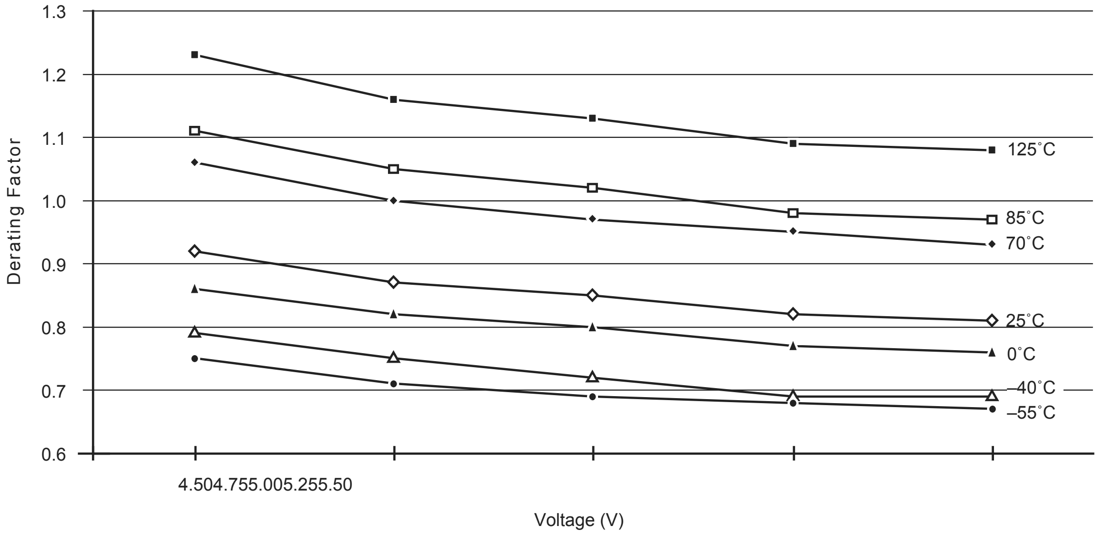
(Commercial Minimum/Maximum Specification) x	**Industrial**		**Military**	
	Min.	**Max.**	**Min.**	Max.
	0.69	1.11	0.67	1.23

***Table 2-10* • Timing Derating Factor for Designs at Typical Temperature (T_J = 25°C) and Voltage (5.0 V)**

(Commercial Maximum Specification) x	0.85

***Table 2-11* • Temperature and Voltage Derating Factors (normalized to Worst-Case Commercial, TJ = 4.75 V, 70°C)**

	–55	**–40**	**0**	**25**	**70**	**85**	**125**
4.50	0.75	0.79	0.86	0.92	1.06	1.11	1.23
4.75	0.71	0.75	0.82	0.87	1.00	1.05	1.13
5.00	0.69	0.72	0.80	0.85	0.97	1.02	1.13
5.25	0.68	0.69	0.77	0.82	0.95	0.98	1.09
5.50	0.67	0.69	0.76	0.81	0.93	0.97	1.08



Note: *This derating factor applies to all routing and propagation delays.*

***Figure 2-9* • Junction Temperature and Voltage Derating Curves (normalized to Worst-Case Commercial, T_J = 4.75 V, 70°C)**

A1240A Timing Characteristics

***Table 2-15* • A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

Logic Module Propagation Delays[1]		**–2 Speed[3]**		**–1 Speed**		**Std. Speed**		**Units**
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{PD1}	Single Module		3.8		4.3		5.0	ns
t_{CO}	Sequential Clock to Q		3.8		4.3		5.0	ns
t_{GO}	Latch G to Q		3.8		4.3		5.0	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		3.8		4.3		5.0	ns
Predicted Routing Delays[2]								
t_{RD1}	FO = 1 Routing Delay		1.4		1.5		1.8	ns
t_{RD2}	FO = 2 Routing Delay		1.7		2.0		2.3	ns
t_{RD3}	FO = 3 Routing Delay		2.3		2.6		3.0	ns
t_{RD4}	FO = 4 Routing Delay		3.1		3.5		4.1	ns
t_{RD8}	FO = 8 Routing Delay		4.7		5.4		6.3	ns
Sequential Timing Characteristics[3,4]								
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.5		6.0		6.5		ns
t_{WASYN}	Flip-Flop (Latch) Clock Asynchronous Pulse Width	4.5		6.0		6.5		ns
t_A	Flip-Flop Clock Input Period	9.8		12.0		15.0		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.4		0.4		0.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.4		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		100.0		80.0		66.0	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$—whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

Pin Descriptions

CLKA Clock A (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB Clock B (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

GND Ground

Low supply voltage.

I/O Input/Output (Input, Output)

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven Low by the ALS software.

MODE Mode (Input)

The MODE pin controls the use of multifunction pins (DCLK, PRA, PRB, SDI). When the MODE pin is High, the special functions are active. When the MODE pin is Low, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled High when required.

NC No Connection

This pin is not connected to circuitry within the device.

PRA Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin’s probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

PRB Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin’s probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

SDO Serial Data Output (Output)

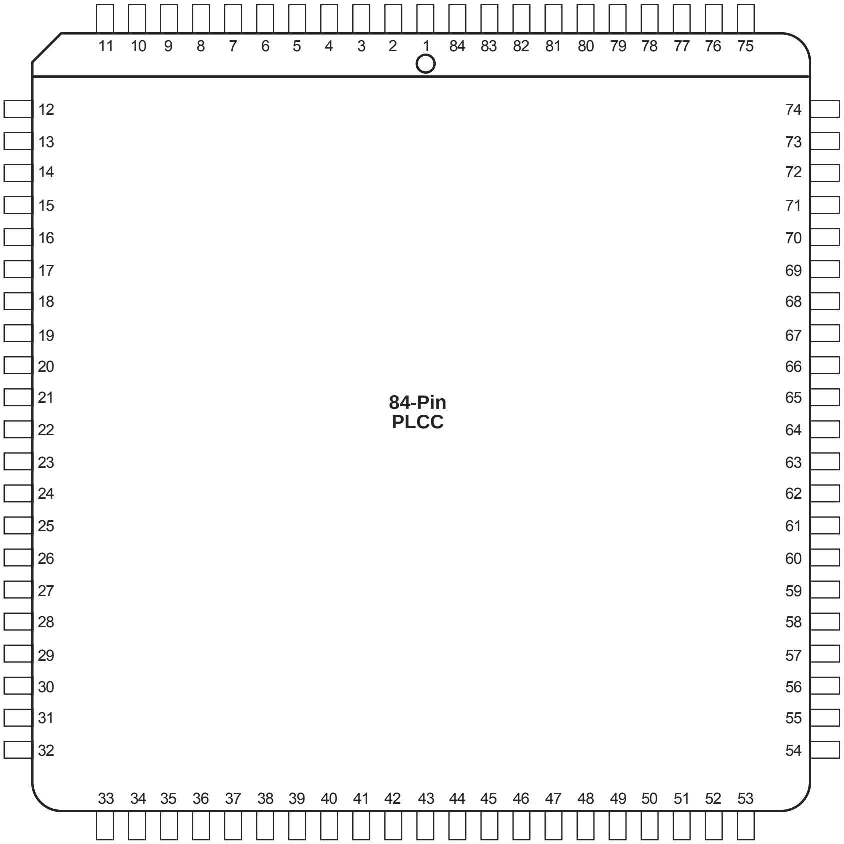
Serial data output for diagnostic probe. SDO is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

VCC 5.0 V Supply Voltage

High supply voltage.

3 – Package Pin Assignments

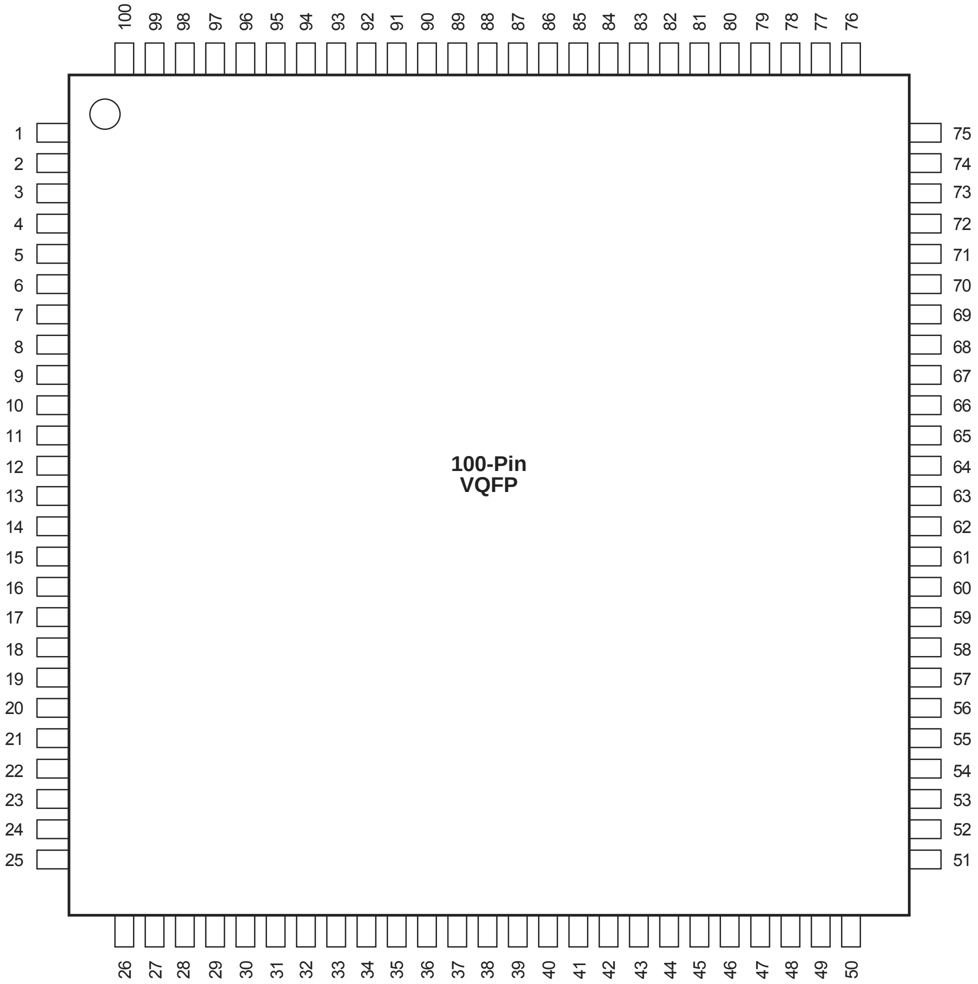
PL84



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

VQ100



Note

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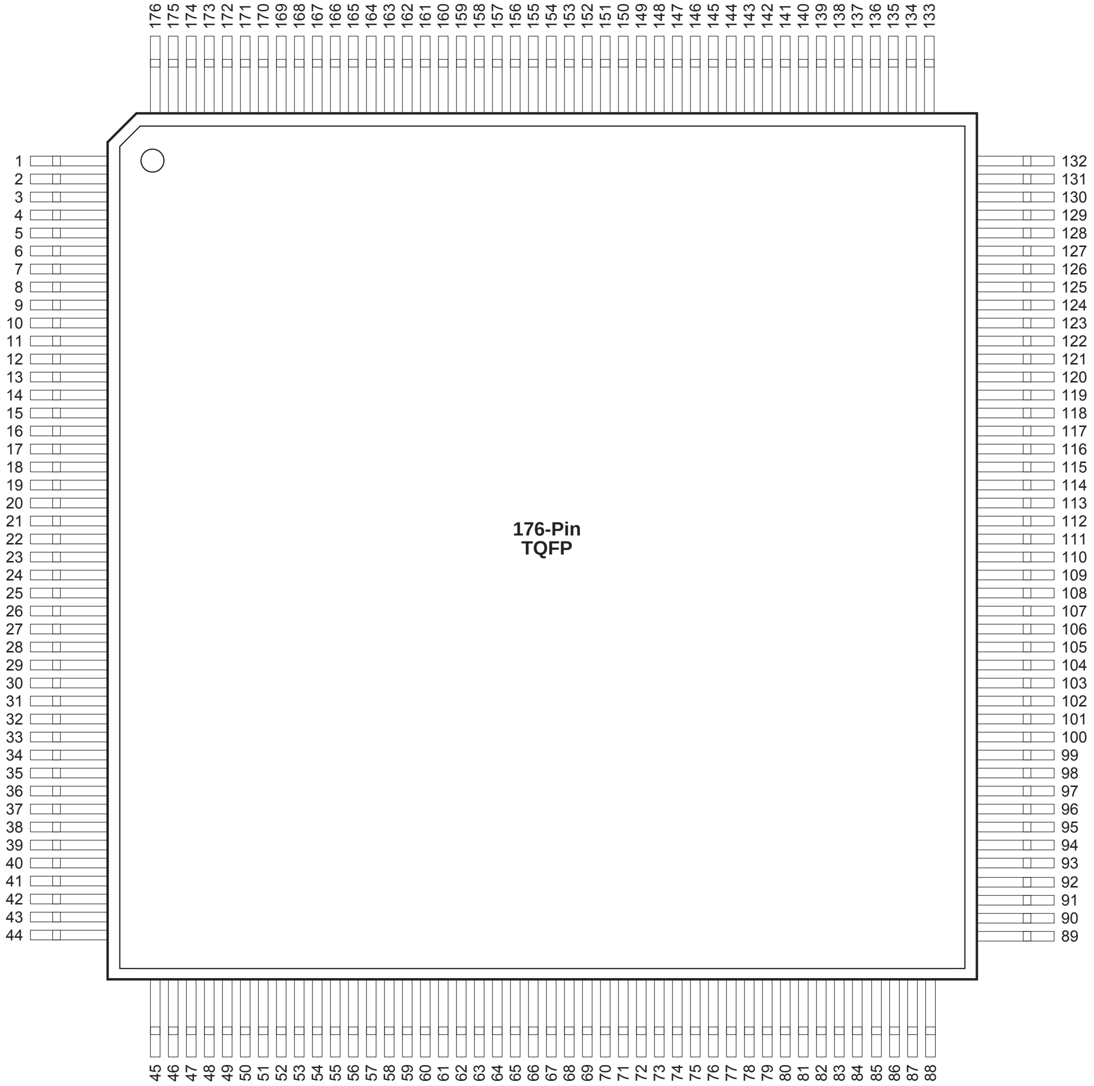
TQ176



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

TQ176		
Pin Number	**A1240A Function**	**A1280A Function**
155	VCC	VCC
156	GND	GND
158	CLKB, I/O	CLKB, I/O
160	PRB, I/O	PRB, I/O
161	NC	I/O
165	NC	NC
166	NC	I/O
168	NC	I/O
170	NC	VCC
173	NC	I/O
175	DCLK, I/O	DCLK, I/O

Notes:

1. NC denotes no connection.
2. All unlisted pin numbers are user I/Os.
3. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

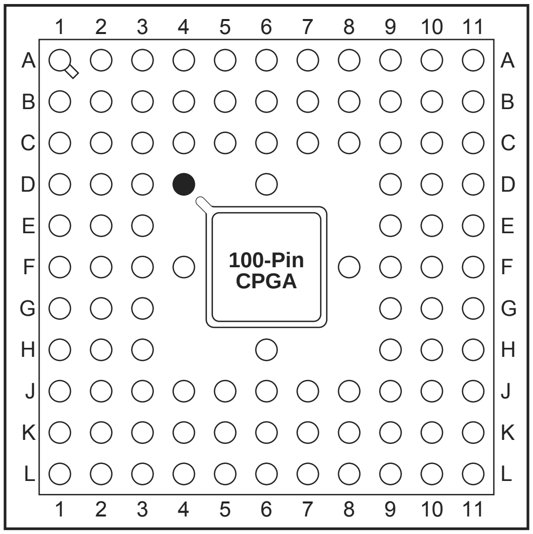
CQ172	
Pin Number	**A1280A Function**
1	MODE
7	GND
12	VCC
17	GND
22	GND
23	VCC
24	VCC
27	VCC
32	GND
37	GND
50	VCC
55	GND
65	GND
66	VCC
75	GND
80	VCC
85	SDO
98	GND
103	GND
106	GND

CQ172	
Pin Number	**A1280A Function**
107	VCC
108	GND
109	VCC
110	VCC
113	VCC
118	GND
123	GND
131	SDI, I/O
136	VCC
141	GND
148	PRA, I/O
150	CLKA, I/O
151	VCC
152	GND
154	CLKB, I/O
156	PRB, I/O
161	GND
166	VCC
171	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG100



● Orientation Pin

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

PG100	
Pin Number	**A1225A Function**
A4	PRB, I/O
A7	PRA, I/O
B6	VCC
C2	MODE
C3	DCLK, I/O
C5	GND
C6	CLKA, I/O
C7	GND
C8	SDI, I/O
D6	CLKB, I/O
D10	GND
E3	GND

PG100	
Pin Number	**A1225A Function**
E11	VCC
F3	VCC
F9	VCC
F10	VCC
F11	GND
G1	VCC
G3	GND
G9	GND
J5	GND
J7	GND
J9	SDO
K6	VCC

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG132	
Pin Number	**A1240A Function**
A1	MODE
B5	GND
B6	CLKB, I/O
B7	CLKA, I/O
B8	PRA, I/O
B9	GND
B12	SDI, I/O
C3	DCLK, I/O
C5	GND
C6	PRB, I/O
C7	VCC
C9	GND
D7	VCC
E3	GND
E11	GND
E12	GND
F4	GND
G2	VCC
G3	VCC
G4	VCC
G10	VCC
G11	VCC
G12	VCC
G13	VCC
H13	GND
J2	GND
J3	GND
J11	GND
K7	VCC
K12	GND
L5	GND
L7	VCC
L9	GND
M9	GND
N12	SDO

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

4 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each version of the datasheet.

Revision	Changes	Page
Revision 8 (January 2012)	The ACT 2 datasheet was formatted newly in the style used for current datasheets. The same information is present (other than noted in the list of changes for this revision) but divided into chapters.	N/A
	Package names used in Table 1 • ACT 2 Product Family Profile and throughout the document were revised to match standards given in *Package Mechanical Drawings* (SAR 27395).	I
	The description for SDO pins had earlier been removed from the datasheet and has now been included again, in the "Pin Descriptions" section (SAR 35819).	2-21
	SDO pin numbers had earlier been removed from package pin assignment tables in the datasheet, and have now been restored to the pin tables (SAR 35819).	3-2
Revision 7 (June 2006)	The "Ordering Information" section was revised to include RoHS information.	II
Revision 6 (December 2000)	In the "PG176" package, pin A3 was incorrectly assigned as CLKA, I/O. A3 is a user I/O. Pin A9 is CLKA, I/O.	3-21

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

Safety Critical, Life Support, and High-Reliability Applications Policy

The products described in this advance status document may not have completed the Microsemi qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the Microsemi SoC Products Group Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the SoC Products Group’s products is available at http://www.microsemi.com/soc/documents/ORT_Report.pdf. Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local sales office for additional reliability information.

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