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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	140
Number of Gates	8000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	172-CQFP with Tie Bar
Supplier Device Package	172-CQFP (63.37x63.37)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1280a-cq172m

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1 – ACT 2 Family Overview

General Description

The ACT 2 family represents Actel's second generation of field programmable gate arrays (FPGAs). The ACT 2 family presents a two-module architecture, consisting of C-modules and S-modules. These modules are optimized for both combinatorial and sequential designs. Based on Actel's patented channeled array architecture, the ACT 2 family provides significant enhancements to gate density and performance while maintaining downward compatibility with the ACT 1 design environment and upward compatibility with the ACT 3 design environment. The devices are implemented in silicon gate, 1.0-µm, two-level metal CMOS, and employ Actel's PLICE® antifuse technology. This revolutionary architecture offers gate array design flexibility, high performance, and fast time-to-production with user programming. The ACT 2 family is supported by the Designer and Designer Advantage Systems, which offers automatic pin assignment, validation of electrical and design rules, automatic placement and routing, timing analysis, user programming, and diagnostic probe capabilities. The systems are supported on the following platforms: 386/486™ PC, Sun™, and HP™ workstations. The systems provide CAE interfaces to the following design environments: Cadence, Viewlogic®, Mentor Graphics®, and OrCAD™.

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2 – Detailed Specifications

Operating Conditions

Table 2-1 • **Absolute Maximum Ratings[1]**

Symbol	Parameter	Limits	Units
VCC	DC supply voltage	−0.5 to +7.0	V
VI	Input voltage	−0.5 to VCC + 0.5	V
VO	Output voltage	−0.5 to VCC + 0.5	V
IIO	I/O source sink current[2]	±20	mA
T_{STG}	Storage temperature	−65 to +150	°C

Notes:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.
2. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND −0.5 V, the internal protection diodes will be forward biased and can draw excessive current.

Table 2-2 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature range*	0 to +70	−40 to +85	−55 to +125	°C
Power supply tolerance	±5	±10	±10	%VCC

Note: *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

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Table 2-3 • **Electrical Specifications**

Symbol	Parameter	Commercial		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
VOH[1]	(IOH = –10 mA)[2]	2.4	–	–	–	–	–	V
	(IOH = –6 mA)	3.84	–	–	–	–	–	V
	(IOH = –4 mA)	–	–	3.7	–	3.7	–	V
VOL[1]	(IOL = 10 mA)[2]	–	0.5	–	–	–	–	V
	(IOL = 6 mA)	–	0.33	–	0.40	–	0.40	V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
Input Transition Time t_R, t_F[2]		–	500	–	500	–	500	ns
C_{IO} I/O capacitance[2,3]		–	10	–	10	–	10	pF
Standby Current, ICC[4] (typical = 1 mA)		–	2	–	10	–	20	mA
Leakage Current[5]		–10	+10	–10	+10	–10	+10	µA
ICC(D)	Dynamic VCC supply current. See the Power Dissipation section.							

Notes:

1. *Only one output tested at a time. VCC = minimum.*
2. *Not tested, for information only.*
3. *Includes worst-case PG176 package capacitance. VOUT = 0 V, f = 1 MHz*
4. *All outputs unloaded. All inputs = VCC or GND, typical ICC = 1 mA. ICC limit includes IPP and ISV during normal operations.*
5. *VOUT, VIN = VCC or GND.*

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a PQ160 package at commercial temperature and still air is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}\text{°C/W}} = \frac{150°C - 70°C}{33°C/W} = 2.4 \text{ W}$$

EQ 1

Table 2-4 • **Package Thermal Characteristics**

Package Type*	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft./min.	Units
Ceramic Pin Grid Array	100	5	35	17	°C/W
	132	5	30	15	°C/W
	176	8	23	12	°C/W
Ceramic Quad Flatpack	172	8	25	15	°C/W
Plastic Quad Flatpack[1]	100	13	48	40	°C/W
	144	15	40	32	°C/W
	160	15	38	30	°C/W
Plastic Leaded Chip Carrier	84	12	37	28	°C/W
Very Thin Quad Flatpack	100	12	43	35	°C/W
Thin Quad Flatpack	176	15	32	25	°C/W

Notes: (Maximum Power in Still Air)

1. *Maximum power dissipation values for PQFP packages are 1.9 W (PQ100), 2.3 W (PQ144), and 2.4 W (PQ160).*
2. *Maximum power dissipation for PLCC packages is 2.7 W.*
3. *Maximum power dissipation for VQFP packages is 2.3 W.*
4. *Maximum power dissipation for TQFP packages is 3.1 W.*

Power Dissipation

P = [ICC standby + ICCactive] * VCC + IOL * VOL * N + IOH* (VCC – VOH) * M

EQ 2

where:

ICC standby is the current flowing when no inputs or outputs are changing

ICCactive is the current flowing due to CMOS switching.

IOL and IOH are TTL sink/source currents.

VOL and VOH are TTL level output voltages.

N is the number of outputs driving TTL loads to VOL.

M is the number of outputs driving TTL loads to VOH.

An accurate determination of N and M is problematical because their values depend on the family type, design details, and on the system I/O. The power can be divided into two components: static and active.

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are given in Table 2-8.

Table 2-8 • **Guidelines for Predicting Power Dissipation**

Data	Value
Logic Modules (m)	80% of modules
Inputs switching (n)	# inputs/4
Outputs switching (p)	# output/4
First routed array clock loads (q1)	40% of sequential modules
Second routed array clock loads (q2)	40% of sequential modules
Load capacitance (C_L)	35 pF
Average logic module switching rate (f_m)	F/10
Average input switching rate (f_n)	F/5
Average output switching rate (f_p)	F/10
Average first routed array clock rate (f_{q1})	F
Average second routed array clock rate (f_{q2})	F/2

ACT 2 Timing Model[1]

Figure 2-1 • **Timing Model**
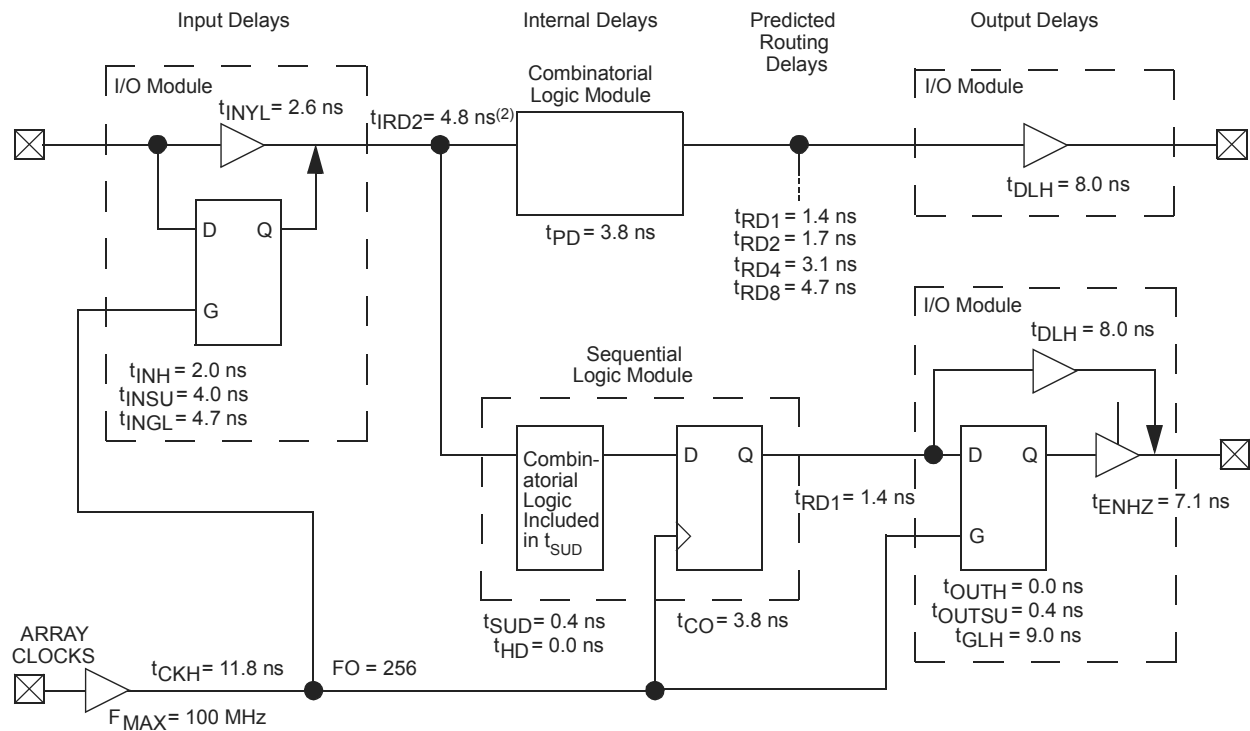
Notes:

1. *Values shown for A1240A-2 at worst-case commercial conditions.*
2. *Input module predicted routing delay*

A1240A Timing Characteristics

Table 2-15 • **A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

Logic Module Propagation Delays[1]		–2 Speed[3]		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t$_{PD1}$	Single Module		3.8		4.3		5.0	ns
t$_{CO}$	Sequential Clock to Q		3.8		4.3		5.0	ns
t$_{GO}$	Latch G to Q		3.8		4.3		5.0	ns
t$_{RS}$	Flip-Flop (Latch) Reset to Q		3.8		4.3		5.0	ns
Predicted Routing Delays[2]								
t$_{RD1}$	FO = 1 Routing Delay		1.4		1.5		1.8	ns
t$_{RD2}$	FO = 2 Routing Delay		1.7		2.0		2.3	ns
t$_{RD3}$	FO = 3 Routing Delay		2.3		2.6		3.0	ns
t$_{RD4}$	FO = 4 Routing Delay		3.1		3.5		4.1	ns
t$_{RD8}$	FO = 8 Routing Delay		4.7		5.4		6.3	ns
Sequential Timing Characteristics[3,4]								
t$_{SUD}$	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		ns
t$_{HD}$	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t$_{SUENA}$	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		ns
t$_{HENA}$	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t$_{WCLKA}$	Flip-Flop (Latch) Clock Active Pulse Width	4.5		6.0		6.5		ns
t$_{WASYN}$	Flip-Flop (Latch) Clock Asynchronous Pulse Width	4.5		6.0		6.5		ns
t$_A$	Flip-Flop Clock Input Period	9.8		12.0		15.0		ns
t$_{INH}$	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t$_{INSU}$	Input Buffer Latch Setup	0.4		0.4		0.5		ns
t$_{OUTH}$	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t$_{OUTSU}$	Output Buffer Latch Setup	0.4		0.4		0.5		ns
f$_{MAX}$	Flip-Flop (Latch) Clock Frequency		100.0		80.0		66.0	MHz

Notes:

1. *For dual-module macros, use t$_{PD1}$ + t$_{RD1}$ + t$_{PDn}$, t$_{CO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$—whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*

4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A1240A Timing Characteristics (continued)

Table 2-16 • **A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

I/O Module Input Propagation Delays		–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t$_{INYH}$	Pad to Y High		2.9		3.3		3.8	ns
t$_{INYL}$	Pad to Y Low		2.6		3.0		3.5	ns
t$_{INGH}$	G to Y High		5.0		5.7		6.6	ns
t$_{INGL}$	G to Y Low		4.7		5.4		6.3	ns
Input Module Predicted Input Routing Delays[*]								
t$_{IRD1}$	FO = 1 Routing Delay		4.2		4.8		5.6	ns
t$_{IRD2}$	FO = 2 Routing Delay		4.8		5.4		6.4	ns
t$_{IRD3}$	FO = 3 Routing Delay		5.4		6.1		7.2	ns
t$_{IRD4}$	FO = 4 Routing Delay		5.9		6.7		7.9	ns
t$_{IRD8}$	FO = 8 Routing Delay		7.9		8.9		10.5	ns
Global Clock Network								
t$_{CKH}$	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		11.8		13.0		15.7	
t$_{CKL}$	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		12.0		13.2		15.9	
t$_{PWH}$	Minimum Pulse Width High	FO = 32	3.8		4.5		5.5		ns
		FO = 256	4.1		5.0		5.8		
t$_{PWL}$	Minimum Pulse Width Low	FO = 32	3.8		4.5		5.5		ns
		FO = 256	4.1		5.0		5.8		
t$_{CKSW}$	Maximum Skew	FO = 32		0.5		0.5		0.5	ns
		FO = 256		2.5		2.5		2.5	
t$_{SUEXT}$	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t$_{HEXT}$	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t$_P$	Minimum Period	FO = 32	8.1		9.1		11.1		ns
		FO = 256	8.8		10.0		11.7		
f$_{MAX}$	Maximum Frequency	FO = 32		125.0		110.0		90.0	ns
		FO = 256		115.0		100.0		85.0	

Note: *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

Pin Descriptions

CLKA   Clock A (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB   Clock B (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK   Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

GND   Ground

Low supply voltage.

I/O   Input/Output (Input, Output)

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven Low by the ALS software.

MODE   Mode (Input)

The MODE pin controls the use of multifunction pins (DCLK, PRA, PRB, SDI). When the MODE pin is High, the special functions are active. When the MODE pin is Low, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled High when required.

NC   No Connection

This pin is not connected to circuitry within the device.

PRA   Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

PRB   Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

SDI   Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.
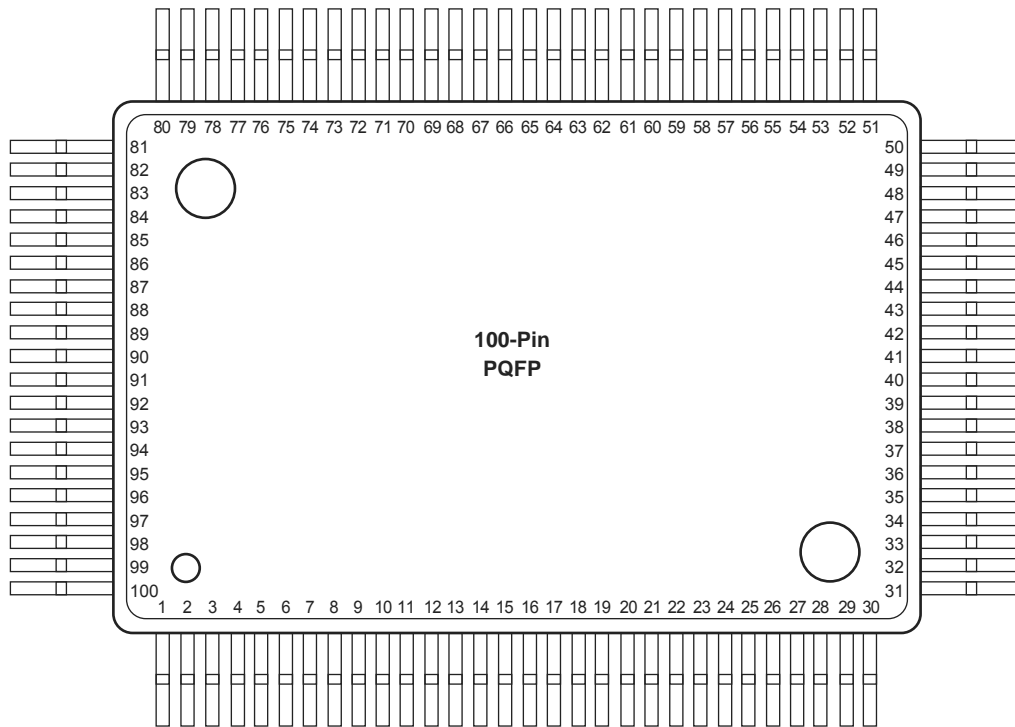
SDO   Serial Data Output (Output)

Serial data output for diagnostic probe. SDO is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

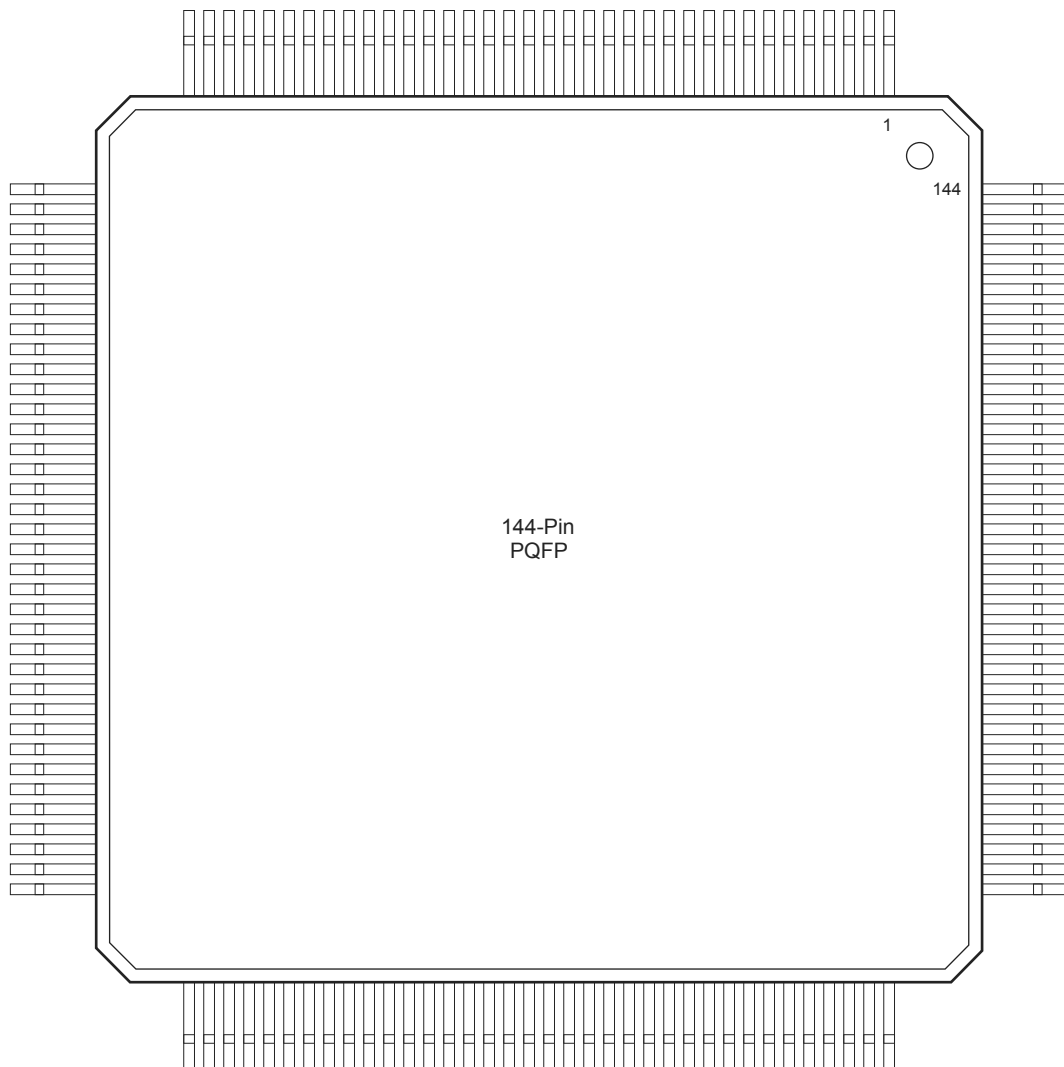**VCC   5.0 V Supply Voltage**

High supply voltage.

PQ100

**100-Pin
PQFP**

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
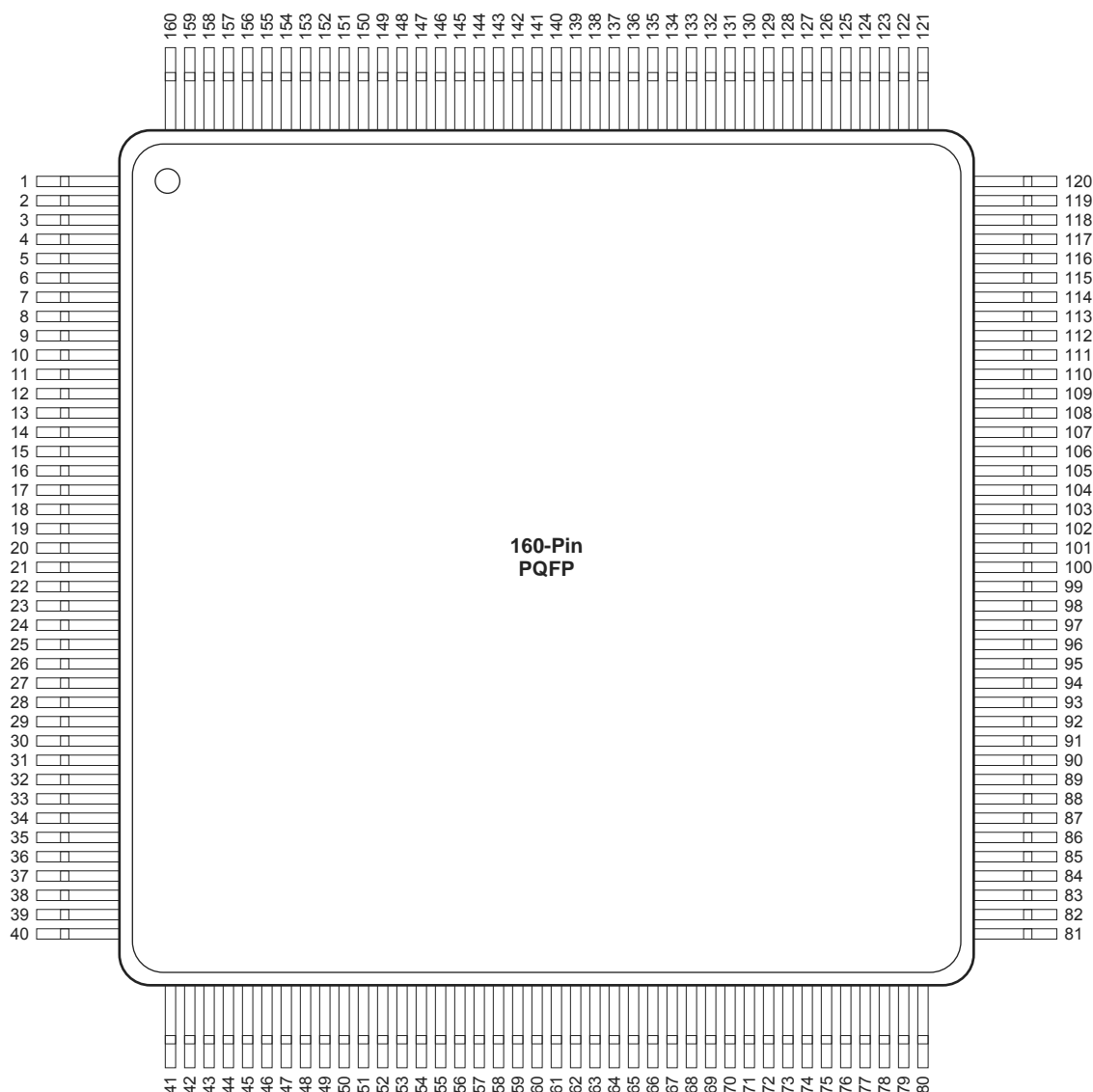http://www.microsemi.com/soc/products/solutions/package/docs.aspx

PQ144

144-Pin
PQFP

1

144

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

PQ160

**160-Pin
PQFP**

Note: This is the top view of the package

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
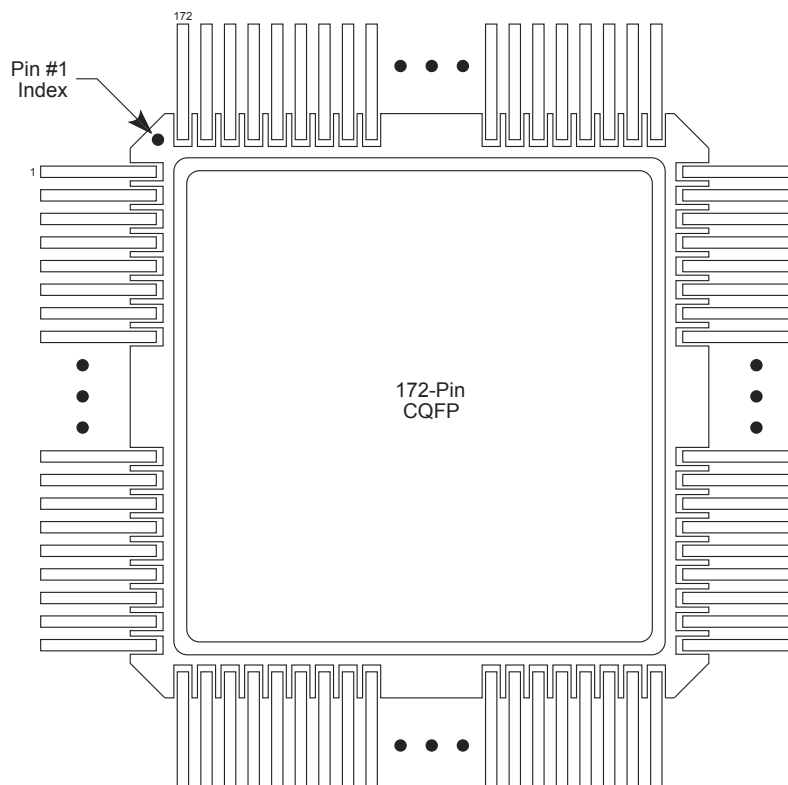http://www.microsemi.com/soc/products/solutions/package/docs.aspx

VQ100

100-Pin
VQFP

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx
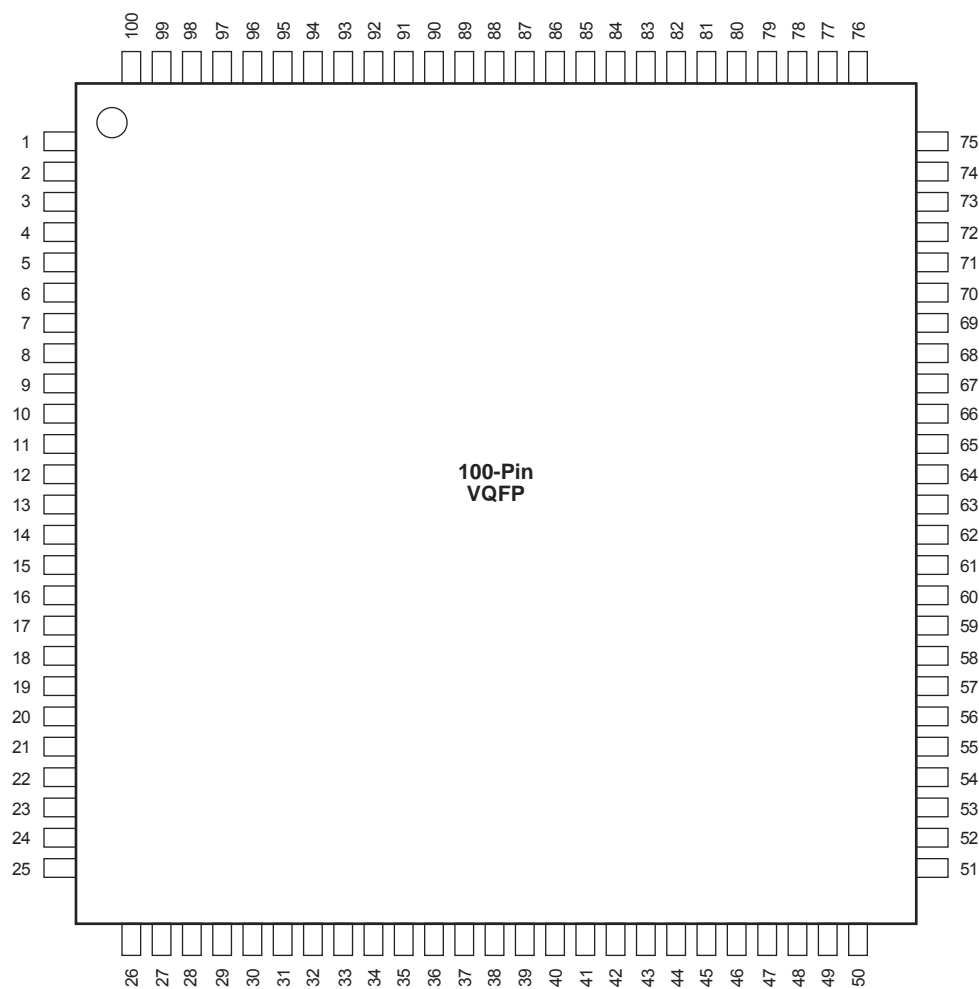
CQ172

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx
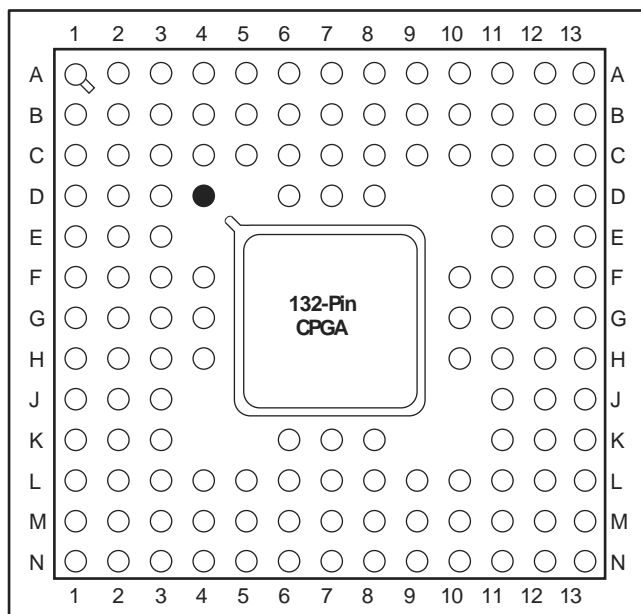
PG132

● Orientation Pin

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
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PG132		PG132	
Pin Number	**A1240A Function**	**Pin Number**	**A1240A Function**
A1	MODE	G3	VCC
B5	GND	G4	VCC
B6	CLKB, I/O	G10	VCC
B7	CLKA, I/O	G11	VCC
B8	PRA, I/O	G12	VCC
B9	GND	G13	VCC
B12	SDI, I/O	H13	GND
C3	DCLK, I/O	J2	GND
C5	GND	J3	GND
C6	PRB, I/O	J11	GND
C7	VCC	K7	VCC
C9	GND	K12	GND
D7	VCC	L5	GND
E3	GND	L7	VCC
E11	GND	L9	GND
E12	GND	M9	GND
F4	GND	N12	SDO
G2	VCC		

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

4 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each version of the datasheet.

Revision	Changes	Page
Revision 8 (January 2012)	The ACT 2 datasheet was formatted newly in the style used for current datasheets. The same information is present (other than noted in the list of changes for this revision) but divided into chapters.	N/A
	Package names used in Table 1 • ACT 2 Product Family Profile and throughout the document were revised to match standards given in *Package Mechanical Drawings* (SAR 27395).	I
	The description for SDO pins had earlier been removed from the datasheet and has now been included again, in the "Pin Descriptions" section (SAR 35819).	2-21
	SDO pin numbers had earlier been removed from package pin assignment tables in the datasheet, and have now been restored to the pin tables (SAR 35819).	3-2
Revision 7 (June 2006)	The "Ordering Information" section was revised to include RoHS information.	II
Revision 6 (December 2000)	In the "PG176" package, pin A3 was incorrectly assigned as CLKA, I/O. A3 is a user I/O. Pin A9 is CLKA, I/O.	3-21

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