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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	140
Number of Gates	8000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Through Hole
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	176-BCPGA
Supplier Device Package	176-CPGA (39.88x39.88)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microsemi/a1280a-pg176c">https://www.e-xfl.com/product-detail/microsemi/a1280a-pg176c</a>

## Ordering Information



## Package Thermal Characteristics

The device junction to case thermal characteristic is  $\theta_{jc}$ , and the junction to ambient air characteristic is  $\theta_{ja}$ . The thermal characteristics for  $\theta_{ja}$  are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a PQ160 package at commercial temperature and still air is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja} \text{ °C/W}} = \frac{150^{\circ}\text{C} - 70^{\circ}\text{C}}{33^{\circ}\text{C/W}} = 2.4 \text{ W}$$

EQ 1

**Table 2-4 • Package Thermal Characteristics**

Package Type*	Pin Count	$\theta_{jc}$	$\theta_{ja}$ Still Air	$\theta_{ja}$ 300 ft./min.	Units
Ceramic Pin Grid Array	100	5	35	17	°C/W
	132	5	30	15	°C/W
	176	8	23	12	°C/W
Ceramic Quad Flatpack	172	8	25	15	°C/W
Plastic Quad Flatpack <sup>1</sup>	100	13	48	40	°C/W
	144	15	40	32	°C/W
	160	15	38	30	°C/W
Plastic Leaded Chip Carrier	84	12	37	28	°C/W
Very Thin Quad Flatpack	100	12	43	35	°C/W
Thin Quad Flatpack	176	15	32	25	°C/W

Notes: (Maximum Power in Still Air)

1. Maximum power dissipation values for PQFP packages are 1.9 W (PQ100), 2.3 W (PQ144), and 2.4 W (PQ160).
2. Maximum power dissipation for PLCC packages is 2.7 W.
3. Maximum power dissipation for VQFP packages is 2.3 W.
4. Maximum power dissipation for TQFP packages is 3.1 W.

## Power Dissipation

$$P = [\text{ICC standby} + \text{ICC active}] * V_{CC} + \text{IOL} * \text{VOL} * N + \text{IOH} * (V_{CC} - \text{VOH}) * M$$

EQ 2

where:

ICC standby is the current flowing when no inputs or outputs are changing

ICC active is the current flowing due to CMOS switching.

IOL and IOH are TTL sink/source currents.

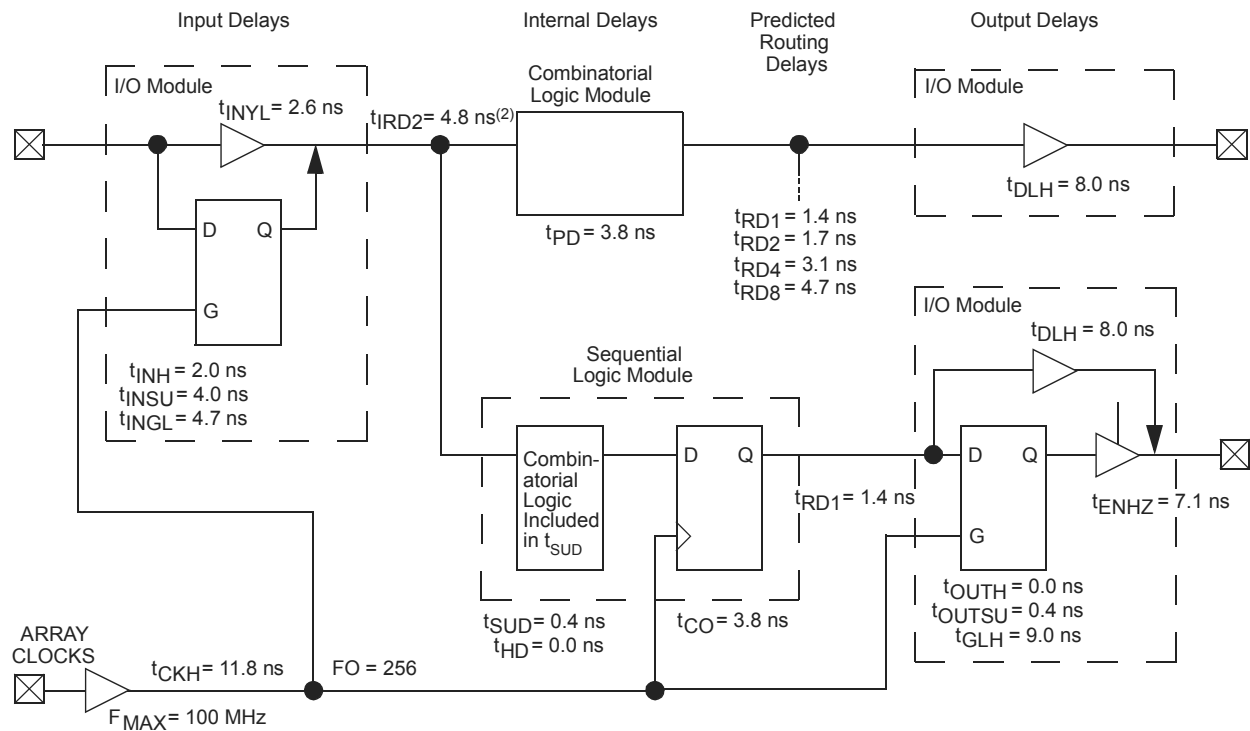
VOL and VOH are TTL level output voltages.

N is the number of outputs driving TTL loads to VOL.

M is the number of outputs driving TTL loads to VOH.

An accurate determination of N and M is problematical because their values depend on the family type, design details, and on the system I/O. The power can be divided into two components: static and active.

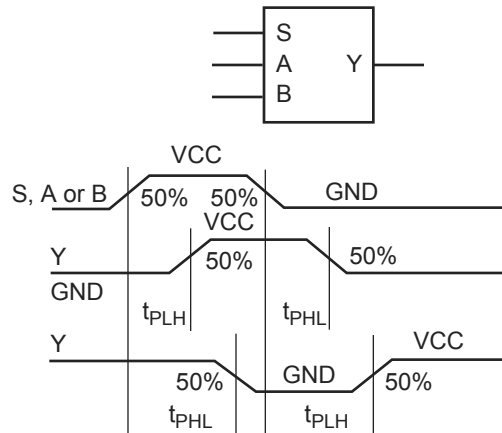
## ACT 2 Timing Model<sup>1</sup>



Notes:

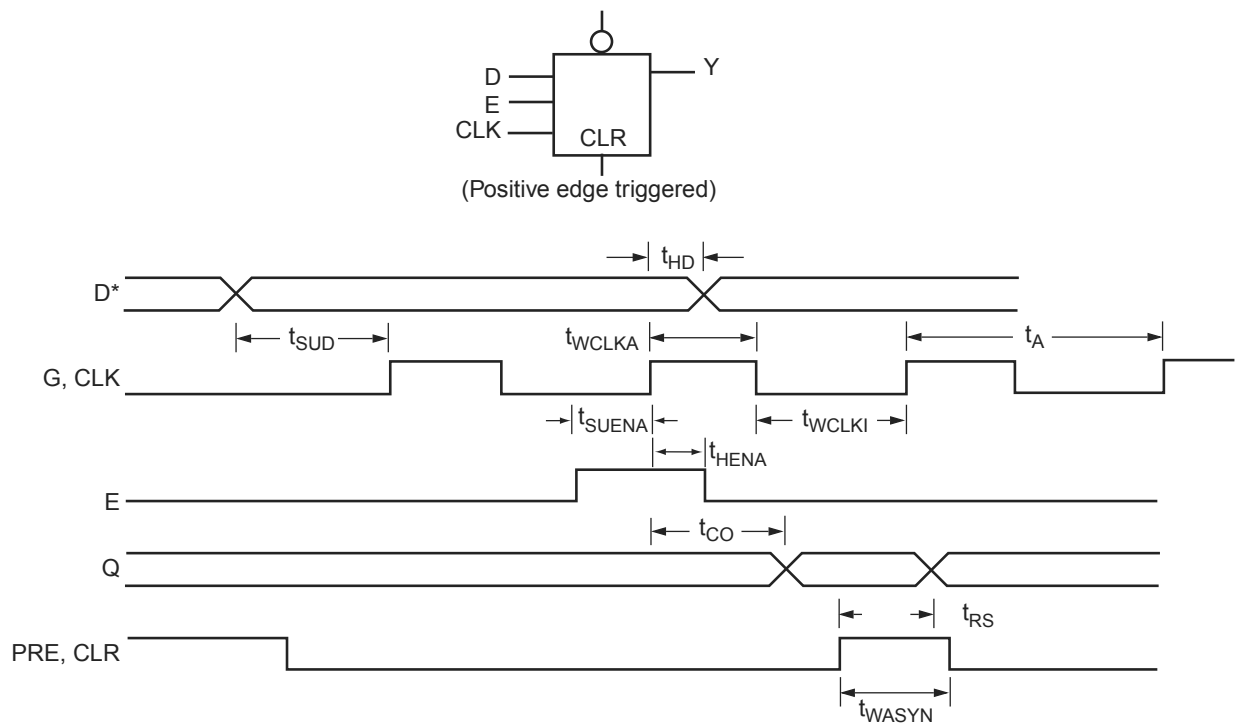
1. Values shown for A1240A-2 at worst-case commercial conditions.
2. Input module predicted routing delay

**Figure 2-1 • Timing Model**



**Figure 2-5 • Module Delays**

## Sequential Module Timing Characteristics



*Note: D represents all data functions involving A, B, and S for multiplexed flip-flops.*

**Figure 2-6 • Flip-Flops and Latches**

## Timing Derating Factor (Temperature and Voltage)

**Table 2-9 • Timing Derating Factor (Temperature and Voltage)**

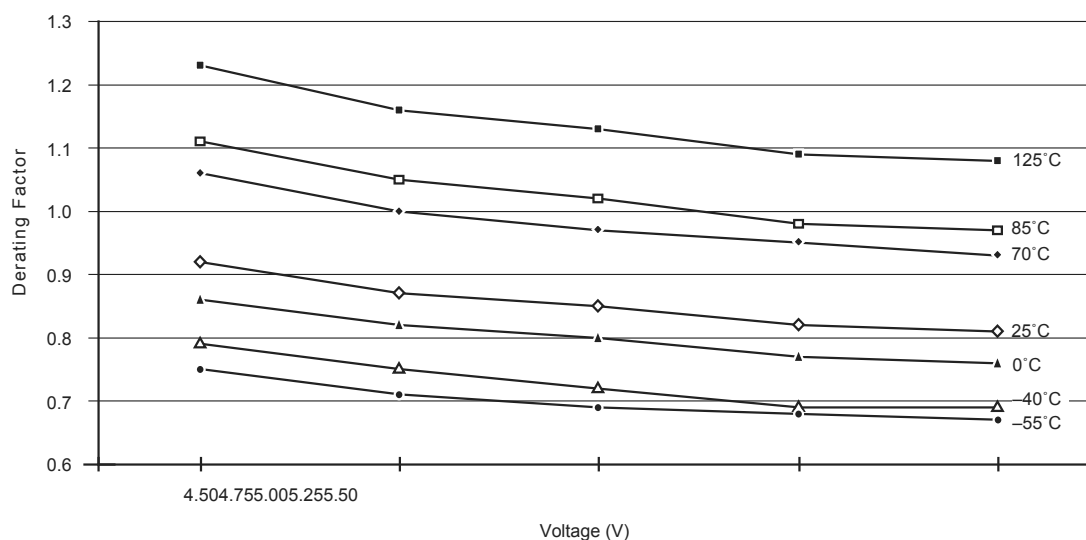
(Commercial Minimum/Maximum Specification) x	Industrial		Military	
	Min.	Max.	Min.	Max.
	0.69	1.11	0.67	1.23

**Table 2-10 • Timing Derating Factor for Designs at Typical Temperature ( $T_J = 25^\circ\text{C}$ ) and Voltage (5.0 V)**

(Commercial Maximum Specification) x	0.85
--------------------------------------	------

**Table 2-11 • Temperature and Voltage Derating Factors  
(normalized to Worst-Case Commercial,  $T_J = 4.75\text{ V}$ ,  $70^\circ\text{C}$ )**

	-55	-40	0	25	70	85	125
<b>4.50</b>	0.75	0.79	0.86	0.92	1.06	1.11	1.23
<b>4.75</b>	0.71	0.75	0.82	0.87	1.00	1.05	1.13
<b>5.00</b>	0.69	0.72	0.80	0.85	0.97	1.02	1.13
<b>5.25</b>	0.68	0.69	0.77	0.82	0.95	0.98	1.09
<b>5.50</b>	0.67	0.69	0.76	0.81	0.93	0.97	1.08



*Note: This derating factor applies to all routing and propagation delays.*

**Figure 2-9 • Junction Temperature and Voltage Derating Curves  
(normalized to Worst-Case Commercial,  $T_J = 4.75\text{ V}$ ,  $70^\circ\text{C}$ )**

## A1225A Timing Characteristics (continued)

Table 2-13 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C

I/O Module Input Propagation Delays			–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description			Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>INYH</sub>	Pad to Y High			2.9		3.3		3.8	ns
t <sub>INYL</sub>	Pad to Y Low			2.6		3.0		3.5	ns
t <sub>INGH</sub>	G to Y High			5.0		5.7		6.6	ns
t <sub>INGL</sub>	G to Y Low			4.7		5.4		6.3	ns
<b>Input Module Predicted Input Routing Delays*</b>									
t <sub>IRD1</sub>	FO = 1 Routing Delay			4.1		4.6		5.4	ns
t <sub>IRD2</sub>	FO = 2 Routing Delay			4.6		5.2		6.1	ns
t <sub>IRD3</sub>	FO = 3 Routing Delay			5.3		6.0		7.1	ns
t <sub>IRD4</sub>	FO = 4 Routing Delay			5.7		6.4		7.6	ns
t <sub>IRD8</sub>	FO = 8 Routing Delay			7.4		8.3		9.8	ns
<b>Global Clock Network</b>									
t <sub>CKH</sub>	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		11.8		13.0		15.7	
t <sub>CKL</sub>	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		12.0		13.2		15.9	
t <sub>PWH</sub>	Minimum Pulse Width High	FO = 32	3.4		4.1		4.5		ns
		FO = 256	3.8		4.5		5.0		
t <sub>PWL</sub>	Minimum Pulse Width Low	FO = 32	3.4		4.1		4.5		ns
		FO = 256	3.8		4.5		5.0		
t <sub>CKSW</sub>	Maximum Skew	FO = 32		0.7		0.7		0.7	ns
		FO = 256		3.5		3.5		3.5	
t <sub>SUEXT</sub>	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t <sub>HEXT</sub>	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t <sub>P</sub>	Minimum Period	FO = 32	7.7		8.3		9.1		ns
		FO = 256	8.1		8.8		10.0		
f <sub>MAX</sub>	Maximum Frequency	FO = 32		130.0		120.0		110.0	ns
		FO = 256		125.0		115.0		100.0	

Note: \*These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

## A1240A Timing Characteristics (continued)

**Table 2-16 • A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C**

I/O Module Input Propagation Delays			–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description			Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>INYH</sub>	Pad to Y High			2.9		3.3		3.8	ns
t <sub>INYL</sub>	Pad to Y Low			2.6		3.0		3.5	ns
t <sub>INGH</sub>	G to Y High			5.0		5.7		6.6	ns
t <sub>INGL</sub>	G to Y Low			4.7		5.4		6.3	ns
<b>Input Module Predicted Input Routing Delays*</b>									
t <sub>IRD1</sub>	FO = 1 Routing Delay			4.2		4.8		5.6	ns
t <sub>IRD2</sub>	FO = 2 Routing Delay			4.8		5.4		6.4	ns
t <sub>IRD3</sub>	FO = 3 Routing Delay			5.4		6.1		7.2	ns
t <sub>IRD4</sub>	FO = 4 Routing Delay			5.9		6.7		7.9	ns
t <sub>IRD8</sub>	FO = 8 Routing Delay			7.9		8.9		10.5	ns
<b>Global Clock Network</b>									
t <sub>CKH</sub>	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		11.8		13.0		15.7	
t <sub>CKL</sub>	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		12.0		13.2		15.9	
t <sub>PWH</sub>	Minimum Pulse Width High	FO = 32	3.8		4.5		5.5		ns
		FO = 256	4.1		5.0		5.8		
t <sub>PWL</sub>	Minimum Pulse Width Low	FO = 32	3.8		4.5		5.5		ns
		FO = 256	4.1		5.0		5.8		
t <sub>CKSW</sub>	Maximum Skew	FO = 32		0.5		0.5		0.5	ns
		FO = 256		2.5		2.5		2.5	
t <sub>SUEXT</sub>	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t <sub>HEXT</sub>	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t <sub>P</sub>	Minimum Period	FO = 32	8.1		9.1		11.1		ns
		FO = 256	8.8		10.0		11.7		
f <sub>MAX</sub>	Maximum Frequency	FO = 32		125.0		110.0		90.0	ns
		FO = 256		115.0		100.0		85.0	

Note: \*These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.



## A1280A Timing Characteristics

**Table 2-18 • A1280A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C**

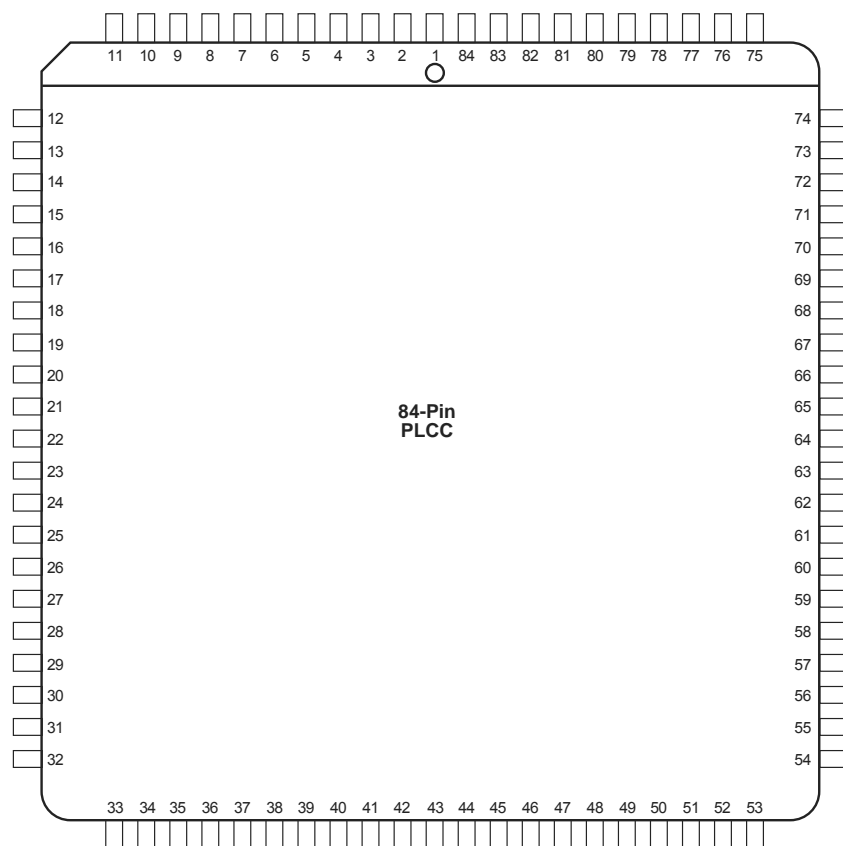
Logic Module Propagation Delays <sup>1</sup>		–2 Speed <sup>3</sup>		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PD1</sub>	Single Module		3.8		4.3		5.0	ns
t <sub>CO</sub>	Sequential Clock to Q		3.8		4.3		5.0	ns
t <sub>GO</sub>	Latch G to Q		3.8		4.3		5.0	ns
t <sub>RS</sub>	Flip-Flop (Latch) Reset to Q		3.8		4.3		5.0	ns
<b>Predicted Routing Delays<sup>2</sup></b>								
t <sub>RD1</sub>	FO = 1 Routing Delay		1.7		2.0		2.3	ns
t <sub>RD2</sub>	FO = 2 Routing Delay		2.5		2.8		3.3	ns
t <sub>RD3</sub>	FO = 3 Routing Delay		3.0		3.4		4.0	ns
t <sub>RD4</sub>	FO = 4 Routing Delay		3.7		4.2		4.9	ns
t <sub>RD8</sub>	FO = 8 Routing Delay		6.7		7.5		8.8	ns
<b>Sequential Timing Characteristics<sup>3,4</sup></b>								
t <sub>SUD</sub>	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		ns
t <sub>HD</sub>	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t <sub>SUENA</sub>	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		ns
t <sub>HENA</sub>	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t <sub>WCLKA</sub>	Flip-Flop (Latch) Clock Active Pulse Width	5.5		6.0		7.0		ns
t <sub>WASYN</sub>	Flip-Flop (Latch) Clock Asynchronous Pulse Width	5.5		6.0		7.0		ns
t <sub>A</sub>	Flip-Flop Clock Input Period	11.7		13.3		18.0		ns
t <sub>INH</sub>	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t <sub>INSU</sub>	Input Buffer Latch Setup	0.4		0.4		0.5		ns
t <sub>OUTH</sub>	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t <sub>OUTSU</sub>	Output Buffer Latch Setup	0.4		0.4		0.5		ns
f <sub>MAX</sub>	Flip-Flop (Latch) Clock Frequency		85.0		75.0		50.0	MHz

**Notes:**

1. For dual-module macros, use t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, t<sub>CO</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, or t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>SUD</sub>—whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
4. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

## 3 – Package Pin Assignments

### PL84



#### **Note**

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

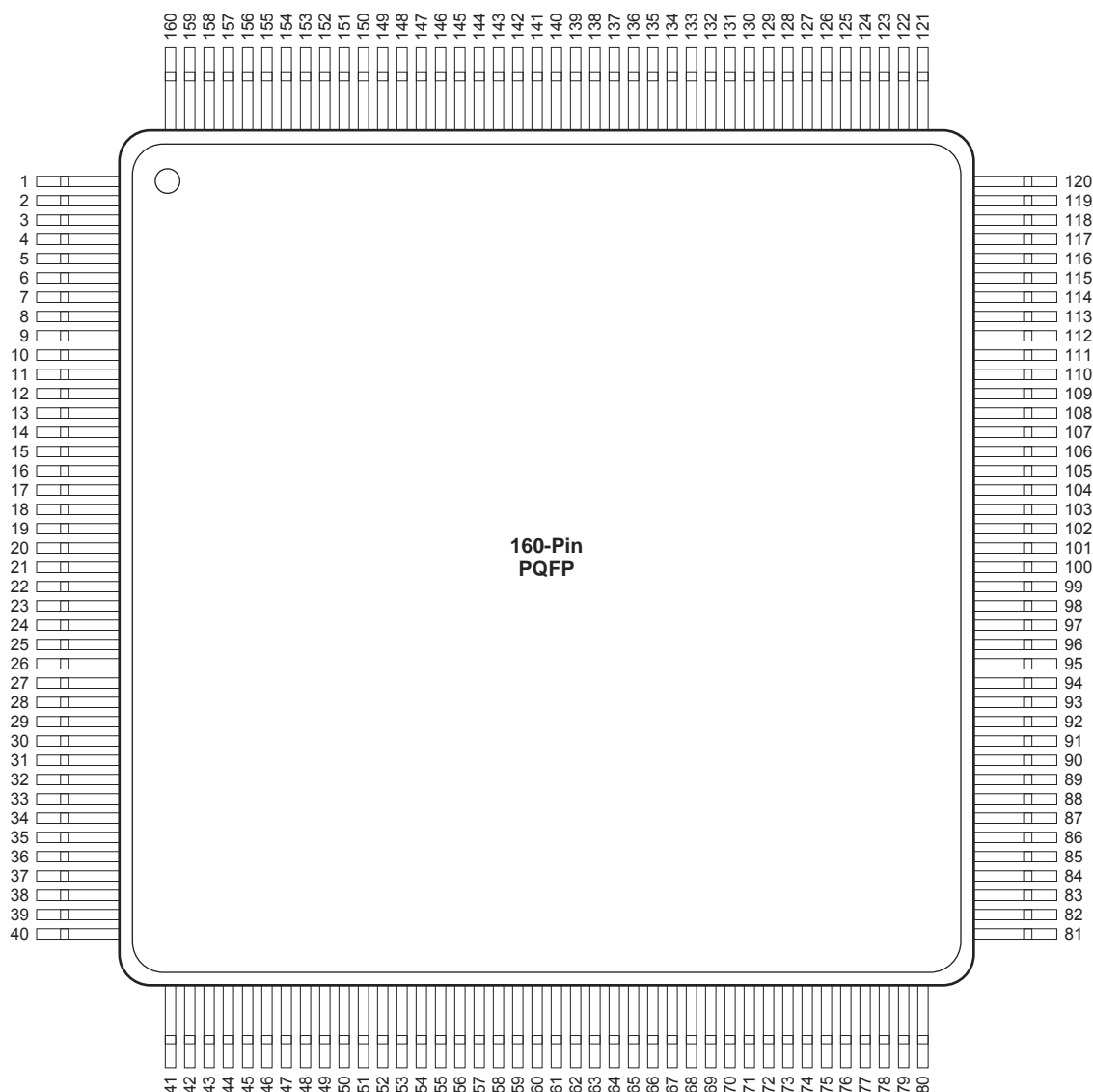
PQ100	
Pin Number	A1225A Function
2	DCLK, I/O
4	MODE
9	GND
16	VCC
17	VCC
22	GND
34	GND
40	VCC
46	GND
52	SDO
57	GND
64	GND

PQ100	
Pin Number	A1225A Function
65	VCC
66	VCC
67	VCC
72	GND
79	SDI, I/O
84	GND
87	PRA, I/O
89	CLKA, I/O
90	VCC
92	CLKB, I/O
94	PRB, I/O
96	GND

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

## PQ160



*Note:* This is the top view of the package

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

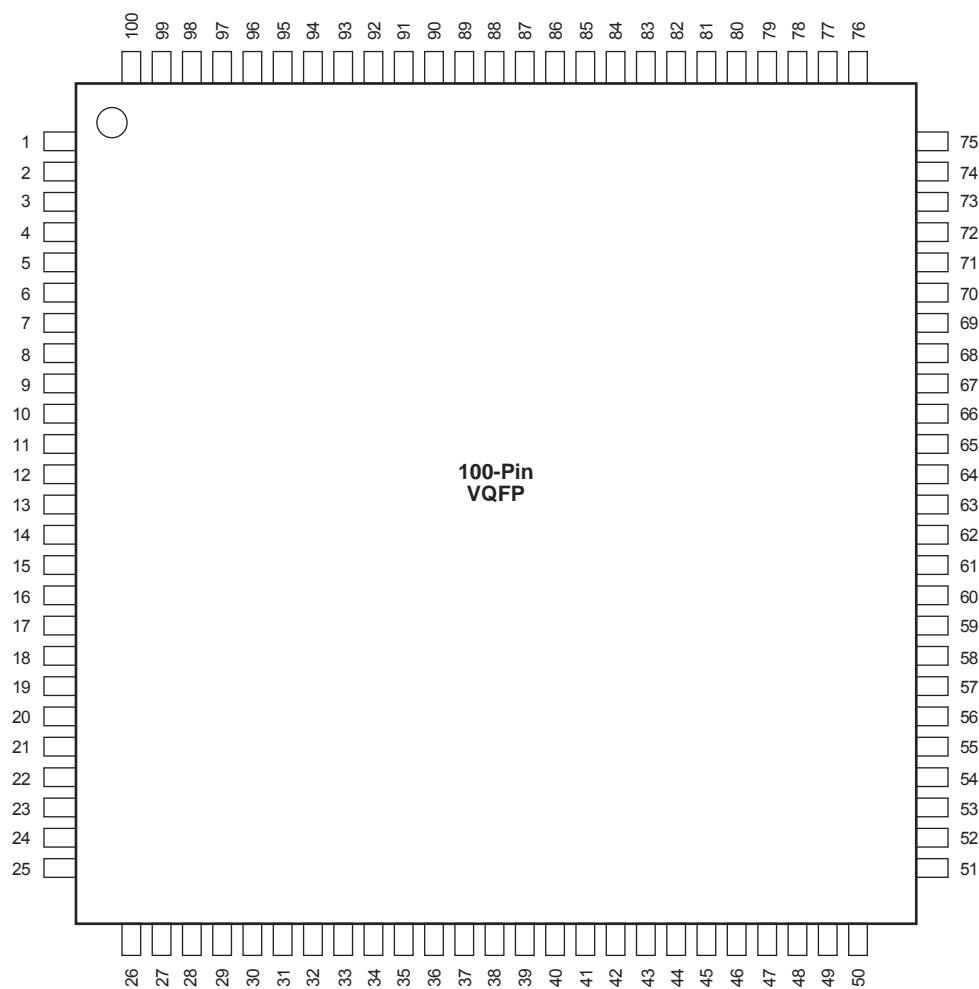
PQ160	
Pin Number	A1280A Function
2	DCLK, I/O
6	VCC
11	GND
16	PRB, I/O
18	CLKB, I/O
20	VCC
21	CLKA, I/O
23	PRA, I/O
30	GND
35	VCC
38	SDI, I/O
40	GND
44	GND
49	GND
54	VCC
57	VCC
58	VCC
59	GND
60	VCC
61	GND
64	GND

PQ160	
Pin Number	A1280A Function
69	GND
80	GND
82	SDO
86	VCC
89	GN
98	GND
99	GND
109	GND
114	VCC
120	GND
125	GND
130	GND
135	VCC
138	VCC
139	VCC
140	GND
145	GND
150	VCC
155	GND
159	MODE
160	GND

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

## VQ100



### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

VQ100	
Pin Number	A1225A Function
2	MODE
7	GND
14	VCC
15	VCC
20	GND
32	GND
38	VCC
44	GND
50	SDO
55	GND
62	GND
63	VCC

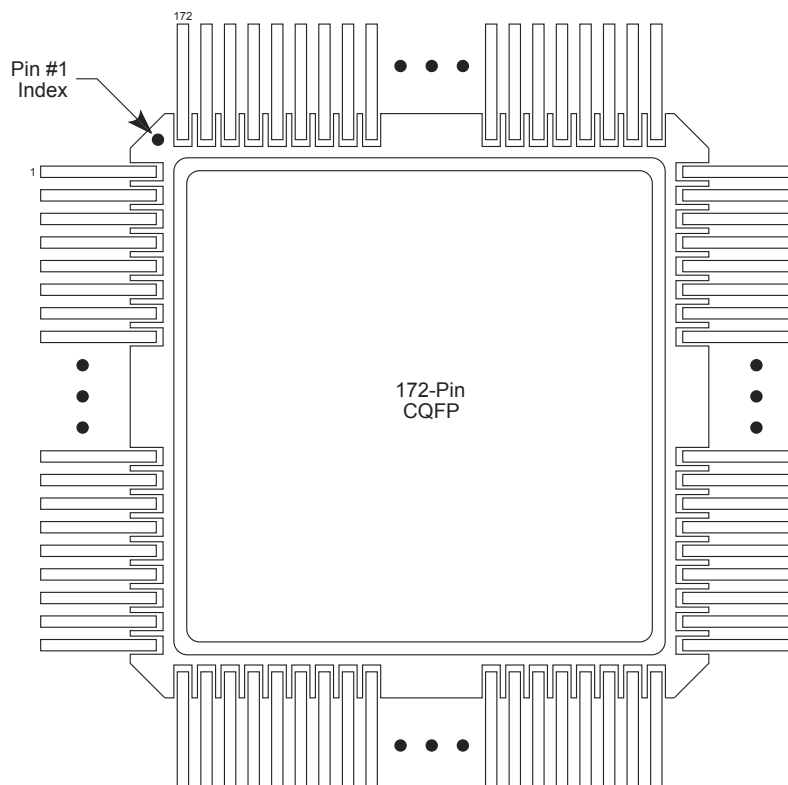
VQ100	
Pin Number	A1225A Function
64	VCC
65	VCC
70	GND
77	SDI, I/O
82	GND
85	PRA, I/O
87	CLKA, I/O
88	VCC
90	CLKB, I/O
92	PRB, I/O
94	GND
100	DCLK, I/O

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

## CQ172

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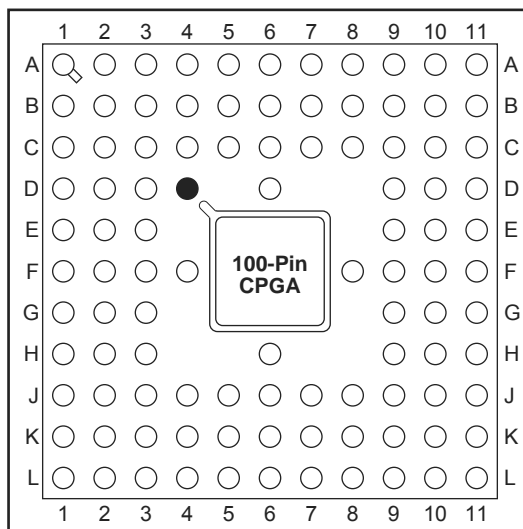
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### **Note**

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>



## PG100

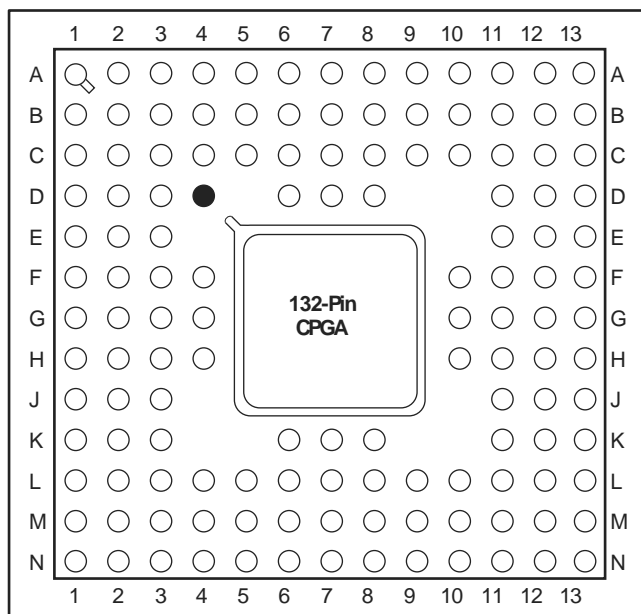


● Orientation Pin

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

## PG132



● Orientation Pin

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

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## 4 – Datasheet Information

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### List of Changes

The following table lists critical changes that were made in each version of the datasheet.

Revision	Changes	Page
Revision 8 (January 2012)	The ACT 2 datasheet was formatted newly in the style used for current datasheets. The same information is present (other than noted in the list of changes for this revision) but divided into chapters.	N/A
	Package names used in Table 1 • ACT 2 Product Family Profile and throughout the document were revised to match standards given in <i>Package Mechanical Drawings</i> (SAR 27395).	I
	The description for SDO pins had earlier been removed from the datasheet and has now been included again, in the "Pin Descriptions" section (SAR 35819).	2-21
	SDO pin numbers had earlier been removed from package pin assignment tables in the datasheet, and have now been restored to the pin tables (SAR 35819).	3-2
Revision 7 (June 2006)	The "Ordering Information" section was revised to include RoHS information.	II
Revision 6 (December 2000)	In the "PG176" package, pin A3 was incorrectly assigned as CLKA, I/O. A3 is a user I/O. Pin A9 is CLKA, I/O.	3-21

## Datasheet Categories

### ***Categories***

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

### ***Product Brief***

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

### ***Advance***

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

### ***Preliminary***

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

### ***Production***

This version contains information that is considered to be final.

## **Export Administration Regulations (EAR)**

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

## **Safety Critical, Life Support, and High-Reliability Applications Policy**

The products described in this advance status document may not have completed the Microsemi qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the Microsemi SoC Products Group Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the SoC Products Group's products is available at [http://www.microsemi.com/soc/documents/ORT\\_Report.pdf](http://www.microsemi.com/soc/documents/ORT_Report.pdf). Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local sales office for additional reliability information.



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