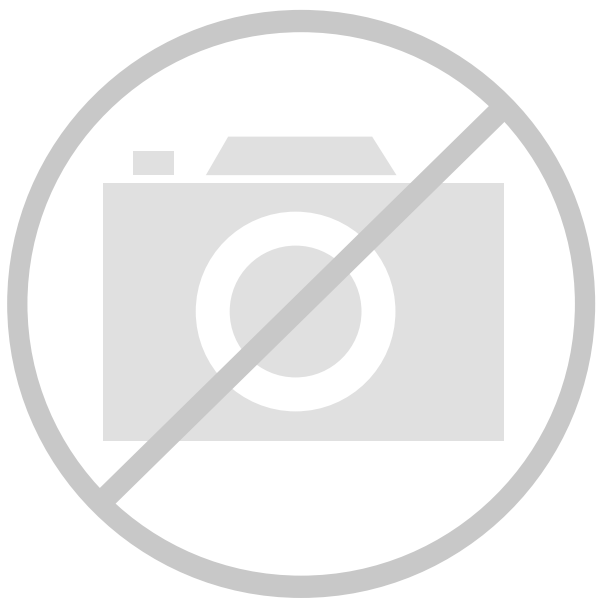




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	140
Number of Gates	8000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Through Hole
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	176-BCPGA
Supplier Device Package	176-CPGA (39.88x39.88)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1280a-pg176m

Ordering Information

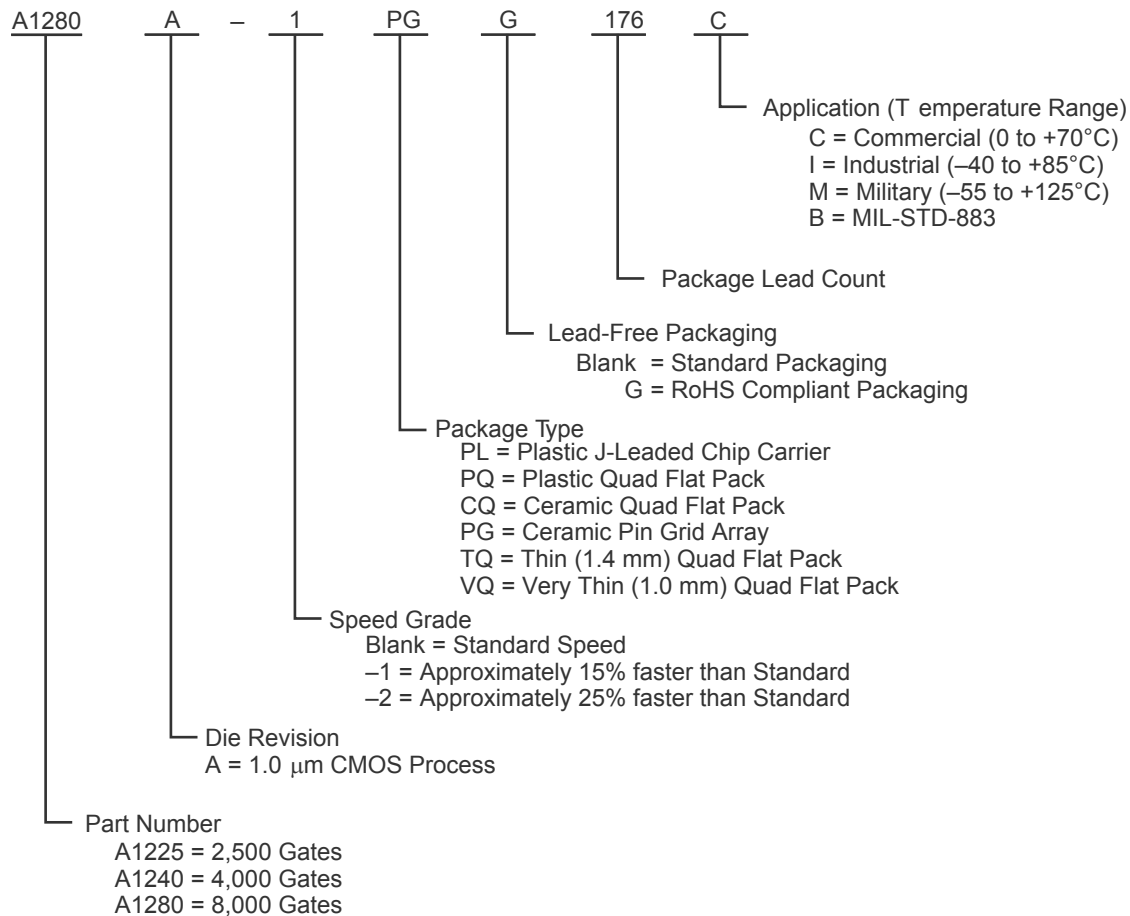


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2 – Detailed Specifications

Operating Conditions

Table 2-1 • Absolute Maximum Ratings¹

Symbol	Parameter	Limits	Units
VCC	DC supply voltage	–0.5 to +7.0	V
VI	Input voltage	–0.5 to VCC + 0.5	V
VO	Output voltage	–0.5 to VCC + 0.5	V
IIO	I/O source sink current ²	±20	mA
T _{STG}	Storage temperature	–65 to +150	°C

Notes:

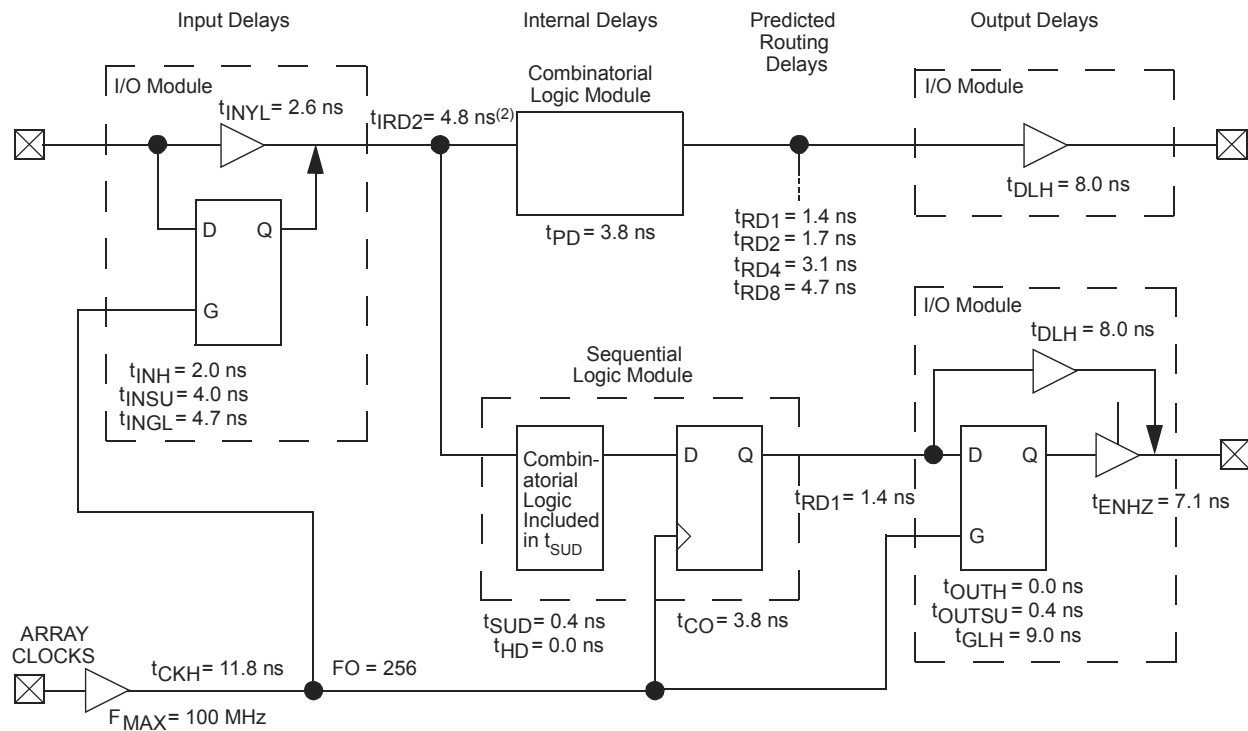
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.
2. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND –0.5 V, the internal protection diodes will be forward biased and can draw excessive current.

Table 2-2 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature range*	0 to +70	–40 to +85	–55 to +125	°C
Power supply tolerance	±5	±10	±10	%VCC

Note: *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.

ACT 2 Timing Model¹



Notes:

1. Values shown for A1240A-2 at worst-case commercial conditions.
2. Input module predicted routing delay

Figure 2-1 • Timing Model

Parameter Measurement

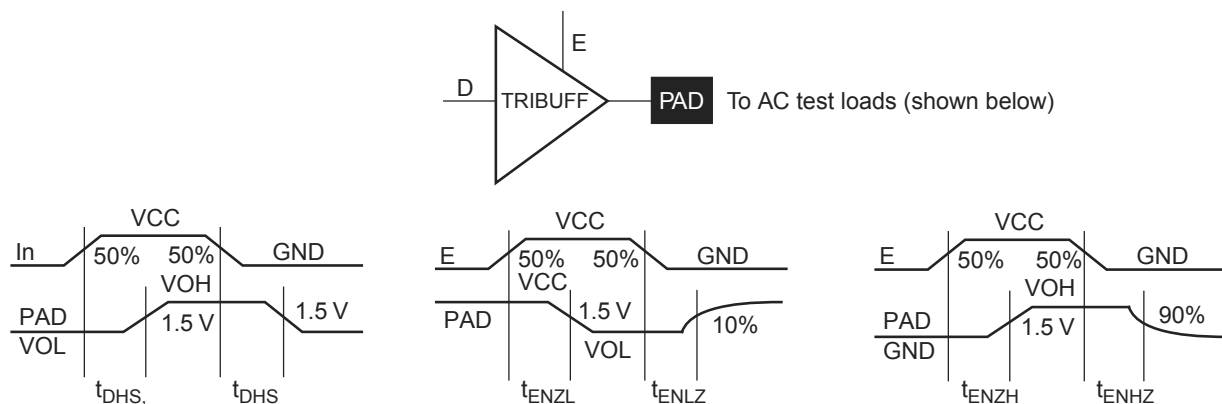


Figure 2-2 • Output Buffer Delays

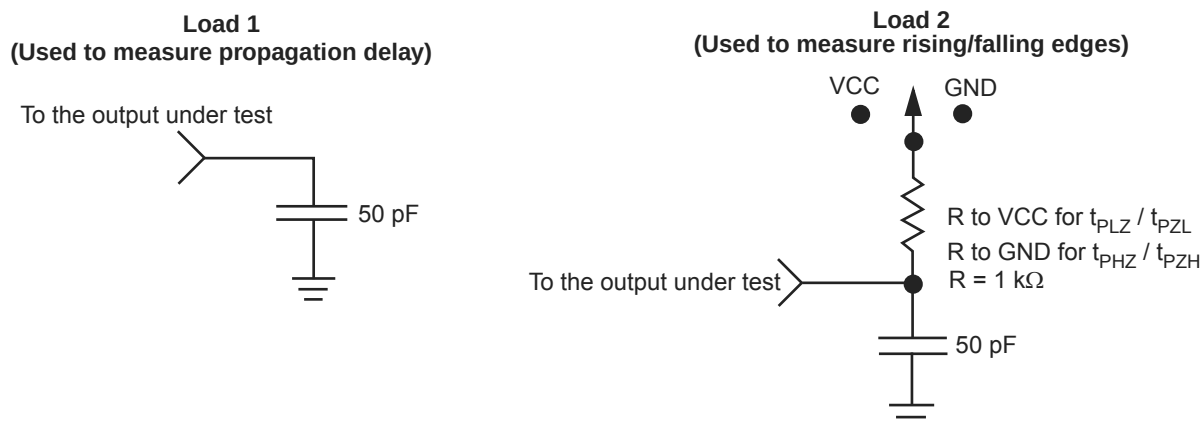


Figure 2-3 • AC Test Loads

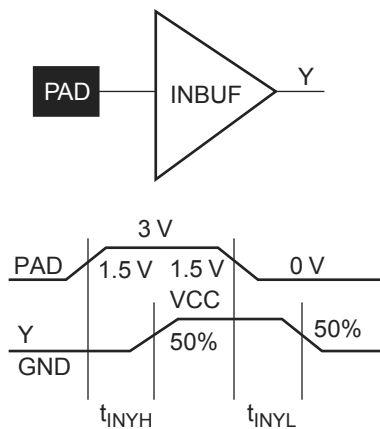


Figure 2-4 • Input Buffer Delays

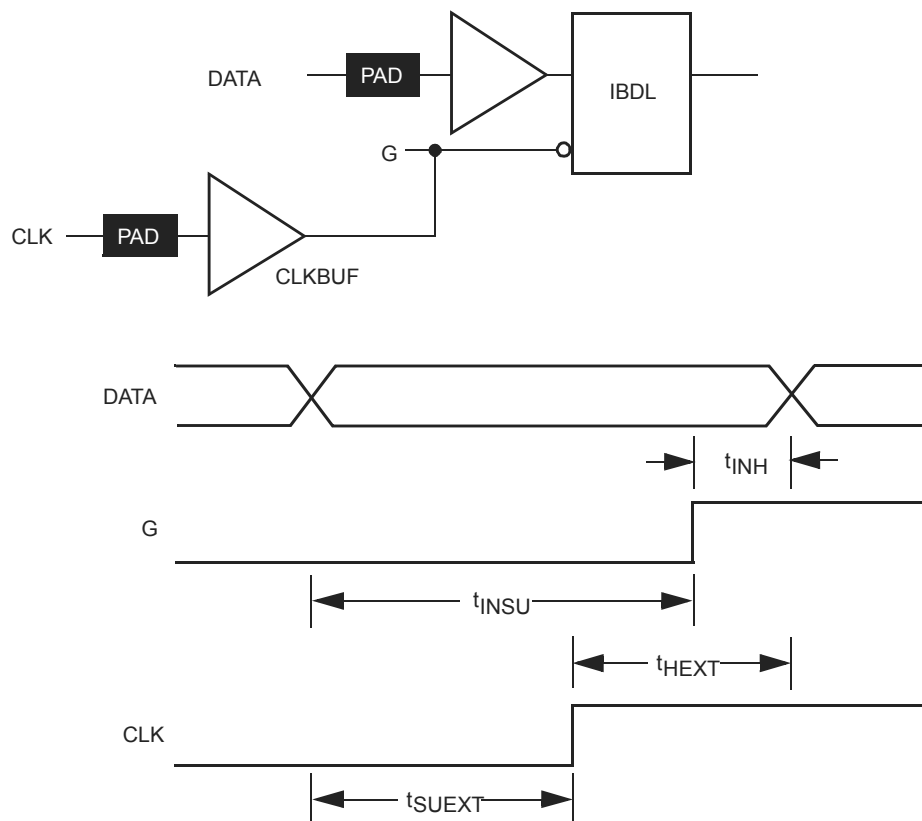


Figure 2-7 • Input Buffer Latches

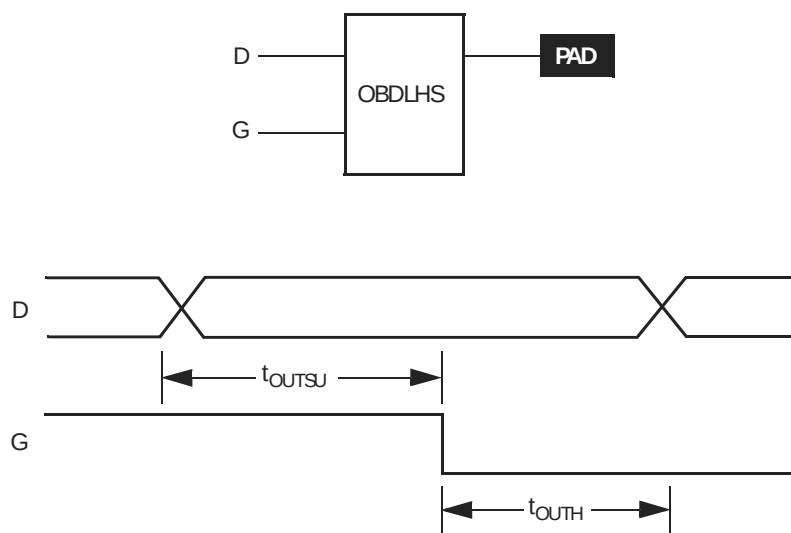


Figure 2-8 • Output Buffer Latches

A1225A Timing Characteristics

Table 2-12 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

Logic Module Propagation Delays ¹		–2 Speed ³		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD1}	Single Module		3.8		4.3		5.0	ns
t _{CO}	Sequential Clock to Q		3.8		4.3		5.0	ns
t _{GO}	Latch G to Q		3.8		4.3		5.0	ns
t _{RS}	Flip-Flop (Latch) Reset to Q		3.8		4.3		5.0	ns
Predicted Routing Delays²								
t _{RD1}	FO = 1 Routing Delay		1.1		1.2		1.4	ns
t _{RD2}	FO = 2 Routing Delay		1.7		1.9		2.2	ns
t _{RD3}	FO = 3 Routing Delay		2.3		2.6		3.0	ns
t _{RD4}	FO = 4 Routing Delay		2.8		3.1		3.7	ns
t _{RD8}	FO = 8 Routing Delay		4.4		4.9		5.8	ns
Sequential Timing Characteristics^{3,4}								
t _{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		ns
t _{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t _{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.5		5.0		6.0		ns
t _{WASYN}	Flip-Flop (Latch) Clock Asynchronous Pulse Width	4.5		5.0		6.0		ns
t _A	Flip-Flop Clock Input Period	9.4		11.0		13.0		ns
t _{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t _{INSU}	Input Buffer Latch Setup	0.4		0.4		0.5		ns
t _{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t _{OUTSU}	Output Buffer Latch Setup	0.4		0.4		0.5		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency		105.0		90.0		75.0	MHz

Notes:

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}—whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
4. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1225A Timing Characteristics (continued)

Table 2-13 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module Input Propagation Delays			–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description			Min.	Max.	Min.	Max.	Min.	Max.	
t _{INYH}	Pad to Y High			2.9		3.3		3.8	ns
t _{INYL}	Pad to Y Low			2.6		3.0		3.5	ns
t _{INGH}	G to Y High			5.0		5.7		6.6	ns
t _{INGL}	G to Y Low			4.7		5.4		6.3	ns
Input Module Predicted Input Routing Delays*									
t _{IRD1}	FO = 1 Routing Delay			4.1		4.6		5.4	ns
t _{IRD2}	FO = 2 Routing Delay			4.6		5.2		6.1	ns
t _{IRD3}	FO = 3 Routing Delay			5.3		6.0		7.1	ns
t _{IRD4}	FO = 4 Routing Delay			5.7		6.4		7.6	ns
t _{IRD8}	FO = 8 Routing Delay			7.4		8.3		9.8	ns
Global Clock Network									
t _{CKH}	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		11.8		13.0		15.7	
t _{CKL}	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		12.0		13.2		15.9	
t _{PWH}	Minimum Pulse Width High	FO = 32	3.4		4.1		4.5		ns
		FO = 256	3.8		4.5		5.0		
t _{PWL}	Minimum Pulse Width Low	FO = 32	3.4		4.1		4.5		ns
		FO = 256	3.8		4.5		5.0		
t _{CKSW}	Maximum Skew	FO = 32		0.7		0.7		0.7	ns
		FO = 256		3.5		3.5		3.5	
t _{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t _{HEXT}	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t _P	Minimum Period	FO = 32	7.7		8.3		9.1		ns
		FO = 256	8.1		8.8		10.0		
f _{MAX}	Maximum Frequency	FO = 32		130.0		120.0		110.0	ns
		FO = 256		125.0		115.0		100.0	

Note: *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1225A Timing Characteristics (continued)

Table 2-14 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

TTL Output Module Timing ¹		-2 Speed		-1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t _{DLH}	Data to Pad High		8.0		9.0		10.6	ns
t _{DHL}	Data to Pad Low		10.1		11.4		13.4	ns
t _{ENZH}	Enable Pad Z to High		8.9		10.0		11.8	ns
t _{ENZL}	Enable Pad Z to Low		11.6		13.2		15.5	ns
t _{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t _{ENLZ}	Enable Pad Low to Z		8.3		9.5		11.1	ns
t _{GLH}	G to Pad High		8.9		10.2		11.9	ns
t _{GHL}	G to Pad Low		11.2		12.7		14.9	ns
d _{TLH}	Delta Low to High		0.07		0.08		0.09	ns/pF
d _{THL}	Delta High to Low		0.12		0.13		0.16	ns/pF
CMOS Output Module Timing ¹								
t _{DLH}	Data to Pad High		10.1		11.5		13.5	ns
t _{DHL}	Data to Pad Low		8.4		9.6		11.2	ns
t _{ENZH}	Enable Pad Z to High		8.9		10.0		11.8	ns
t _{ENZL}	Enable Pad Z to Low		11.6		13.2		15.5	ns
t _{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t _{ENLZ}	Enable Pad Low to Z		8.3		9.5		11.1	ns
t _{GLH}	G to Pad High		8.9		10.2		11.9	ns
t _{GHL}	G to Pad Low		11.2		12.7		14.9	ns
d _{TLH}	Delta Low to High		0.12		0.13		0.16	ns/pF
d _{THL}	Delta High to Low		0.09		0.10		0.12	ns/pF

Notes:

1. Delays based on 50 pF loading.
2. SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.

A1240A Timing Characteristics (continued)

Table 2-17 • A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

TTL Output Module Timing ¹		-2 Speed		-1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t _{DLH}	Data to Pad High		8.0		9.0		10.6	ns
t _{DHL}	Data to Pad Low		10.1		11.4		13.4	ns
t _{ENZH}	Enable Pad Z to High		8.9		10.0		11.8	ns
t _{ENZL}	Enable Pad Z to Low		11.7		13.2		15.5	ns
t _{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t _{ENLZ}	Enable Pad Low to Z		8.4		9.5		11.1	ns
t _{GLH}	G to Pad High		9.0		10.2		11.9	ns
t _{GHL}	G to Pad Low		11.2		12.7		14.9	ns
d _{TLH}	Delta Low to High		0.07		0.08		0.09	ns/pF
d _{THL}	Delta High to Low		0.12		0.13		0.16	ns/pF
CMOS Output Module Timing ¹								
t _{DLH}	Data to Pad High		10.2		11.5		13.5	ns
t _{DHL}	Data to Pad Low		8.4		9.6		11.2	ns
t _{ENZH}	Enable Pad Z to High		8.9		10.0		11.8	ns
t _{ENZL}	Enable Pad Z to Low		11.7		13.2		15.5	ns
t _{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t _{ENLZ}	Enable Pad Low to Z		8.4		9.5		11.1	ns
t _{GLH}	G to Pad High		9.0		10.2		11.9	ns
t _{GHL}	G to Pad Low		11.2		12.7		14.9	ns
d _{TLH}	Delta Low to High		0.12		0.13		0.16	ns/pF
d _{THL}	Delta High to Low		0.09		0.10		0.12	ns/pF

Notes:

1. Delays based on 50 pF loading.
2. SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.

Table 2-20 • A1280A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

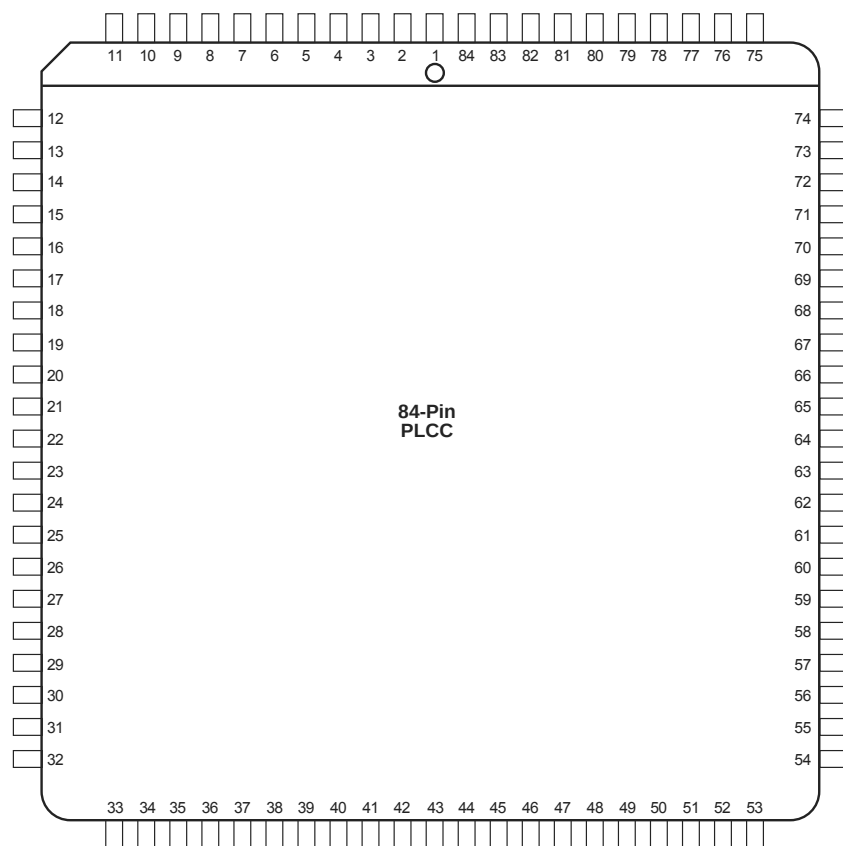
TTL Output Module Timing ¹		–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t _{DLH}	Data to Pad High		8.1		9.0		10.6	ns
t _{DHL}	Data to Pad Low		10.2		11.4		13.4	ns
t _{ENZH}	Enable Pad Z to High		9.0		10.0		11.8	ns
t _{ENZL}	Enable Pad Z to Low		11.8		13.2		15.5	ns
t _{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t _{ENLZ}	Enable Pad Low to Z		8.4		9.5		11.1	ns
t _{GLH}	G to Pad High		9.0		10.2		11.9	ns
t _{GHL}	G to Pad Low		11.3		12.7		14.9	ns
d _{TLH}	Delta Low to High		0.07		0.08		0.09	ns/pF
d _{THL}	Delta High to Low		0.12		0.13		0.16	ns/pF
CMOS Output Module Timing ¹								
t _{DLH}	Data to Pad High		10.3		11.5		13.5	ns
t _{DHL}	Data to Pad Low		8.5		9.6		11.2	ns
t _{ENZH}	Enable Pad Z to High		9.0		10.0		11.8	ns
t _{ENZL}	Enable Pad Z to Low		11.8		13.2		15.5	ns
t _{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t _{ENLZ}	Enable Pad Low to Z		8.4		9.5		11.1	ns
t _{GLH}	G to Pad High		9.0		10.2		11.9	ns
t _{GHL}	G to Pad Low		11.3		12.7		14.9	ns
d _{TLH}	Delta Low to High		0.12		0.13		0.16	ns/pF
d _{THL}	Delta High to Low		0.09		0.10		0.12	ns/pF

Notes:

1. Delays based on 50 pF loading.
2. SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.

3 – Package Pin Assignments

PL84



Note

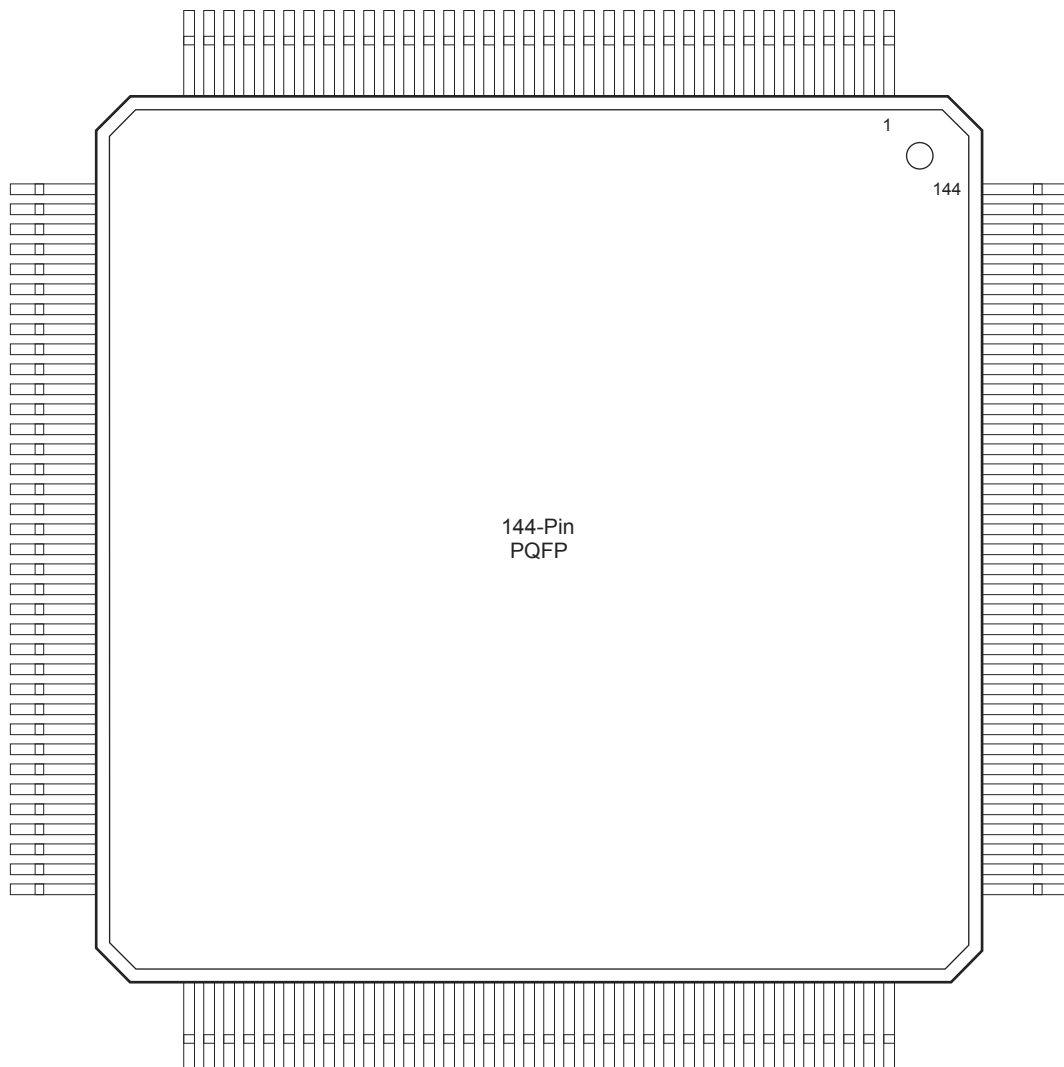
For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

PL84			
Pin Number	A1225A Function	A1240A Function	A1280A Function
2	CLKB, I/O	CLKB, I/O	CLKB, I/O
4	PRB, I/O	PRB, I/O	PRB, I/O
6	GND	GND	GND
10	DCLK, I/O	DCLK, I/O	DCLK, I/O
12	MODE	MODE	MODE
22	VCC	VCC	VCC
23	VCC	VCC	VCC
28	GND	GND	GND
43	VCC	VCC	VCC
49	GND	GND	GND
52	SDO	SDO	SDO
63	GND	GND	GND
64	VCC	VCC	VCC
65	VCC	VCC	VCC
70	GND	GND	GND
76	SDI, I/O	SDI, I/O	SDI, I/O
81	PRA, I/O	PRA, I/O	PRA, I/O
83	CLKA, I/O	CLKA, I/O	CLKA, I/O
84	VCC	VCC	VCC

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

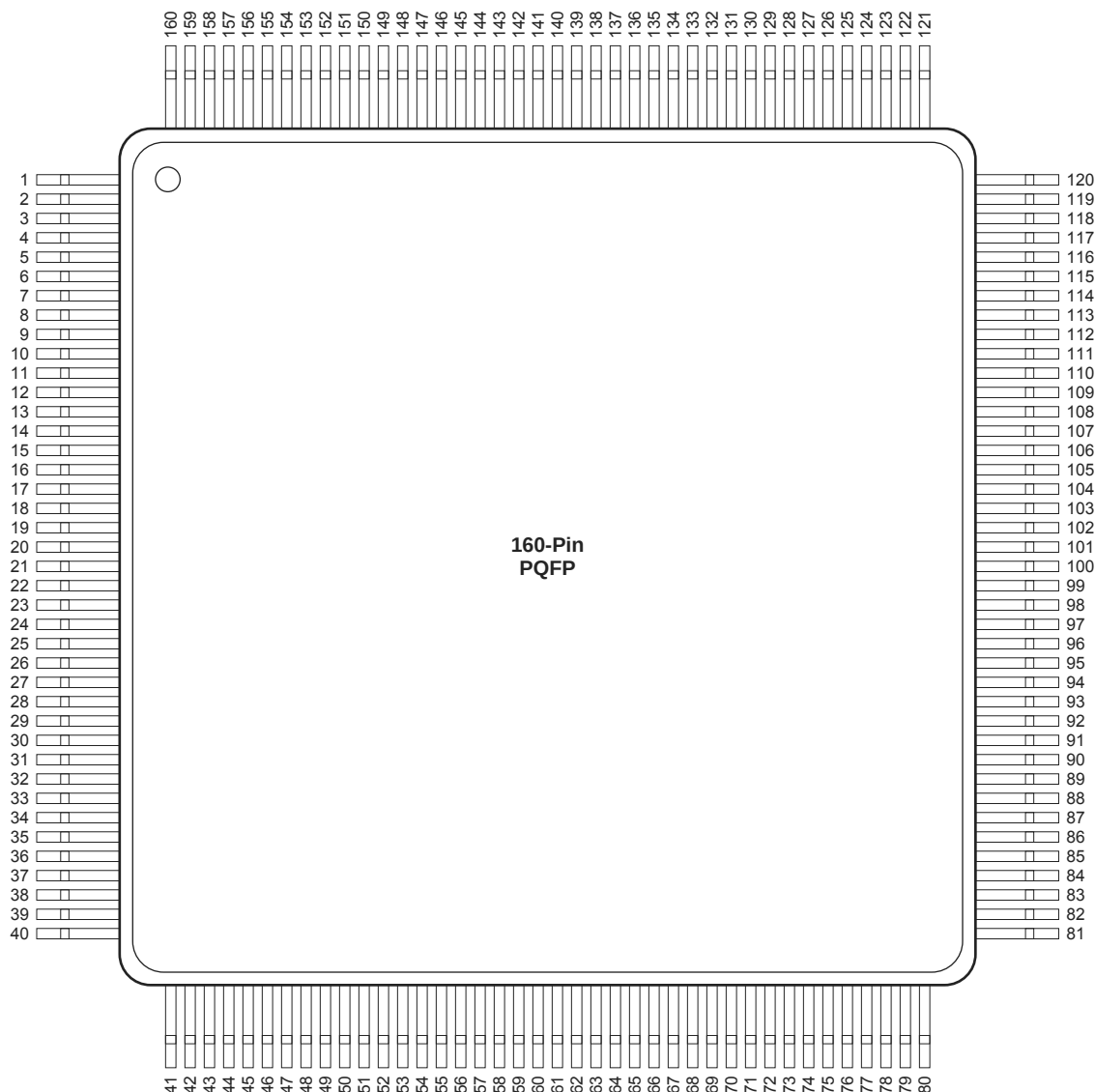
PQ144



Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

PQ160

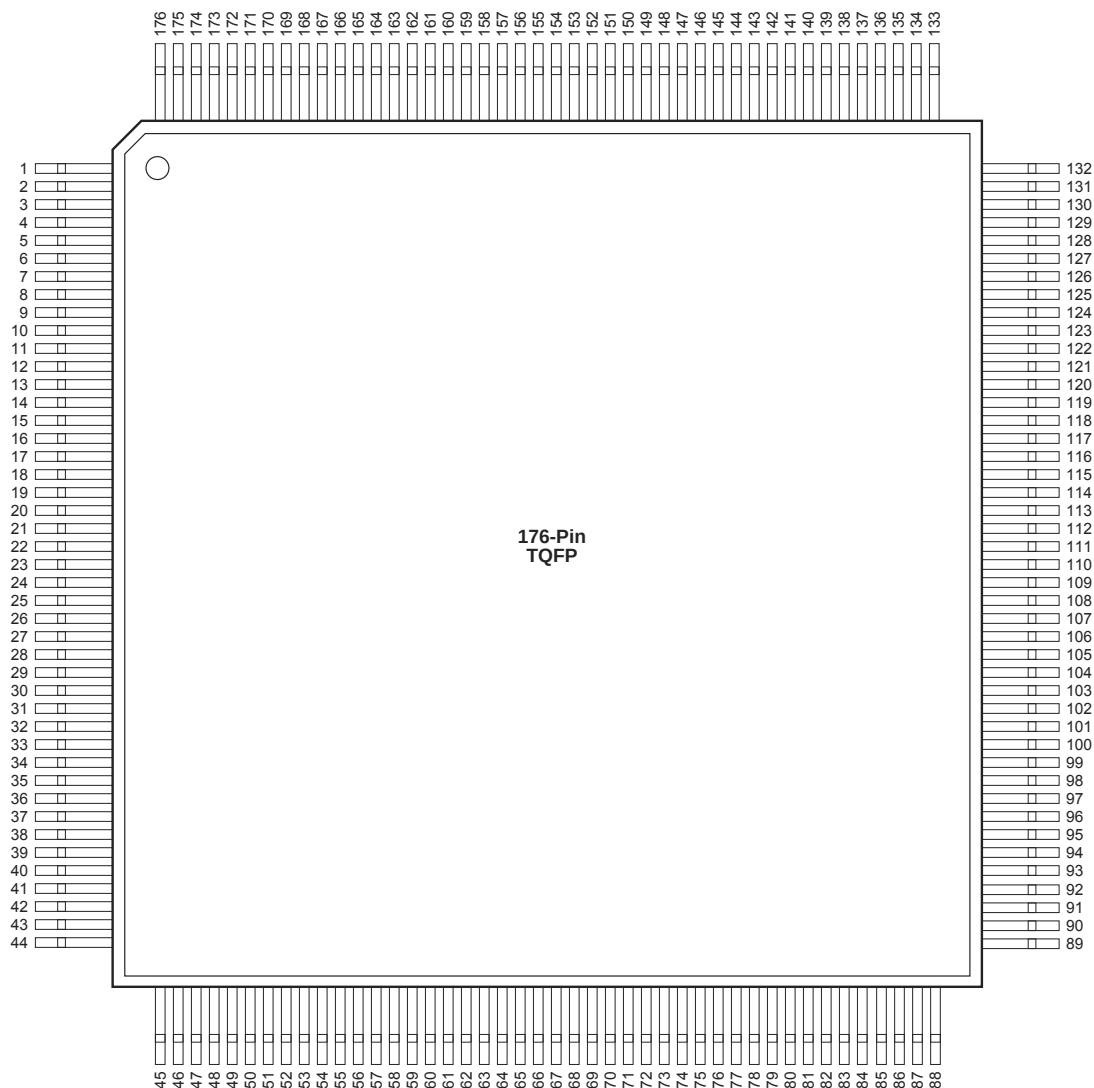


Note: This is the top view of the package

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

TQ176



Note

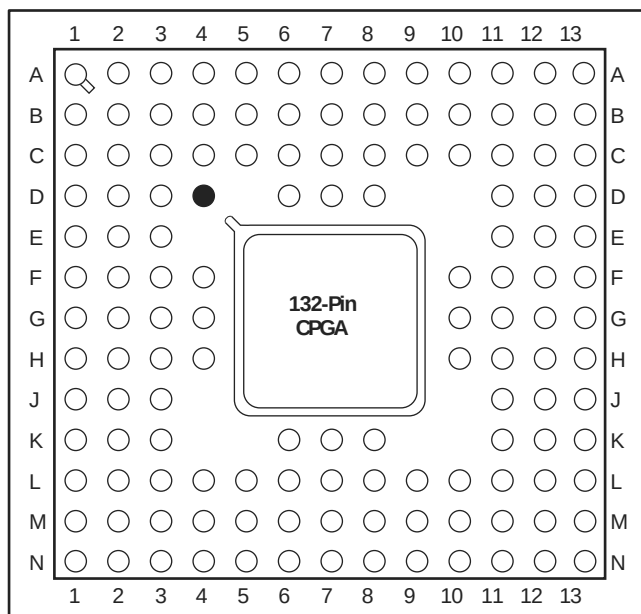
For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

PG100		PG100	
Pin Number	A1225A Function	Pin Number	A1225A Function
A4	PRB, I/O	E11	VCC
A7	PRA, I/O	F3	VCC
B6	VCC	F9	VCC
C2	MODE	F10	VCC
C3	DCLK, I/O	F11	GND
C5	GND	G1	VCC
C6	CLKA, I/O	G3	GND
C7	GND	G9	GND
C8	SDI, I/O	J5	GND
D6	CLKB, I/O	J7	GND
D10	GND	J9	SDO
E3	GND	K6	VCC

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG132



● Orientation Pin

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

PG176	
Pin Number	A1280A Function
A9	CLKA, I/O
B3	DCLK, I/O
B8	CLKB, I/O
B14	SDI, I/O
C3	MODE
C8	GND
C9	PRA, I/O
D4	GND
D5	VCC
D6	GND
D7	PRB, I/O
D8	VCC
D10	GND
D11	VCC
D12	GND
E4	GND
E12	GND
F4	VCC
F12	GND
G4	GND
G12	VCC
H2	VCC

PG176	
Pin Number	A1280A Function
H3	VCC
H4	GND
H12	GND
H13	VCC
H14	VCC
J4	VCC
J12	GND
J13	GND
J14	VCC
K4	GND
K12	GND
L4	GND
M4	GND
M5	VCC
M6	GND
M8	GND
M10	GND
M11	VCC
M12	GND
N8	VCC
P13	SDO

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

