Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	125
Number of Gates	8000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1280a-pq160m

Product Plan

Device/Package	Speed Grade[1]			Application[1]			
	Std.	−1	−2	C	I	M	B
A1225A Device							
84-Pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	−	−
100-Pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	✓	−	−
100-Pin Very Thin Quad Flatpack (VQ)	✓	✓	✓	✓	−	−	−
100-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	−	−	−
A1240A Device							
84-Pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	−	−
132-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	−	✓	✓
144-Pin Plastic Quad Flat Pack (PQ)	✓	✓	✓	✓	✓	−	−
176-Pin Thin (1.4 mm) Quad Flat Pack (TQ)	✓	✓	✓	✓	−	−	−
A1280A Device							
160-Pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	✓	−	−
172-Pin Ceramic Quad Flatpack (CQ)	✓	✓	✓	✓	−	✓	✓
176-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	−	✓	✓
176-Pin Thin (1.4 mm) Quad Flat Pack (TQ)	✓	✓	✓	✓	−	−	−

Notes:

1. *Applications:*
   C = Commercial
   I = Industrial
   M = Military
   B = MIL-STD-883

Availability:
✓ = Available
P = Planned
− = Not planned

Speed Grade:
−1 = Approx. 15% faster than Std.
−2 = Approx. 25% faster than Std.

2. *Contact your Microsemi SoC Products Group sales representative for product availability.*

Device Resources

Device Series	Logic Modules	Gates	User I/Os									
			PG176	PG132	PG100	PQ160	PQ144	PQ100	PL84	CQ172	TQ176	VQ100
A1225A	451	2,500	−	−	83	−	−	83	72	−	−	83
A1240A	684	4,000	−	104	−	−	104	−	72	−	104	−
A1280A	1,232	8,000	140	−	−	125	−	−	72	140	140	−

Contact your local Microsemi SoC Products Group representative for device availability:

http://www.microsemi.com/soc/contact/default.aspx.

Microsemi

1 – ACT 2 Family Overview

General Description

The ACT 2 family represents Actel's second generation of field programmable gate arrays (FPGAs). The ACT 2 family presents a two-module architecture, consisting of C-modules and S-modules. These modules are optimized for both combinatorial and sequential designs. Based on Actel's patented channeled array architecture, the ACT 2 family provides significant enhancements to gate density and performance while maintaining downward compatibility with the ACT 1 design environment and upward compatibility with the ACT 3 design environment. The devices are implemented in silicon gate, 1.0-µm, two-level metal CMOS, and employ Actel's PLICE® antifuse technology. This revolutionary architecture offers gate array design flexibility, high performance, and fast time-to-production with user programming. The ACT 2 family is supported by the Designer and Designer Advantage Systems, which offers automatic pin assignment, validation of electrical and design rules, automatic placement and routing, timing analysis, user programming, and diagnostic probe capabilities. The systems are supported on the following platforms: 386/486™ PC, Sun™, and HP™ workstations. The systems provide CAE interfaces to the following design environments: Cadence, Viewlogic®, Mentor Graphics®, and OrCAD™.

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc}, and the junction to ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a PQ160 package at commercial temperature and still air is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}\text{°C/W}} = \frac{150°C - 70°C}{33°C/W} = 2.4 \text{ W}$$

EQ 1

Table 2-4 • **Package Thermal Characteristics**

Package Type*	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft./min.	Units
Ceramic Pin Grid Array	100	5	35	17	°C/W
	132	5	30	15	°C/W
	176	8	23	12	°C/W
Ceramic Quad Flatpack	172	8	25	15	°C/W
Plastic Quad Flatpack[1]	100	13	48	40	°C/W
	144	15	40	32	°C/W
	160	15	38	30	°C/W
Plastic Leaded Chip Carrier	84	12	37	28	°C/W
Very Thin Quad Flatpack	100	12	43	35	°C/W
Thin Quad Flatpack	176	15	32	25	°C/W

Notes: (Maximum Power in Still Air)

1. *Maximum power dissipation values for PQFP packages are 1.9 W (PQ100), 2.3 W (PQ144), and 2.4 W (PQ160).*
2. *Maximum power dissipation for PLCC packages is 2.7 W.*
3. *Maximum power dissipation for VQFP packages is 2.3 W.*
4. *Maximum power dissipation for TQFP packages is 3.1 W.*

Power Dissipation

P = [ICC standby + ICCactive] * VCC + IOL * VOL * N + IOH* (VCC – VOH) * M

EQ 2

where:

ICC standby is the current flowing when no inputs or outputs are changing

ICCactive is the current flowing due to CMOS switching.

IOL and IOH are TTL sink/source currents.

VOL and VOH are TTL level output voltages.

N is the number of outputs driving TTL loads to VOL.

M is the number of outputs driving TTL loads to VOH.

An accurate determination of N and M is problematical because their values depend on the family type, design details, and on the system I/O. The power can be divided into two components: static and active.

ACT 2 Timing Model[1]
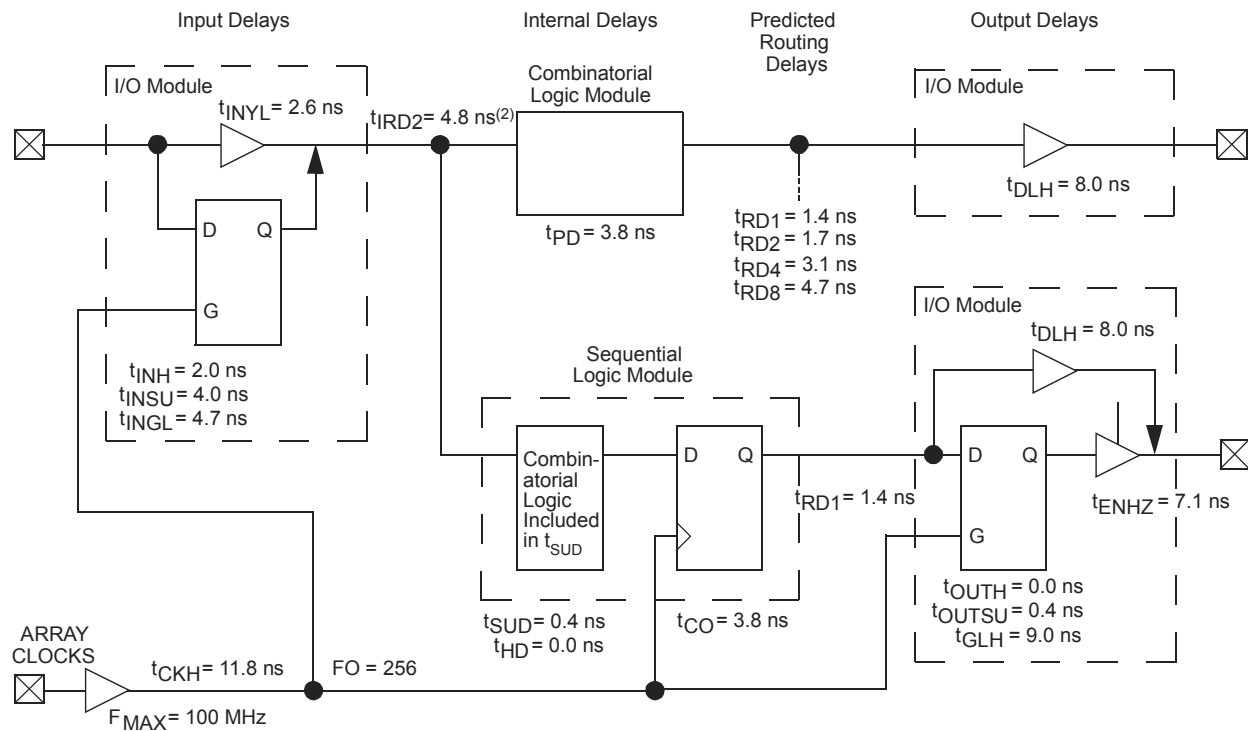
Notes:

1. *Values shown for A1240A-2 at worst-case commercial conditions.*
2. *Input module predicted routing delay*
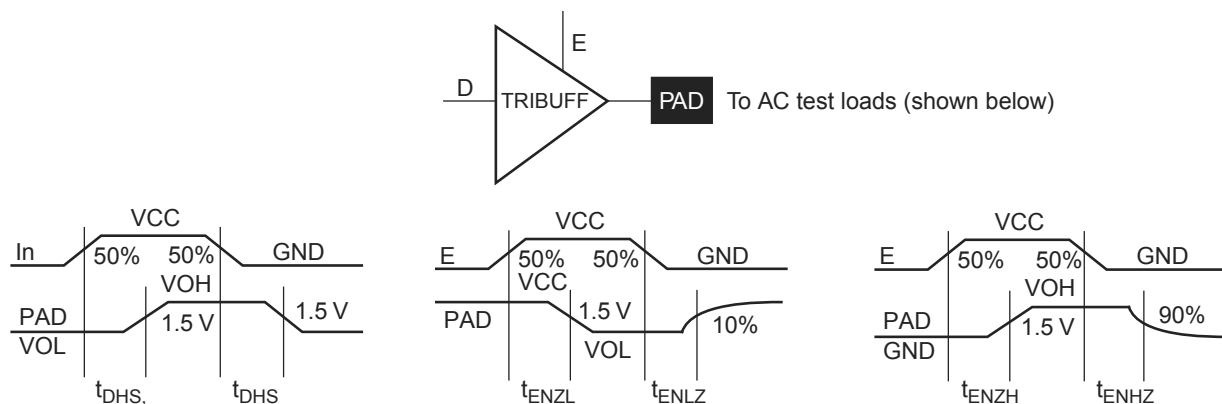
Figure 2-1 • **Timing Model**

Parameter Measurement

Figure 2-2 • **Output Buffer Delays**
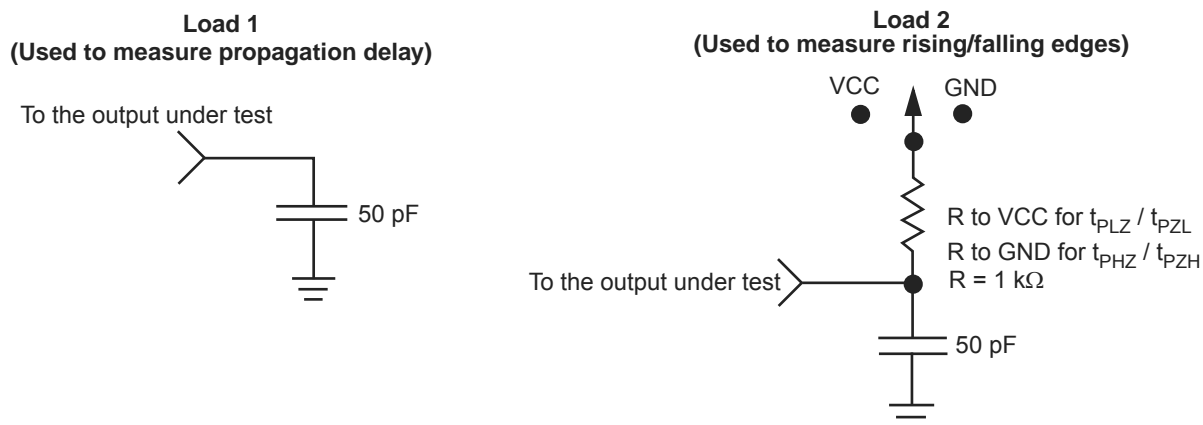

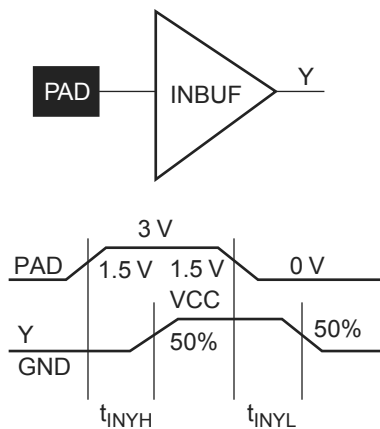*Figure 2-3 •* **AC Test Loads**

Figure 2-4 • **Input Buffer Delays**

Timing Derating Factor (Temperature and Voltage)

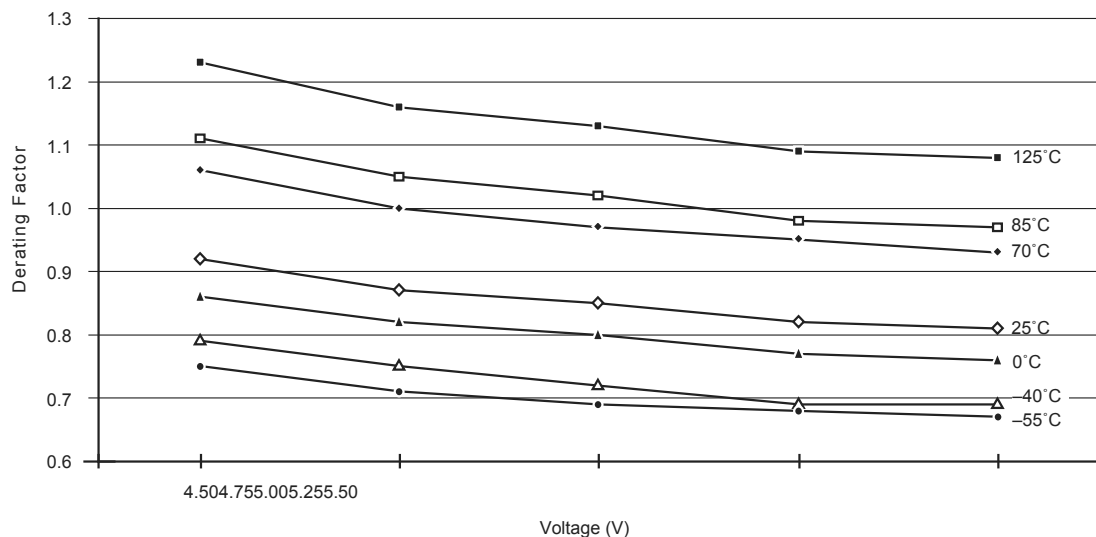*Table 2-9 •* **Timing Derating Factor (Temperature and Voltage)**

(Commercial Minimum/Maximum Specification) x	Industrial		Military	
	Min.	**Max.**	**Min.**	Max.
	0.69	1.11	0.67	1.23

Table 2-10 • **Timing Derating Factor for Designs at Typical Temperature (T$_J$ = 25°C) and Voltage (5.0 V)**

(Commercial Maximum Specification) x	0.85

Table 2-11 • **Temperature and Voltage Derating Factors (normalized to Worst-Case Commercial, TJ = 4.75 V, 70°C)**

	−55	**−40**	**0**	**25**	**70**	**85**	**125**
4.50	0.75	0.79	0.86	0.92	1.06	1.11	1.23
4.75	0.71	0.75	0.82	0.87	1.00	1.05	1.13
5.00	0.69	0.72	0.80	0.85	0.97	1.02	1.13
5.25	0.68	0.69	0.77	0.82	0.95	0.98	1.09
5.50	0.67	0.69	0.76	0.81	0.93	0.97	1.08

Note: *This derating factor applies to all routing and propagation delays.*

Figure 2-9 •   **Junction Temperature and Voltage Derating Curves (normalized to Worst-Case Commercial, T$_J$ = 4.75 V, 70°C)**

A1225A Timing Characteristics (continued)

Table 2-14 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C

TTL Output Module Timing[1]		–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t$_{DLH}$	Data to Pad High		8.0		9.0		10.6	ns
t$_{DHL}$	Data to Pad Low		10.1		11.4		13.4	ns
t$_{ENZH}$	Enable Pad Z to High		8.9		10.0		11.8	ns
t$_{ENZL}$	Enable Pad Z to Low		11.6		13.2		15.5	ns
t$_{ENHZ}$	Enable Pad High to Z		7.1		8.0		9.4	ns
t$_{ENLZ}$	Enable Pad Low to Z		8.3		9.5		11.1	ns
t$_{GLH}$	G to Pad High		8.9		10.2		11.9	ns
t$_{GHL}$	G to Pad Low		11.2		12.7		14.9	ns
d$_{TLH}$	Delta Low to High		0.07		0.08		0.09	ns/pF
d$_{THL}$	Delta High to Low		0.12		0.13		0.16	ns/pF
CMOS Output Module Timing[1]								
t$_{DLH}$	Data to Pad High		10.1		11.5		13.5	ns
t$_{DHL}$	Data to Pad Low		8.4		9.6		11.2	ns
t$_{ENZH}$	Enable Pad Z to High		8.9		10.0		11.8	ns
t$_{ENZL}$	Enable Pad Z to Low		11.6		13.2		15.5	ns
t$_{ENHZ}$	Enable Pad High to Z		7.1		8.0		9.4	ns
t$_{ENLZ}$	Enable Pad Low to Z		8.3		9.5		11.1	ns
t$_{GLH}$	G to Pad High		8.9		10.2		11.9	ns
t$_{GHL}$	G to Pad Low		11.2		12.7		14.9	ns
d$_{TLH}$	Delta Low to High		0.12		0.13		0.16	ns/pF
d$_{THL}$	Delta High to Low		0.09		0.10		0.12	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.*

A1240A Timing Characteristics (continued)

Table 2-17 • **A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

TTL Output Module Timing[1]		–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t$_{DLH}$	Data to Pad High		8.0		9.0		10.6	ns
t$_{DHL}$	Data to Pad Low		10.1		11.4		13.4	ns
t$_{ENZH}$	Enable Pad Z to High		8.9		10.0		11.8	ns
t$_{ENZL}$	Enable Pad Z to Low		11.7		13.2		15.5	ns
t$_{ENHZ}$	Enable Pad High to Z		7.1		8.0		9.4	ns
t$_{ENLZ}$	Enable Pad Low to Z		8.4		9.5		11.1	ns
t$_{GLH}$	G to Pad High		9.0		10.2		11.9	ns
t$_{GHL}$	G to Pad Low		11.2		12.7		14.9	ns
d$_{TLH}$	Delta Low to High		0.07		0.08		0.09	ns/pF
d$_{THL}$	Delta High to Low		0.12		0.13		0.16	ns/pF
CMOS Output Module Timing[1]								
t$_{DLH}$	Data to Pad High		10.2		11.5		13.5	ns
t$_{DHL}$	Data to Pad Low		8.4		9.6		11.2	ns
t$_{ENZH}$	Enable Pad Z to High		8.9		10.0		11.8	ns
t$_{ENZL}$	Enable Pad Z to Low		11.7		13.2		15.5	ns
t$_{ENHZ}$	Enable Pad High to Z		7.1		8.0		9.4	ns
t$_{ENLZ}$	Enable Pad Low to Z		8.4		9.5		11.1	ns
t$_{GLH}$	G to Pad High		9.0		10.2		11.9	ns
t$_{GHL}$	G to Pad Low		11.2		12.7		14.9	ns
d$_{TLH}$	Delta Low to High		0.12		0.13		0.16	ns/pF
d$_{THL}$	Delta High to Low		0.09		0.10		0.12	ns/pF

Notes:

1. Delays based on 50 pF loading.

2. SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.

A1280A Timing Characteristics

Table 2-18 • **A1280A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

Logic Module Propagation Delays[1]		–2 Speed[3]		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Single Module		3.8		4.3		5.0	ns
t_{CO}	Sequential Clock to Q		3.8		4.3		5.0	ns
t_{GO}	Latch G to Q		3.8		4.3		5.0	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		3.8		4.3		5.0	ns
Predicted Routing Delays[2]								
t_{RD1}	FO = 1 Routing Delay		1.7		2.0		2.3	ns
t_{RD2}	FO = 2 Routing Delay		2.5		2.8		3.3	ns
t_{RD3}	FO = 3 Routing Delay		3.0		3.4		4.0	ns
t_{RD4}	FO = 4 Routing Delay		3.7		4.2		4.9	ns
t_{RD8}	FO = 8 Routing Delay		6.7		7.5		8.8	ns
Sequential Timing Characteristics[3,4]								
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.5		6.0		7.0		ns
t_{WASYN}	Flip-Flop (Latch) Clock Asynchronous Pulse Width	5.5		6.0		7.0		ns
t_A	Flip-Flop Clock Input Period	11.7		13.3		18.0		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.4		0.4		0.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.4		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		85.0		75.0		50.0	MHz

Notes:

1. *For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}—whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*

4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A1280A Timing Characteristics (continued)

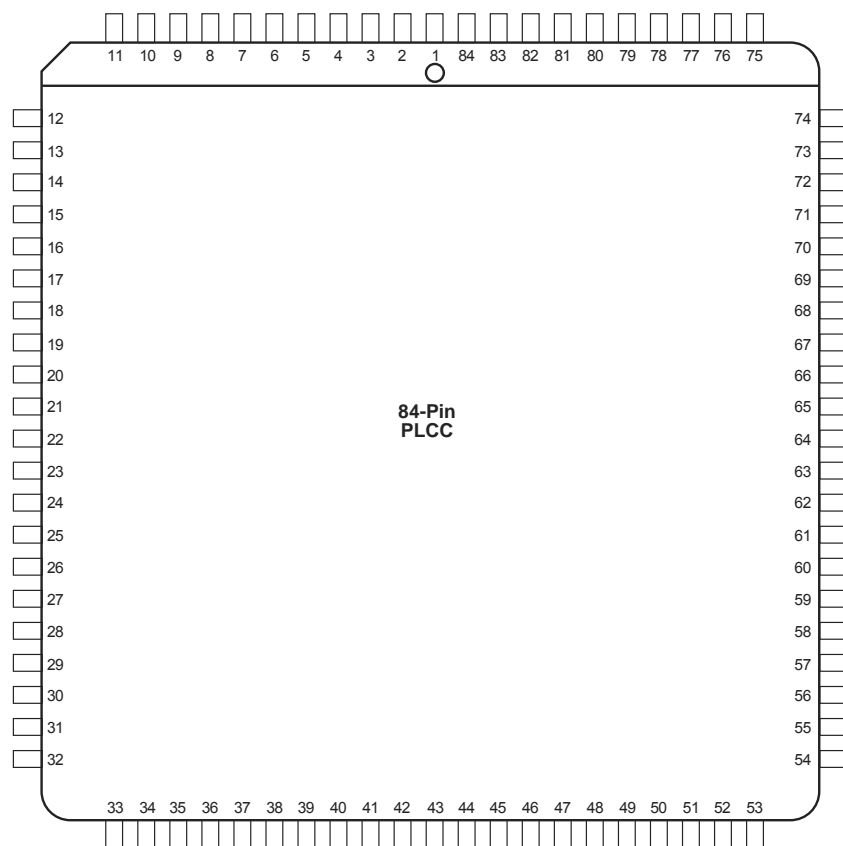*Table 2-19 •* **A1280A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

I/O Module Input Propagation Delays		–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t$_{INYH}$	Pad to Y High		2.9		3.3		3.8	ns
t$_{INYL}$	Pad to Y Low		2.7		3.0		3.5	ns
t$_{INGH}$	G to Y High		5.0		5.7		6.6	ns
t$_{INGL}$	G to Y Low		4.8		5.4		6.3	ns
Input Module Predicted Input Routing Delays[*]								
t$_{IRD1}$	FO = 1 Routing Delay		4.6		5.1		6.0	ns
t$_{IRD2}$	FO = 2 Routing Delay		5.2		5.9		6.9	ns
t$_{IRD3}$	FO = 3 Routing Delay		5.6		6.3		7.4	ns
t$_{IRD4}$	FO = 4 Routing Delay		6.5		7.3		8.6	ns
t$_{IRD8}$	FO = 8 Routing Delay		9.4		10.5		12.4	ns
Global Clock Network								
t$_{CKH}$	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		13.1		14.6		17.2	
t$_{CKL}$	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		13.3		14.9		17.5	
t$_{PWH}$	Minimum Pulse Width High	FO = 32	5.0		5.5		6.6		ns
		FO = 256	5.8		6.4		7.6		
t$_{PWL}$	Minimum Pulse Width Low	FO = 32	5.0		5.5		6.6		ns
		FO = 256	5.8		6.4		7.6		
t$_{CKSW}$	Maximum Skew	FO = 32		0.5		0.5		0.5	ns
		FO = 256		2.5		2.5		2.5	
t$_{SUEXT}$	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t$_{HEXT}$	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t$_P$	Minimum Period	FO = 32	9.6		11.2		13.3		ns
		FO = 256	10.6		12.6		15.3		
f$_{MAX}$	Maximum Frequency	FO = 32		105.0		90.0		75.0	ns
		FO = 256		95.0		80.0		65.0	

Note: **These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1280A Timing Characteristics (continued)

Microsemi

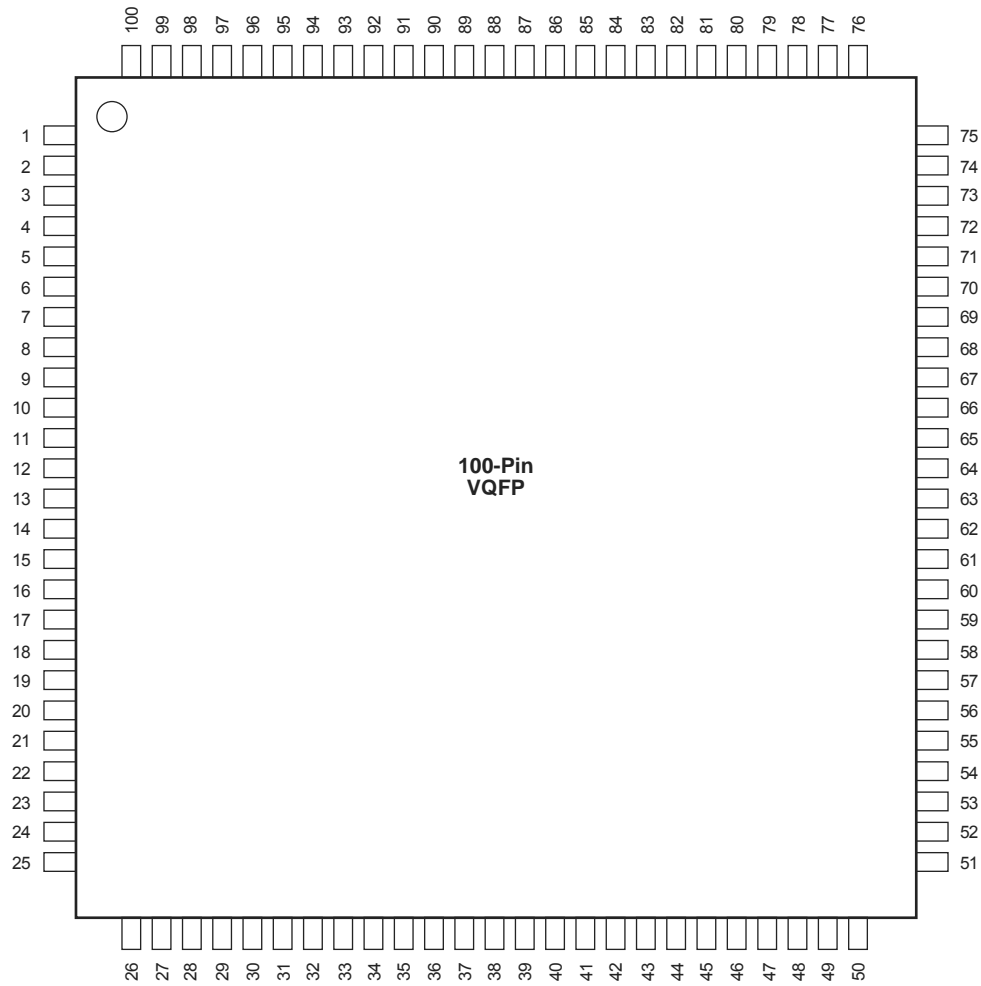# 3 – Package Pin Assignments

PL84

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

VQ100

**100-Pin
VQFP**

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

VQ100		VQ100	
Pin Number	**A1225A Function**	**Pin Number**	**A1225A Function**
2	MODE	64	VCC
7	GND	65	VCC
14	VCC	70	GND
15	VCC	77	SDI, I/O
20	GND	82	GND
32	GND	85	PRA, I/O
38	VCC	87	CLKA, I/O
44	GND	88	VCC
50	SDO	90	CLKB, I/O
55	GND	92	PRB, I/O
62	GND	94	GND
63	VCC	100	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
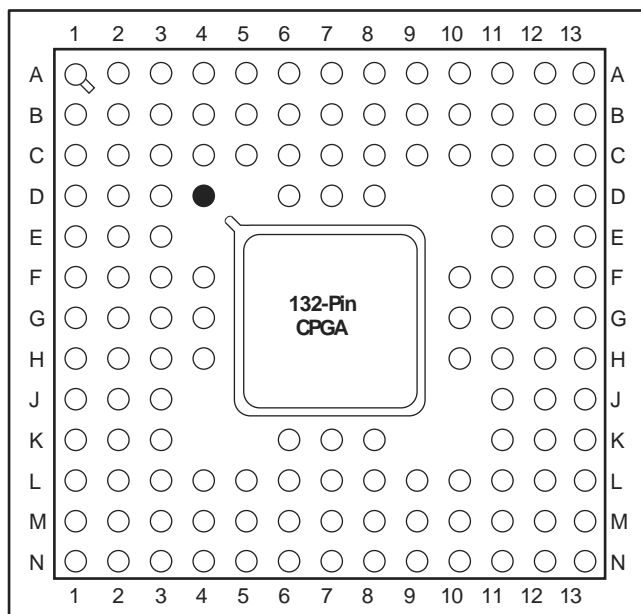
TQ176
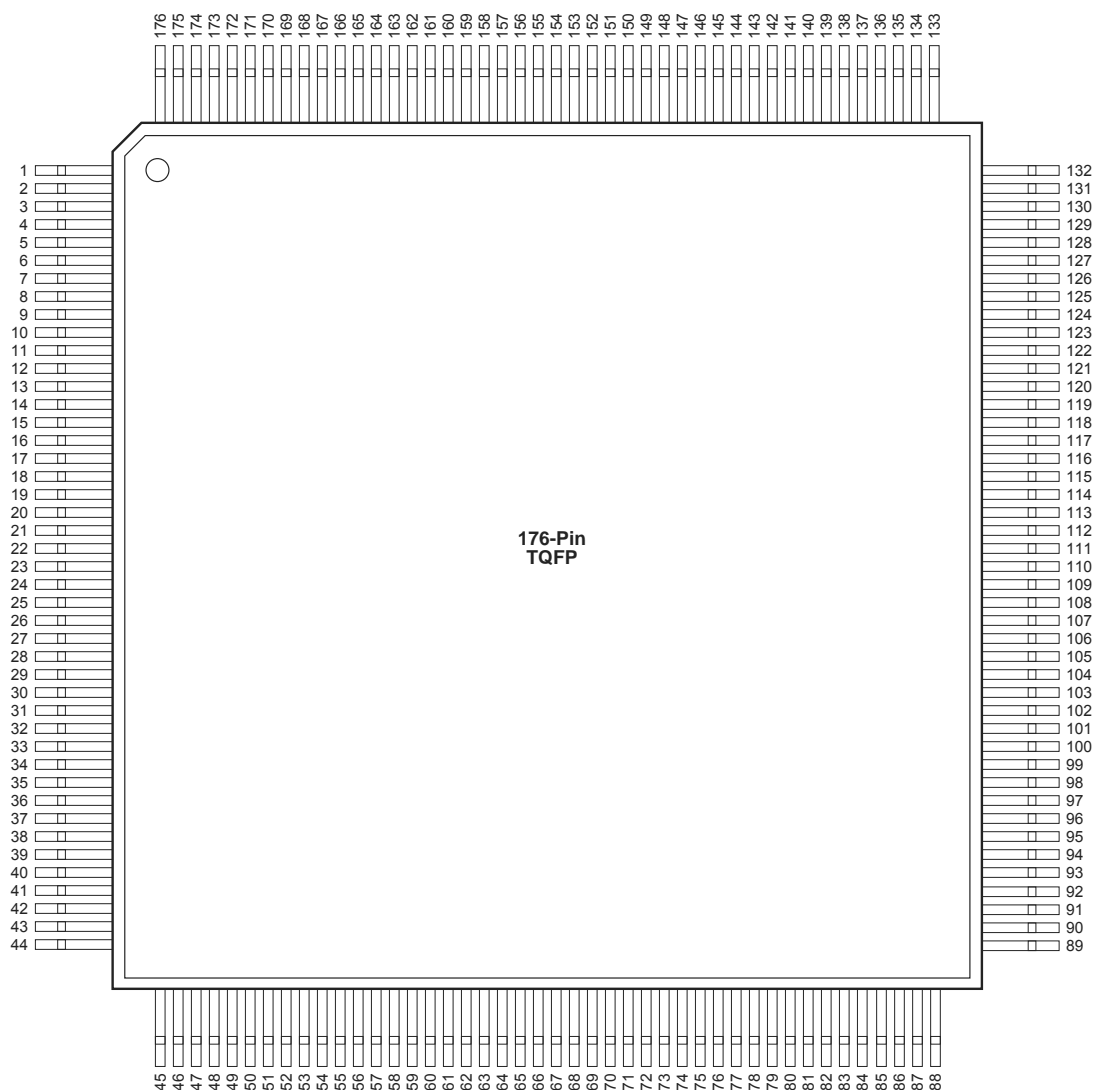
176-Pin
TQFP

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

TQ176			TQ176		
Pin Number	**A1240A Function**	**A1280A Function**	**Pin Number**	**A1240A Function**	**A1280A Function**
1	GND	GND	82	NC	VCC
2	MODE	MODE	86	NC	I/O
8	NC	NC	87	SDO	SDO
10	NC	I/O	89	GND	GND
11	NC	I/O	96	NC	I/O
13	NC	VCC	97	NC	I/O
18	GND	GND	101	NC	NC
19	NC	I/O	103	NC	I/O
20	NC	I/O	106	GND	GND
22	NC	I/O	107	NC	I/O
23	GND	GND	108	NC	I/O
24	NC	VCC	109	GND	GND
25	VCC	VCC	110	VCC	VCC
26	NC	I/O	111	GND	GND
27	NC	I/O	112	VCC	VCC
28	VCC	VCC	113	VCC	VCC
29	NC	I/O	114	NC	I/O
33	NC	NC	115	NC	I/O
37	NC	I/O	116	NC	VCC
38	NC	NC	121	NC	NC
45	GND	GND	124	NC	I/O
52	NC	VCC	125	NC	I/O
54	NC	I/O	126	NC	NC
55	NC	I/O	133	GND	GND
57	NC	NC	135	SDI, I/O	SDI, I/O
61	NC	I/O	136	NC	I/O
64	NC	I/O	140	NC	VCC
66	NC	I/O	143	NC	I/O
67	GND	GND	144	NC	I/O
68	VCC	VCC	145	NC	NC
74	NC	I/O	147	NC	I/O
77	NC	NC	151	NC	I/O
78	NC	I/O	152	PRA, I/O	PRA, I/O
80	NC	I/O	154	CLKA, I/O	CLKA, I/O

PG132

● Orientation Pin

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

PG176

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx
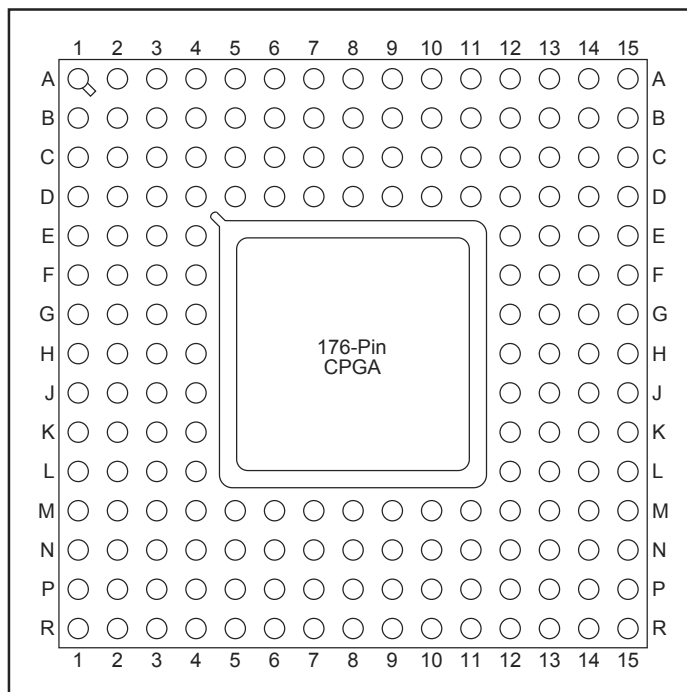
PG176	
Pin Number	**A1280A Function**
A9	CLKA, I/O
B3	DCLK, I/O
B8	CLKB, I/O
B14	SDI, I/O
C3	MODE
C8	GND
C9	PRA, I/O
D4	GND
D5	VCC
D6	GND
D7	PRB, I/O
D8	VCC
D10	GND
D11	VCC
D12	GND
E4	GND
E12	GND
F4	VCC
F12	GND
G4	GND
G12	VCC
H2	VCC

PG176	
Pin Number	**A1280A Function**
H3	VCC
H4	GND
H12	GND
H13	VCC
H14	VCC
J4	VCC
J12	GND
J13	GND
J14	VCC
K4	GND
K12	GND
L4	GND
M4	GND
M5	VCC
M6	GND
M8	GND
M10	GND
M11	VCC
M12	GND
N8	VCC
P13	SDO

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.