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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1232
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	125
Number of Gates	8000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1280a-pqg160c

Ordering Information

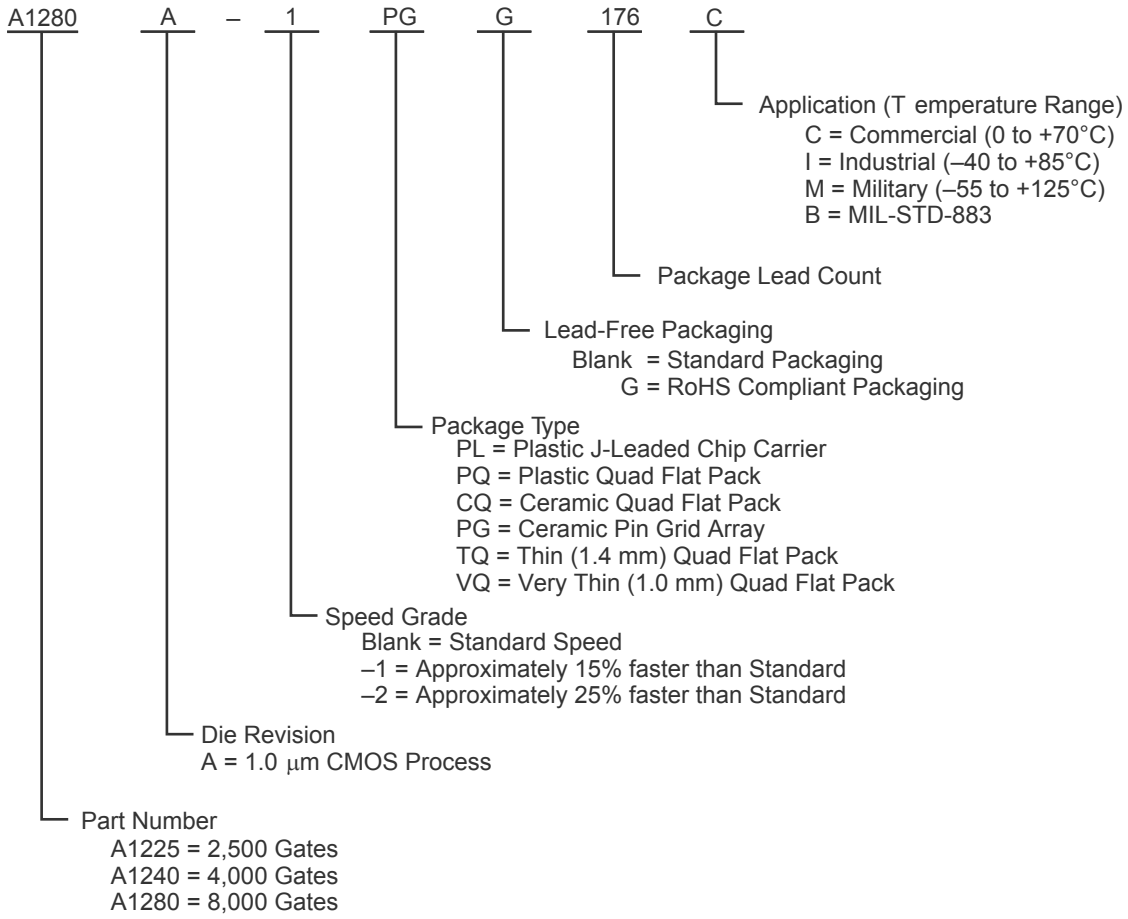


Table 2-3 • **Electrical Specifications**

Symbol	Parameter	Commercial		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
VOH[1]	(IOH = –10 mA)[2]	2.4	–	–	–	–	–	V
	(IOH = –6 mA)	3.84	–	–	–	–	–	V
	(IOH = –4 mA)	–	–	3.7	–	3.7	–	V
VOL[1]	(IOL = 10 mA)[2]	–	0.5	–	–	–	–	V
	(IOL = 6 mA)	–	0.33	–	0.40	–	0.40	V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
Input Transition Time t_R, t_F[2]		–	500	–	500	–	500	ns
C_{IO} I/O capacitance[2,3]		–	10	–	10	–	10	pF
Standby Current, ICC[4] (typical = 1 mA)		–	2	–	10	–	20	mA
Leakage Current[5]		–10	+10	–10	+10	–10	+10	µA
ICC(D)	Dynamic VCC supply current. See the Power Dissipation section.							

Notes:

1. *Only one output tested at a time. VCC = minimum.*
2. *Not tested, for information only.*
3. *Includes worst-case PG176 package capacitance. VOUT = 0 V, f = 1 MHz*
4. *All outputs unloaded. All inputs = VCC or GND, typical ICC = 1 mA. ICC limit includes IPP and ISV during normal operations.*
5. *VOUT, VIN = VCC or GND.*

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. EQ 4 shows a piece-wise linear summation over all components.

$$\text{Power} = VCC^2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs}$$
$$+ (p * (C_{EQO} + C_L) * fp)_{outputs}$$
$$+ 0.5 * (q1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r1 * f_{q1})_{routed\_Clk1}$$
$$+ 0.5 * (q2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2}$$

EQ 4

Where:

m = Number of logic modules switching at f_m

n = Number of input buffers switching at f_n

p = Number of output buffers switching at f_p

q1 = Number of clock loads on the first routed array clock

q2 = Number of clock loads on the second routed array clock

r_1 = Fixed capacitance due to first routed array clock

r_2 = Fixed capacitance due to second routed array clock

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_L = Output lead capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

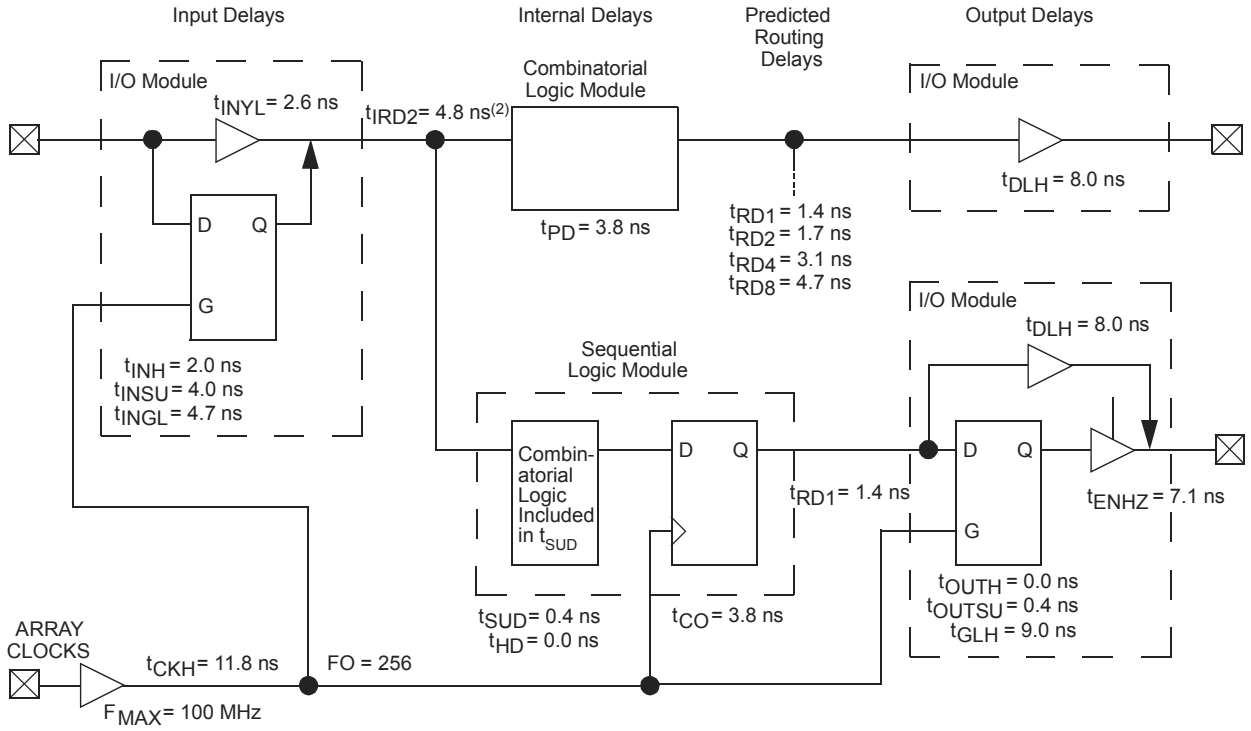
f_{q1} = Average first routed array clock rate in MHz

f_{q2} = Average second routed array clock rate in MHz

Table 2-7 • **Fixed Capacitance Values for Microsemi FPGAs**

Device Type	r1, routed_Clk1	r2, routed_Clk2
A1225A	106	106.0
A1240A	134	134.2
A1280A	168	167.8

ACT 2 Timing Model[1]



Notes:

1. *Values shown for A1240A-2 at worst-case commercial conditions.*
2. *Input module predicted routing delay*

Figure 2-1 • **Timing Model**

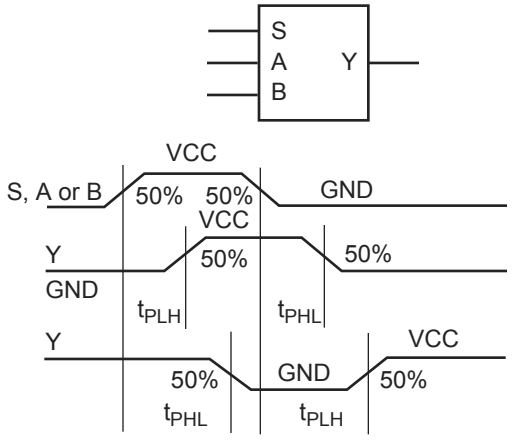
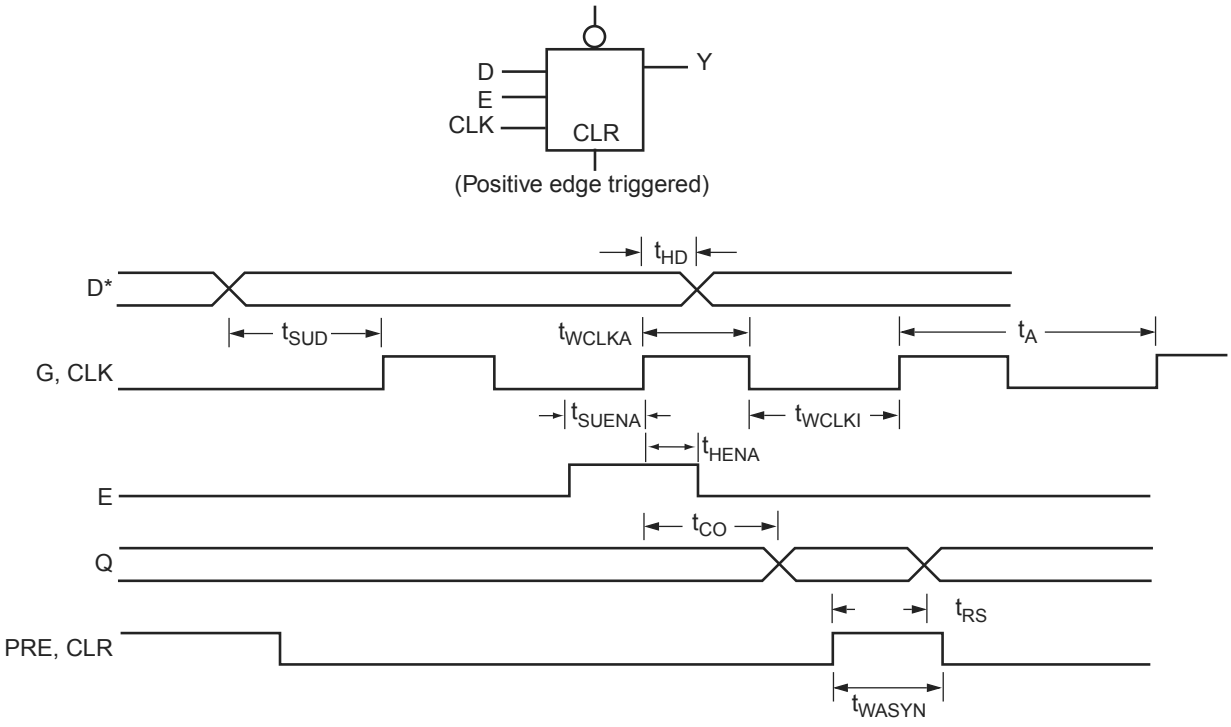


Figure 2-5 • **Module Delays**

Sequential Module Timing Characteristics



Note: D represents all data functions involving A, B, and S for multiplexed flip-flops.

Figure 2-6 • **Flip-Flops and Latches**

A1225A Timing Characteristics

***Table 2-12* • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

Logic Module Propagation Delays[1]		**–2 Speed[3]**		**–1 Speed**		**Std. Speed**		**Units**
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{PD1}	Single Module		3.8		4.3		5.0	ns
t_{CO}	Sequential Clock to Q		3.8		4.3		5.0	ns
t_{GO}	Latch G to Q		3.8		4.3		5.0	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		3.8		4.3		5.0	ns
Predicted Routing Delays[2]								
t_{RD1}	FO = 1 Routing Delay		1.1		1.2		1.4	ns
t_{RD2}	FO = 2 Routing Delay		1.7		1.9		2.2	ns
t_{RD3}	FO = 3 Routing Delay		2.3		2.6		3.0	ns
t_{RD4}	FO = 4 Routing Delay		2.8		3.1		3.7	ns
t_{RD8}	FO = 8 Routing Delay		4.4		4.9		5.8	ns
Sequential Timing Characteristics[3,4]								
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.5		5.0		6.0		ns
t_{WASYN}	Flip-Flop (Latch) Clock Asynchronous Pulse Width	4.5		5.0		6.0		ns
t_A	Flip-Flop Clock Input Period	9.4		11.0		13.0		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.4		0.4		0.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.4		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		105.0		90.0		75.0	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$—whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A1280A Timing Characteristics

***Table 2-18* • A1280A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

Logic Module Propagation Delays[1]		**–2 Speed[3]**		**–1 Speed**		**Std. Speed**		**Units**
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{PD1}	Single Module		3.8		4.3		5.0	ns
t_{CO}	Sequential Clock to Q		3.8		4.3		5.0	ns
t_{GO}	Latch G to Q		3.8		4.3		5.0	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		3.8		4.3		5.0	ns
Predicted Routing Delays[2]								
t_{RD1}	FO = 1 Routing Delay		1.7		2.0		2.3	ns
t_{RD2}	FO = 2 Routing Delay		2.5		2.8		3.3	ns
t_{RD3}	FO = 3 Routing Delay		3.0		3.4		4.0	ns
t_{RD4}	FO = 4 Routing Delay		3.7		4.2		4.9	ns
t_{RD8}	FO = 8 Routing Delay		6.7		7.5		8.8	ns
Sequential Timing Characteristics[3,4]								
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.5		6.0		7.0		ns
t_{WASYN}	Flip-Flop (Latch) Clock Asynchronous Pulse Width	5.5		6.0		7.0		ns
t_A	Flip-Flop Clock Input Period	11.7		13.3		18.0		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.4		0.4		0.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.4		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		85.0		75.0		50.0	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$—whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

***Table 2-20* • A1280A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

TTL Output Module Timing[1]		**–2 Speed**		**–1 Speed**		**Std. Speed**		**Units**
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{DLH}	Data to Pad High		8.1		9.0		10.6	ns
t_{DHL}	Data to Pad Low		10.2		11.4		13.4	ns
t_{ENZH}	Enable Pad Z to High		9.0		10.0		11.8	ns
t_{ENZL}	Enable Pad Z to Low		11.8		13.2		15.5	ns
t_{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t_{ENLZ}	Enable Pad Low to Z		8.4		9.5		11.1	ns
t_{GLH}	G to Pad High		9.0		10.2		11.9	ns
t_{GHL}	G to Pad Low		11.3		12.7		14.9	ns
d_{TLH}	Delta Low to High		0.07		0.08		0.09	ns/pF
d_{THL}	Delta High to Low		0.12		0.13		0.16	ns/pF
CMOS Output Module Timing[1]								
t_{DLH}	Data to Pad High		10.3		11.5		13.5	ns
t_{DHL}	Data to Pad Low		8.5		9.6		11.2	ns
t_{ENZH}	Enable Pad Z to High		9.0		10.0		11.8	ns
t_{ENZL}	Enable Pad Z to Low		11.8		13.2		15.5	ns
t_{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t_{ENLZ}	Enable Pad Low to Z		8.4		9.5		11.1	ns
t_{GLH}	G to Pad High		9.0		10.2		11.9	ns
t_{GHL}	G to Pad Low		11.3		12.7		14.9	ns
d_{TLH}	Delta Low to High		0.12		0.13		0.16	ns/pF
d_{THL}	Delta High to Low		0.09		0.10		0.12	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.*

PQ100	
Pin Number	**A1225A Function**
2	DCLK, I/O
4	MODE
9	GND
16	VCC
17	VCC
22	GND
34	GND
40	VCC
46	GND
52	SDO
57	GND
64	GND

PQ100	
Pin Number	**A1225A Function**
65	VCC
66	VCC
67	VCC
72	GND
79	SDI, I/O
84	GND
87	PRA, I/O
89	CLKA, I/O
90	VCC
92	CLKB, I/O
94	PRB, I/O
96	GND

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

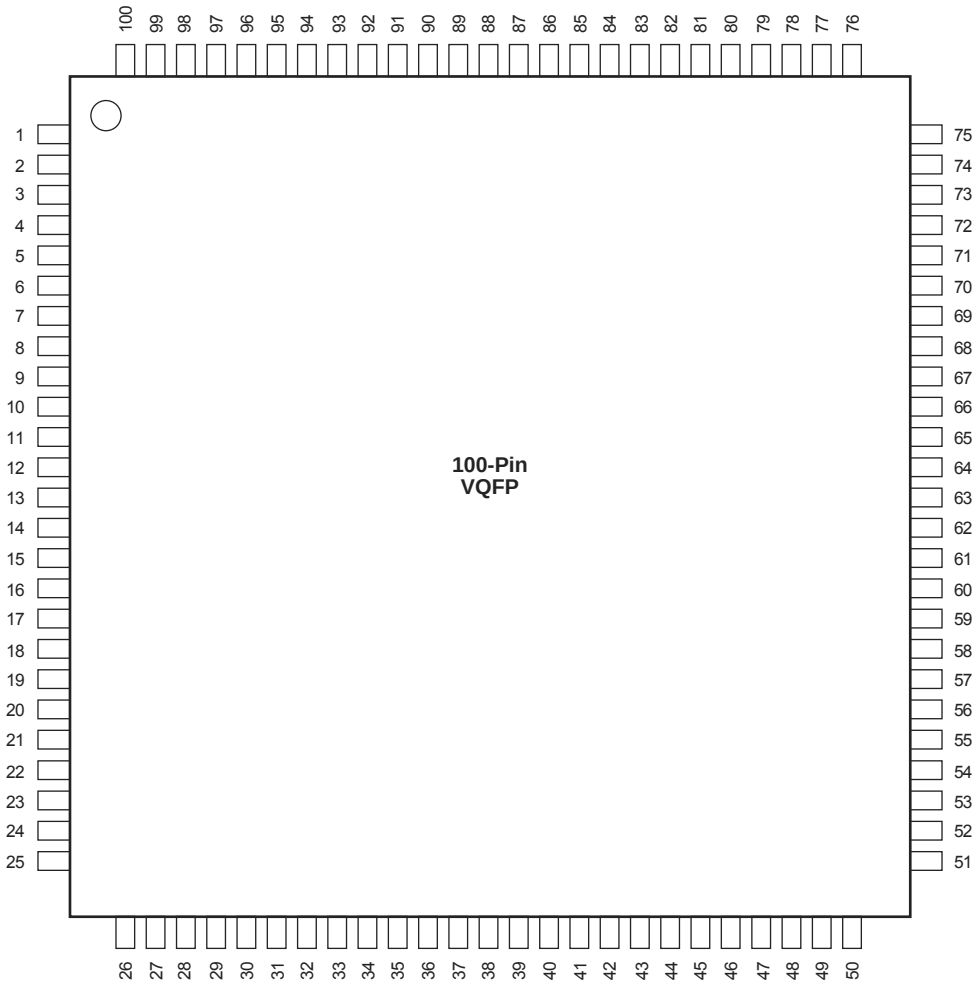
PQ144	
Pin Number	**A1240A Function**
2	MODE
9	GND
10	GND
11	GND
18	VCC
19	VCC
20	VCC
21	VCC
28	GND
29	GND
30	GND
44	GND
45	GND
46	GND
54	VCC
55	VCC
56	VCC
64	GND
65	GND
71	SDO
79	GND
80	GND
81	GND
88	GND

PQ144	
Pin Number	**A1240A Function**
89	VCC
90	VCC
91	VCC
92	VCC
93	VCC
100	GND
101	GND
102	GND
110	SDI, I/O
116	GND
117	GND
118	GND
123	PRA, I/O
125	CLKA, I/O
126	VCC
127	VCC
128	VCC
130	CLKB, I/O
132	PRB, I/O
136	GND
137	GND
138	GND
144	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

VQ100



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

VQ100	
Pin Number	**A1225A Function**
2	MODE
7	GND
14	VCC
15	VCC
20	GND
32	GND
38	VCC
44	GND
50	SDO
55	GND
62	GND
63	VCC

VQ100	
Pin Number	**A1225A Function**
64	VCC
65	VCC
70	GND
77	SDI, I/O
82	GND
85	PRA, I/O
87	CLKA, I/O
88	VCC
90	CLKB, I/O
92	PRB, I/O
94	GND
100	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

TQ176		
Pin Number	**A1240A Function**	**A1280A Function**
1	GND	GND
2	MODE	MODE
8	NC	NC
10	NC	I/O
11	NC	I/O
13	NC	VCC
18	GND	GND
19	NC	I/O
20	NC	I/O
22	NC	I/O
23	GND	GND
24	NC	VCC
25	VCC	VCC
26	NC	I/O
27	NC	I/O
28	VCC	VCC
29	NC	I/O
33	NC	NC
37	NC	I/O
38	NC	NC
45	GND	GND
52	NC	VCC
54	NC	I/O
55	NC	I/O
57	NC	NC
61	NC	I/O
64	NC	I/O
66	NC	I/O
67	GND	GND
68	VCC	VCC
74	NC	I/O
77	NC	NC
78	NC	I/O
80	NC	I/O

TQ176		
Pin Number	**A1240A Function**	**A1280A Function**
82	NC	VCC
86	NC	I/O
87	SDO	SDO
89	GND	GND
96	NC	I/O
97	NC	I/O
101	NC	NC
103	NC	I/O
106	GND	GND
107	NC	I/O
108	NC	I/O
109	GND	GND
110	VCC	VCC
111	GND	GND
112	VCC	VCC
113	VCC	VCC
114	NC	I/O
115	NC	I/O
116	NC	VCC
121	NC	NC
124	NC	I/O
125	NC	I/O
126	NC	NC
133	GND	GND
135	SDI, I/O	SDI, I/O
136	NC	I/O
140	NC	VCC
143	NC	I/O
144	NC	I/O
145	NC	NC
147	NC	I/O
151	NC	I/O
152	PRA, I/O	PRA, I/O
154	CLKA, I/O	CLKA, I/O

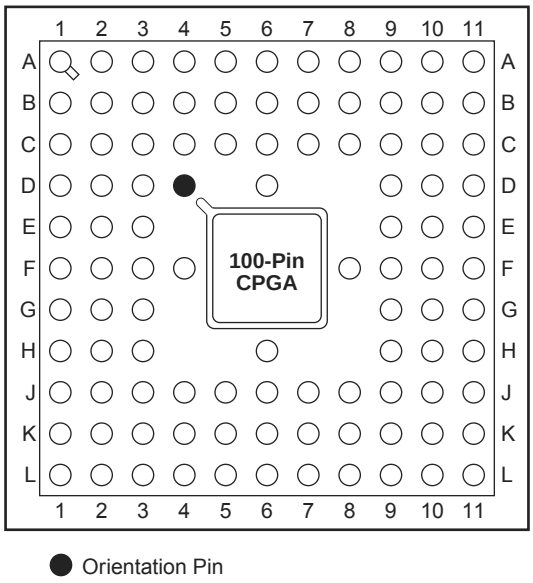
CQ172	
Pin Number	**A1280A Function**
1	MODE
7	GND
12	VCC
17	GND
22	GND
23	VCC
24	VCC
27	VCC
32	GND
37	GND
50	VCC
55	GND
65	GND
66	VCC
75	GND
80	VCC
85	SDO
98	GND
103	GND
106	GND

CQ172	
Pin Number	**A1280A Function**
107	VCC
108	GND
109	VCC
110	VCC
113	VCC
118	GND
123	GND
131	SDI, I/O
136	VCC
141	GND
148	PRA, I/O
150	CLKA, I/O
151	VCC
152	GND
154	CLKB, I/O
156	PRB, I/O
161	GND
166	VCC
171	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG100



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

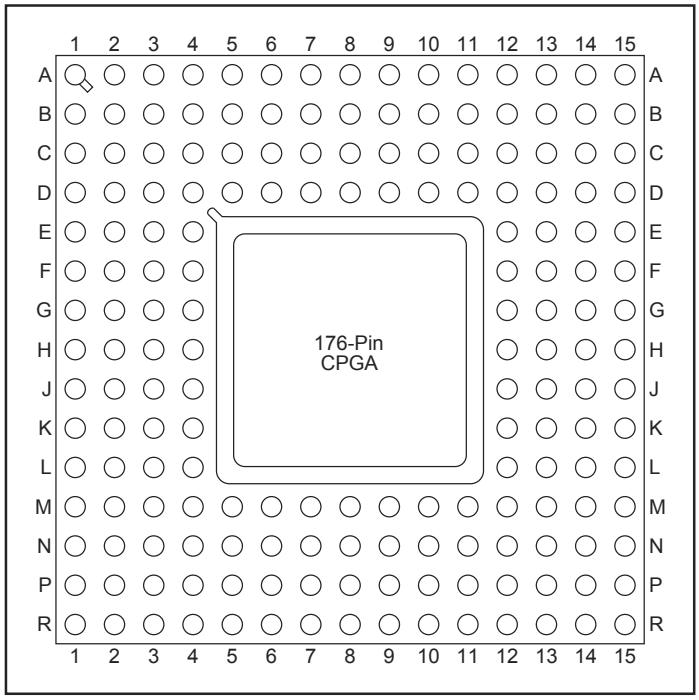
PG132	
Pin Number	**A1240A Function**
A1	MODE
B5	GND
B6	CLKB, I/O
B7	CLKA, I/O
B8	PRA, I/O
B9	GND
B12	SDI, I/O
C3	DCLK, I/O
C5	GND
C6	PRB, I/O
C7	VCC
C9	GND
D7	VCC
E3	GND
E11	GND
E12	GND
F4	GND
G2	VCC

PG132	
Pin Number	**A1240A Function**
G3	VCC
G4	VCC
G10	VCC
G11	VCC
G12	VCC
G13	VCC
H13	GND
J2	GND
J3	GND
J11	GND
K7	VCC
K12	GND
L5	GND
L7	VCC
L9	GND
M9	GND
N12	SDO

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG176



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

Safety Critical, Life Support, and High-Reliability Applications Policy

The products described in this advance status document may not have completed the Microsemi qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the Microsemi SoC Products Group Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the SoC Products Group’s products is available at http://www.microsemi.com/soc/documents/ORT_Report.pdf. Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local sales office for additional reliability information.