



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |   |
|--------------------------------|---|
| Product Status                 | Obsolete  |
| Number of LABs/CLBs            | 1232  |
| Number of Logic Elements/Cells | -   |
| Total RAM Bits                 | -   |
| Number of I/O                  | 125   |
| Number of Gates                | 8000  |
| Voltage - Supply               | 4.5V ~ 5.5V   |
| Mounting Type                  | Surface Mount   |
| Operating Temperature          | -40°C ~ 85°C (TA)   |
| Package / Case                 | 160-BQFP  |
| Supplier Device Package        | 160-PQFP (28x28)  |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/microsemi/a1280a-pqg160i">https://www.e-xfl.com/product-detail/microsemi/a1280a-pqg160i</a> |

# 1 – ACT 2 Family Overview

---

## General Description

The ACT 2 family represents Actel's second generation of field programmable gate arrays (FPGAs). The ACT 2 family presents a two-module architecture, consisting of C-modules and S-modules. These modules are optimized for both combinatorial and sequential designs. Based on Actel's patented channeled array architecture, the ACT 2 family provides significant enhancements to gate density and performance while maintaining downward compatibility with the ACT 1 design environment and upward compatibility with the ACT 3 design environment. The devices are implemented in silicon gate, 1.0- $\mu\text{m}$ , two-level metal CMOS, and employ Actel's PLICE® antifuse technology. This revolutionary architecture offers gate array design flexibility, high performance, and fast time-to-production with user programming. The ACT 2 family is supported by the Designer and Designer Advantage Systems, which offers automatic pin assignment, validation of electrical and design rules, automatic placement and routing, timing analysis, user programming, and diagnostic probe capabilities. The systems are supported on the following platforms: 386/486™ PC, Sun™, and HP™ workstations. The systems provide CAE interfaces to the following design environments: Cadence, Viewlogic®, Mentor Graphics®, and OrCAD™.

## 2 – Detailed Specifications

### Operating Conditions

**Table 2-1 • Absolute Maximum Ratings<sup>1</sup>**

| Symbol           | Parameter                            | Limits            | Units |
|------------------|--------------------------------------|-------------------|-------|
| VCC              | DC supply voltage                    | –0.5 to +7.0      | V     |
| VI               | Input voltage                        | –0.5 to VCC + 0.5 | V     |
| VO               | Output voltage                       | –0.5 to VCC + 0.5 | V     |
| IIO              | I/O source sink current <sup>2</sup> | ±20               | mA    |
| T <sub>STG</sub> | Storage temperature                  | –65 to +150       | °C    |

Notes:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.
2. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND –0.5 V, the internal protection diodes will be forward biased and can draw excessive current.

**Table 2-2 • Recommended Operating Conditions**

| Parameter              | Commercial | Industrial | Military    | Units |
|------------------------|------------|------------|-------------|-------|
| Temperature range*     | 0 to +70   | –40 to +85 | –55 to +125 | °C    |
| Power supply tolerance | ±5         | ±10        | ±10         | %VCC  |

Note: \*Ambient temperature ( $T_A$ ) is used for commercial and industrial; case temperature ( $T_C$ ) is used for military.

## Static Power Component

Microsemi FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated in Table 2-5 for commercial, worst case conditions.

**Table 2-5 • Standby Power Calculation**

| ICC  | VCC    | Power   |
|------|--------|---------|
| 2 mA | 5.25 V | 10.5 mW |

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

## Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs.

An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

## Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by EQ 3.

$$\text{Power } (\mu\text{W}) = C_{\text{EQ}} * V_{\text{CC}}^2 * F$$

EQ 3

Where:

$C_{\text{EQ}}$  is the equivalent capacitance expressed in pF.

VCC is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring ICC active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown in Table 2-6.

**Table 2-6 • CEQ Values for Microsemi FPGAs**

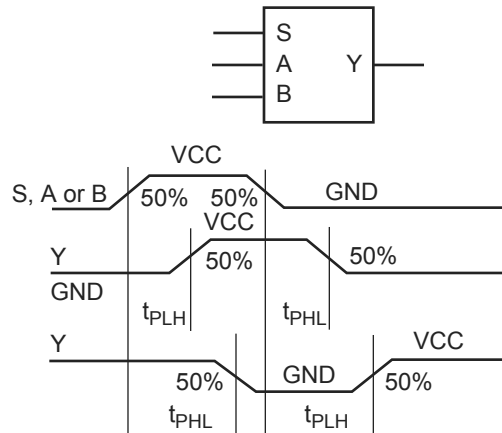
| Item  | CEQ Value |
|---|-----------|
| Modules ( $C_{\text{EQM}}$ )                          | 5.8       |
| Input Buffers ( $C_{\text{EQI}}$ )                    | 12.9      |
| Output Buffers ( $C_{\text{EQO}}$ )                   | 23.8      |
| Routed Array Clock Buffer Loads ( $C_{\text{EQCR}}$ ) | 3.9       |

## Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are given in Table 2-8.

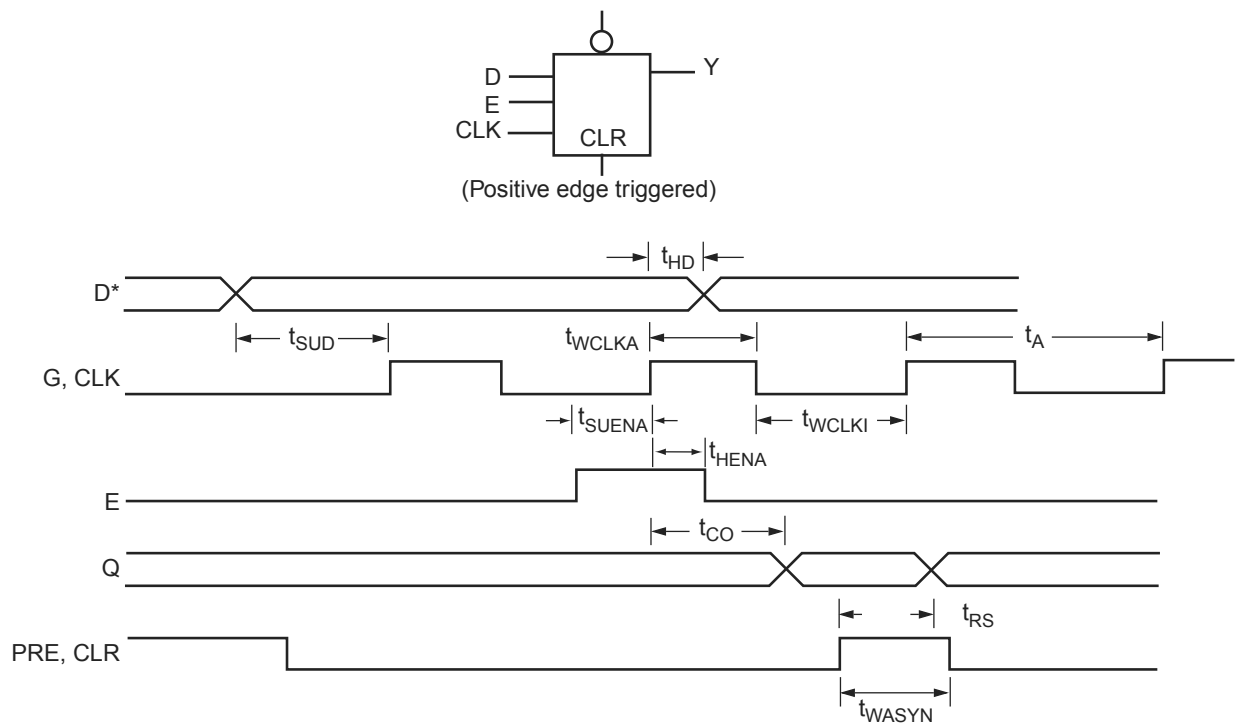
**Table 2-8 • Guidelines for Predicting Power Dissipation**

| Data  | Value                     |
|---|---------------------------|
| Logic Modules (m)                                   | 80% of modules            |
| Inputs switching (n)                                | # inputs/4                |
| Outputs switching (p)                               | # output/4                |
| First routed array clock loads (q1)                 | 40% of sequential modules |
| Second routed array clock loads (q2)                | 40% of sequential modules |
| Load capacitance ( $C_L$ )                          | 35 pF                     |
| Average logic module switching rate ( $f_m$ )       | F/10                      |
| Average input switching rate ( $f_n$ )              | F/5                       |
| Average output switching rate ( $f_p$ )             | F/10                      |
| Average first routed array clock rate ( $f_{q1}$ )  | F                         |
| Average second routed array clock rate ( $f_{q2}$ ) | F/2                       |



**Figure 2-5 • Module Delays**

## Sequential Module Timing Characteristics



*Note: D represents all data functions involving A, B, and S for multiplexed flip-flops.*

**Figure 2-6 • Flip-Flops and Latches**

## A1225A Timing Characteristics

**Table 2-12 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C**

| Logic Module Propagation Delays <sup>1</sup>           |  | –2 Speed <sup>3</sup> |       | –1 Speed |      | Std. Speed |      | Units |
|--|--|-----------------------|-------|----------|------|------------|------|-------|
| Parameter/Description                                  |  | Min.                  | Max.  | Min.     | Max. | Min.       | Max. |       |
| t <sub>PD1</sub>                                       | Single Module                                    |                       | 3.8   |          | 4.3  |            | 5.0  | ns    |
| t <sub>CO</sub>  | Sequential Clock to Q                            |                       | 3.8   |          | 4.3  |            | 5.0  | ns    |
| t <sub>GO</sub>  | Latch G to Q                                     |                       | 3.8   |          | 4.3  |            | 5.0  | ns    |
| t <sub>RS</sub>  | Flip-Flop (Latch) Reset to Q                     |                       | 3.8   |          | 4.3  |            | 5.0  | ns    |
| <b>Predicted Routing Delays<sup>2</sup></b>            |  |                       |       |          |      |            |      |       |
| t <sub>RD1</sub>                                       | FO = 1 Routing Delay                             |                       | 1.1   |          | 1.2  |            | 1.4  | ns    |
| t <sub>RD2</sub>                                       | FO = 2 Routing Delay                             |                       | 1.7   |          | 1.9  |            | 2.2  | ns    |
| t <sub>RD3</sub>                                       | FO = 3 Routing Delay                             |                       | 2.3   |          | 2.6  |            | 3.0  | ns    |
| t <sub>RD4</sub>                                       | FO = 4 Routing Delay                             |                       | 2.8   |          | 3.1  |            | 3.7  | ns    |
| t <sub>RD8</sub>                                       | FO = 8 Routing Delay                             |                       | 4.4   |          | 4.9  |            | 5.8  | ns    |
| <b>Sequential Timing Characteristics<sup>3,4</sup></b> |  |                       |       |          |      |            |      |       |
| t <sub>SUD</sub>                                       | Flip-Flop (Latch) Data Input Setup               | 0.4                   |       | 0.4      |      | 0.5        |      | ns    |
| t <sub>HD</sub>  | Flip-Flop (Latch) Data Input Hold                | 0.0                   |       | 0.0      |      | 0.0        |      | ns    |
| t <sub>SUENA</sub>                                     | Flip-Flop (Latch) Enable Setup                   | 0.8                   |       | 0.9      |      | 1.0        |      | ns    |
| t <sub>HENA</sub>                                      | Flip-Flop (Latch) Enable Hold                    | 0.0                   |       | 0.0      |      | 0.0        |      | ns    |
| t <sub>WCLKA</sub>                                     | Flip-Flop (Latch) Clock Active Pulse Width       | 4.5                   |       | 5.0      |      | 6.0        |      | ns    |
| t <sub>WASYN</sub>                                     | Flip-Flop (Latch) Clock Asynchronous Pulse Width | 4.5                   |       | 5.0      |      | 6.0        |      | ns    |
| t <sub>A</sub>   | Flip-Flop Clock Input Period                     | 9.4                   |       | 11.0     |      | 13.0       |      | ns    |
| t <sub>INH</sub>                                       | Input Buffer Latch Hold                          | 0.0                   |       | 0.0      |      | 0.0        |      | ns    |
| t <sub>INSU</sub>                                      | Input Buffer Latch Setup                         | 0.4                   |       | 0.4      |      | 0.5        |      | ns    |
| t <sub>OUTH</sub>                                      | Output Buffer Latch Hold                         | 0.0                   |       | 0.0      |      | 0.0        |      | ns    |
| t <sub>OUTSU</sub>                                     | Output Buffer Latch Setup                        | 0.4                   |       | 0.4      |      | 0.5        |      | ns    |
| f <sub>MAX</sub>                                       | Flip-Flop (Latch) Clock Frequency                |                       | 105.0 |          | 90.0 |            | 75.0 | MHz   |

**Notes:**

1. For dual-module macros, use t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, t<sub>CO</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, or t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>SUD</sub>—whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
4. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

## Pin Descriptions

**CLKA                      Clock A (Input)**

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

**CLKB                      Clock B (Input)**

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

**DCLK                      Diagnostic Clock (Input)**

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

**GND                      Ground**

Low supply voltage.

**I/O                      Input/Output (Input, Output)**

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven Low by the ALS software.

**MODE                      Mode (Input)**

The MODE pin controls the use of multifunction pins (DCLK, PRA, PRB, SDI). When the MODE pin is High, the special functions are active. When the MODE pin is Low, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled High when required.

**NC                      No Connection**

This pin is not connected to circuitry within the device.

**PRA                      Probe A (Output)**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

**PRB                      Probe B (Output)**

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

**SDI                      Serial Data Input (Input)**

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

**SDO                      Serial Data Output (Output)**

Serial data output for diagnostic probe. SDO is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

**VCC                      5.0 V Supply Voltage**

High supply voltage.



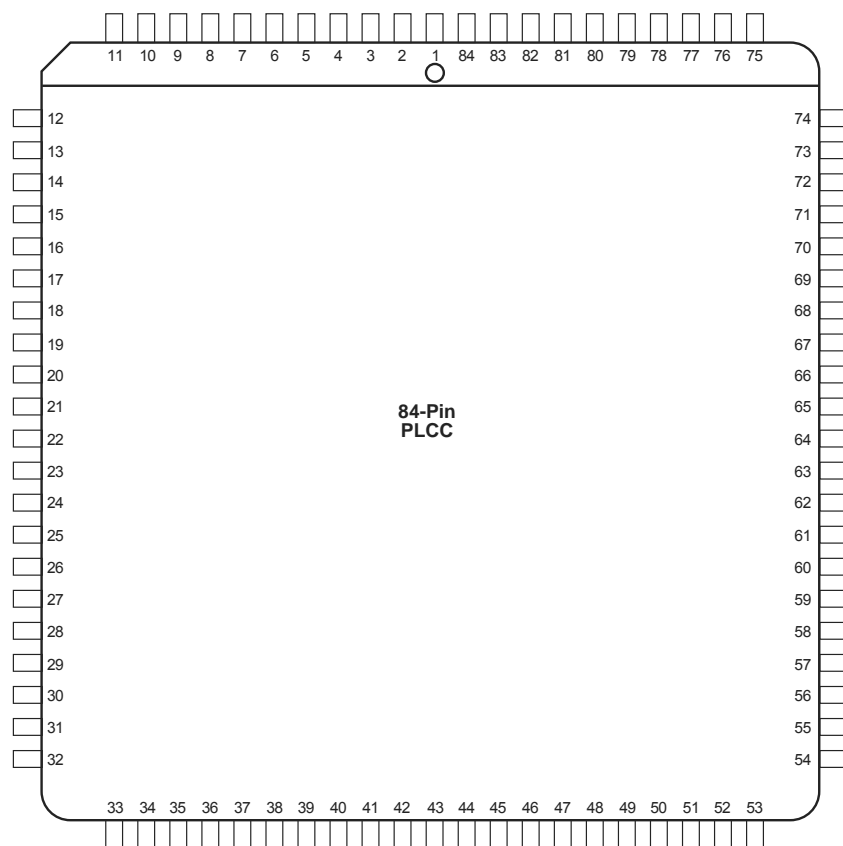
---

## 3 – Package Pin Assignments

---

### PL84

---



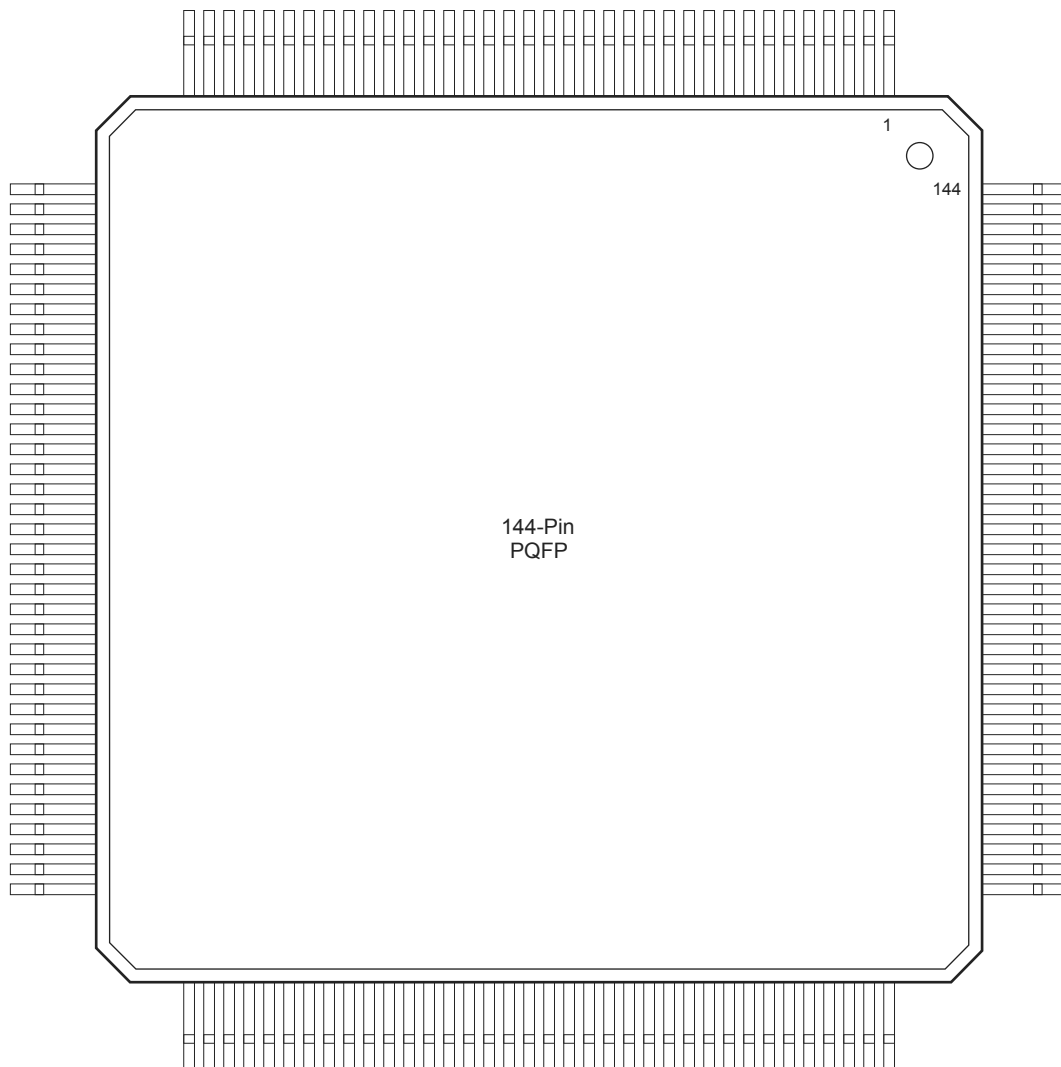
---

#### **Note**

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

## PQ144

---



---

### **Note**

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

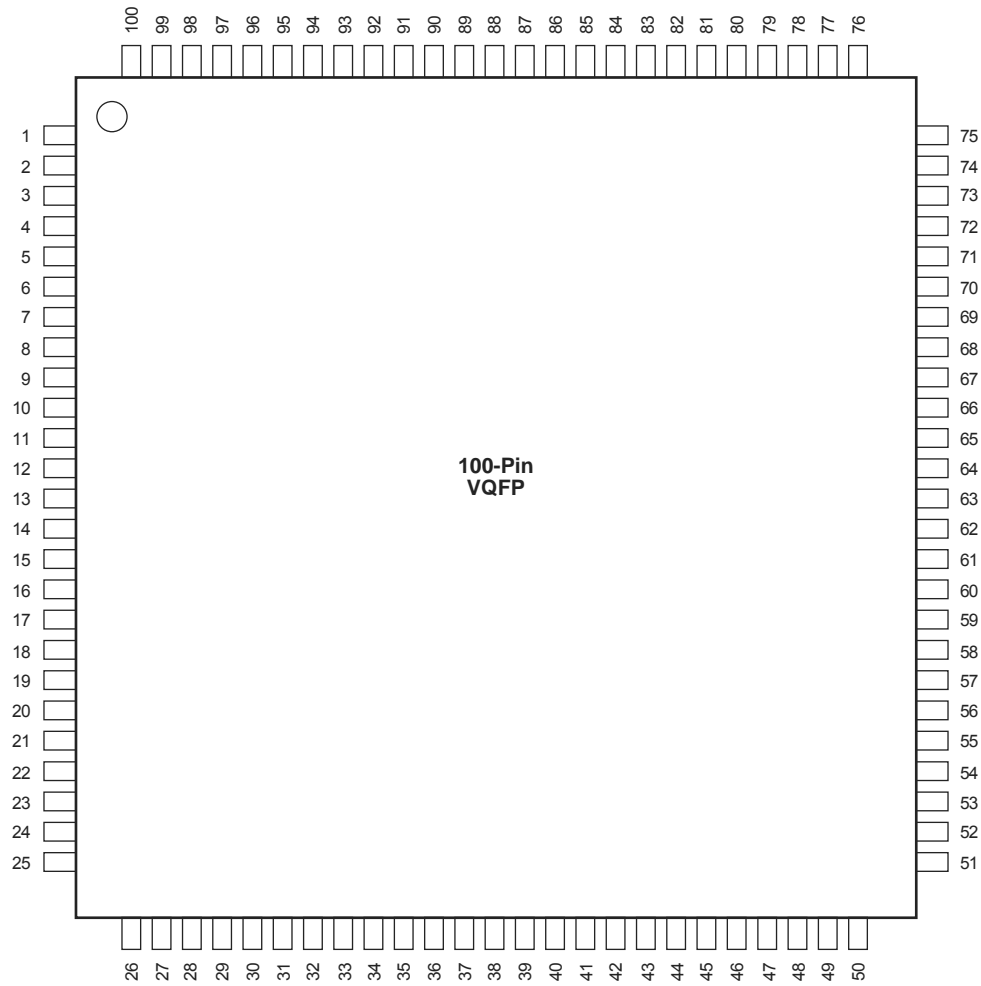
| PQ160      |                 |
|------------|-----------------|
| Pin Number | A1280A Function |
| 2          | DCLK, I/O       |
| 6          | VCC             |
| 11         | GND             |
| 16         | PRB, I/O        |
| 18         | CLKB, I/O       |
| 20         | VCC             |
| 21         | CLKA, I/O       |
| 23         | PRA, I/O        |
| 30         | GND             |
| 35         | VCC             |
| 38         | SDI, I/O        |
| 40         | GND             |
| 44         | GND             |
| 49         | GND             |
| 54         | VCC             |
| 57         | VCC             |
| 58         | VCC             |
| 59         | GND             |
| 60         | VCC             |
| 61         | GND             |
| 64         | GND             |

| PQ160      |                 |
|------------|-----------------|
| Pin Number | A1280A Function |
| 69         | GND             |
| 80         | GND             |
| 82         | SDO             |
| 86         | VCC             |
| 89         | GN              |
| 98         | GND             |
| 99         | GND             |
| 109        | GND             |
| 114        | VCC             |
| 120        | GND             |
| 125        | GND             |
| 130        | GND             |
| 135        | VCC             |
| 138        | VCC             |
| 139        | VCC             |
| 140        | GND             |
| 145        | GND             |
| 150        | VCC             |
| 155        | GND             |
| 159        | MODE            |
| 160        | GND             |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

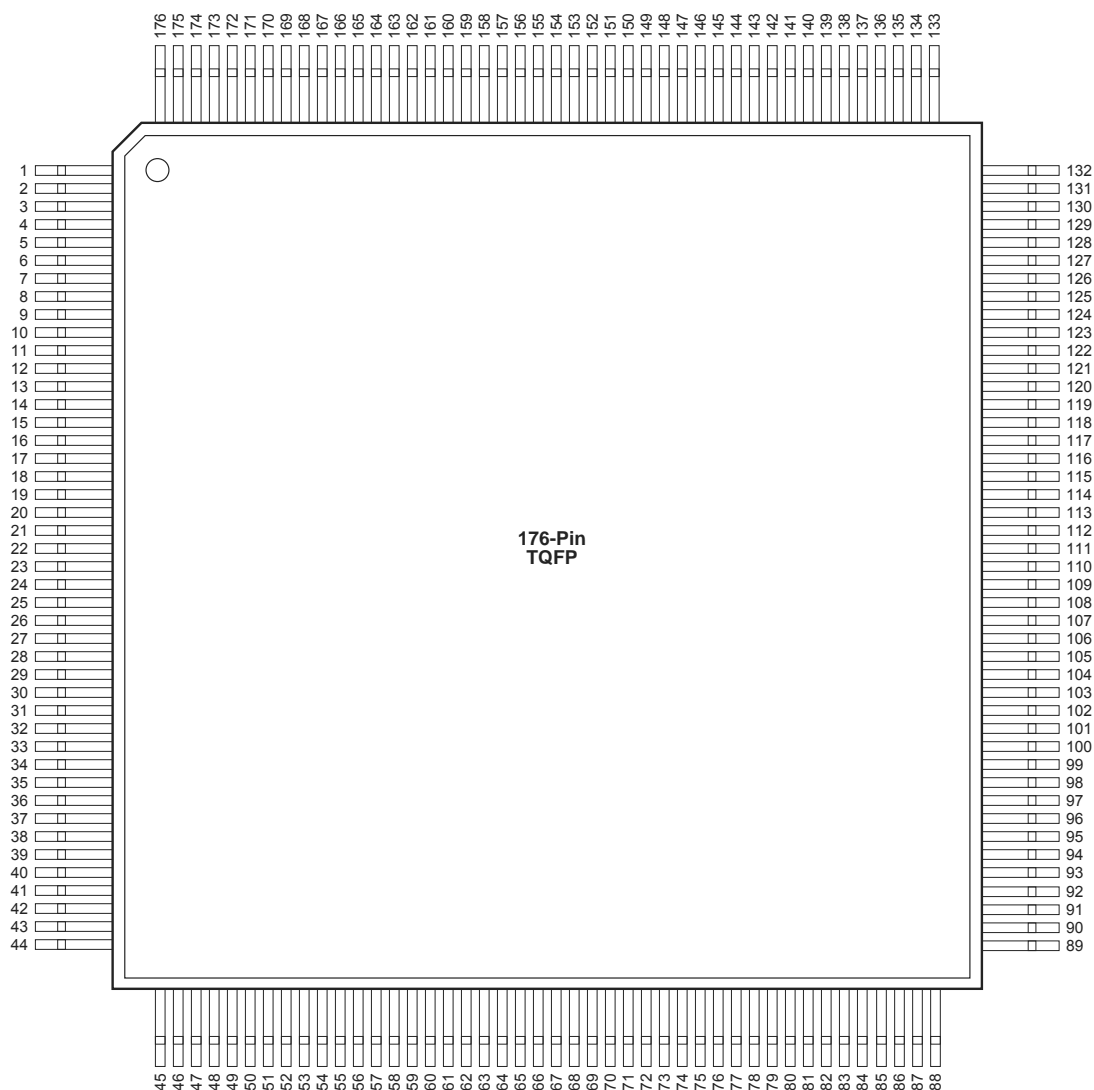
## VQ100



### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

# TQ176



## Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

| TQ176      |                 |                 |
|------------|-----------------|-----------------|
| Pin Number | A1240A Function | A1280A Function |
| 1          | GND             | GND             |
| 2          | MODE            | MODE            |
| 8          | NC              | NC              |
| 10         | NC              | I/O             |
| 11         | NC              | I/O             |
| 13         | NC              | VCC             |
| 18         | GND             | GND             |
| 19         | NC              | I/O             |
| 20         | NC              | I/O             |
| 22         | NC              | I/O             |
| 23         | GND             | GND             |
| 24         | NC              | VCC             |
| 25         | VCC             | VCC             |
| 26         | NC              | I/O             |
| 27         | NC              | I/O             |
| 28         | VCC             | VCC             |
| 29         | NC              | I/O             |
| 33         | NC              | NC              |
| 37         | NC              | I/O             |
| 38         | NC              | NC              |
| 45         | GND             | GND             |
| 52         | NC              | VCC             |
| 54         | NC              | I/O             |
| 55         | NC              | I/O             |
| 57         | NC              | NC              |
| 61         | NC              | I/O             |
| 64         | NC              | I/O             |
| 66         | NC              | I/O             |
| 67         | GND             | GND             |
| 68         | VCC             | VCC             |
| 74         | NC              | I/O             |
| 77         | NC              | NC              |
| 78         | NC              | I/O             |
| 80         | NC              | I/O             |

| TQ176      |                 |                 |
|------------|-----------------|-----------------|
| Pin Number | A1240A Function | A1280A Function |
| 82         | NC              | VCC             |
| 86         | NC              | I/O             |
| 87         | SDO             | SDO             |
| 89         | GND             | GND             |
| 96         | NC              | I/O             |
| 97         | NC              | I/O             |
| 101        | NC              | NC              |
| 103        | NC              | I/O             |
| 106        | GND             | GND             |
| 107        | NC              | I/O             |
| 108        | NC              | I/O             |
| 109        | GND             | GND             |
| 110        | VCC             | VCC             |
| 111        | GND             | GND             |
| 112        | VCC             | VCC             |
| 113        | VCC             | VCC             |
| 114        | NC              | I/O             |
| 115        | NC              | I/O             |
| 116        | NC              | VCC             |
| 121        | NC              | NC              |
| 124        | NC              | I/O             |
| 125        | NC              | I/O             |
| 126        | NC              | NC              |
| 133        | GND             | GND             |
| 135        | SDI, I/O        | SDI, I/O        |
| 136        | NC              | I/O             |
| 140        | NC              | VCC             |
| 143        | NC              | I/O             |
| 144        | NC              | I/O             |
| 145        | NC              | NC              |
| 147        | NC              | I/O             |
| 151        | NC              | I/O             |
| 152        | PRA, I/O        | PRA, I/O        |
| 154        | CLKA, I/O       | CLKA, I/O       |

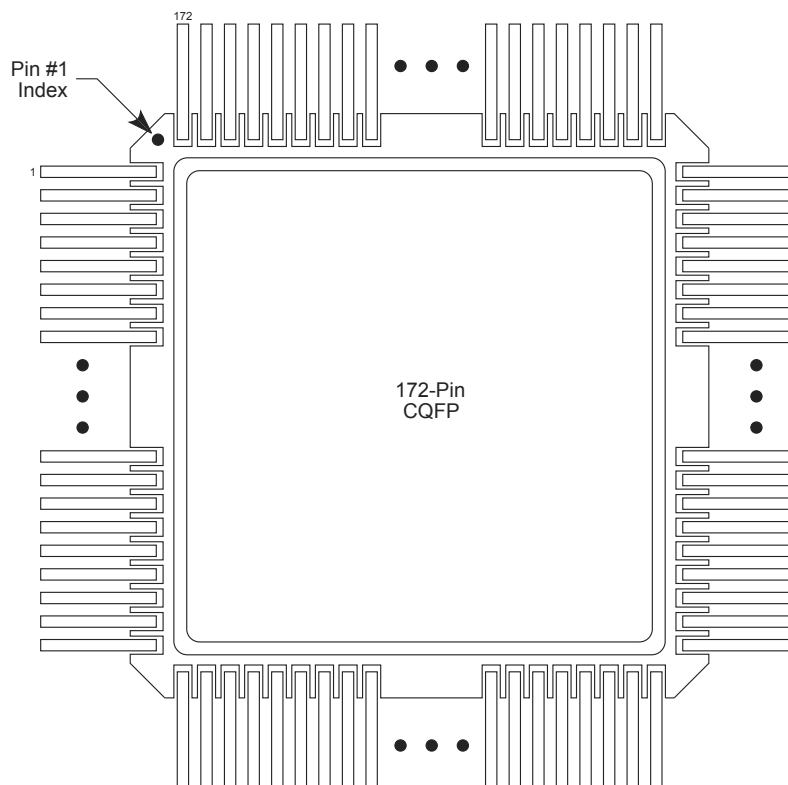
| TQ176      |                 |                 |
|------------|-----------------|-----------------|
| Pin Number | A1240A Function | A1280A Function |
| 155        | VCC             | VCC             |
| 156        | GND             | GND             |
| 158        | CLKB, I/O       | CLKB, I/O       |
| 160        | PRB, I/O        | PRB, I/O        |
| 161        | NC              | I/O             |
| 165        | NC              | NC              |
| 166        | NC              | I/O             |
| 168        | NC              | I/O             |
| 170        | NC              | VCC             |
| 173        | NC              | I/O             |
| 175        | DCLK, I/O       | DCLK, I/O       |

*Notes:*

1. NC denotes no connection.
2. All unlisted pin numbers are user I/Os.
3. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

## CQ172

---



---

### **Note**

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

| PG132      |                 |
|------------|-----------------|
| Pin Number | A1240A Function |
| A1         | MODE            |
| B5         | GND             |
| B6         | CLKB, I/O       |
| B7         | CLKA, I/O       |
| B8         | PRA, I/O        |
| B9         | GND             |
| B12        | SDI, I/O        |
| C3         | DCLK, I/O       |
| C5         | GND             |
| C6         | PRB, I/O        |
| C7         | VCC             |
| C9         | GND             |
| D7         | VCC             |
| E3         | GND             |
| E11        | GND             |
| E12        | GND             |
| F4         | GND             |
| G2         | VCC             |

| PG132      |                 |
|------------|-----------------|
| Pin Number | A1240A Function |
| G3         | VCC             |
| G4         | VCC             |
| G10        | VCC             |
| G11        | VCC             |
| G12        | VCC             |
| G13        | VCC             |
| H13        | GND             |
| J2         | GND             |
| J3         | GND             |
| J11        | GND             |
| K7         | VCC             |
| K12        | GND             |
| L5         | GND             |
| L7         | VCC             |
| L9         | GND             |
| M9         | GND             |
| N12        | SDO             |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

---

## 4 – Datasheet Information

---

### List of Changes

The following table lists critical changes that were made in each version of the datasheet.

| Revision                      | Changes  | Page |
|-------------------------------|--|------|
| Revision 8<br>(January 2012)  | The ACT 2 datasheet was formatted newly in the style used for current datasheets. The same information is present (other than noted in the list of changes for this revision) but divided into chapters. | N/A  |
|                               | Package names used in Table 1 • ACT 2 Product Family Profile and throughout the document were revised to match standards given in <i>Package Mechanical Drawings</i> (SAR 27395).                        | I    |
|                               | The description for SDO pins had earlier been removed from the datasheet and has now been included again, in the "Pin Descriptions" section (SAR 35819).   | 2-21 |
|                               | SDO pin numbers had earlier been removed from package pin assignment tables in the datasheet, and have now been restored to the pin tables (SAR 35819).  | 3-2  |
| Revision 7<br>(June 2006)     | The "Ordering Information" section was revised to include RoHS information.  | II   |
| Revision 6<br>(December 2000) | In the "PG176" package, pin A3 was incorrectly assigned as CLKA, I/O. A3 is a user I/O. Pin A9 is CLKA, I/O.   | 3-21 |





**Microsemi Corporate Headquarters**  
One Enterprise, Aliso Viejo CA 92656 USA  
Within the USA: +1 (949) 380-6100  
Sales: +1 (949) 380-6136  
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at [www.microsemi.com](http://www.microsemi.com).

© 2012 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.