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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	6
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 4x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f1571t-i-mf

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## 2.0 ENHANCED MID-RANGE CPU

This family of devices contains an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect and Relative Addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

FIGURE 2-1:	CORE BLOCK DIAGRAM

- Automatic Interrupt Context Saving
- 16-Level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set



#### 7.3 Interrupts During Sleep

Some interrupts can be used to wake from Sleep. To wake from Sleep, the peripheral must be able to operate without the system clock. The interrupt source must have the appropriate Interrupt Enable bit(s) set prior to entering Sleep.

On waking from Sleep, if the GIE bit is also set, the processor will branch to the interrupt vector. Otherwise, the processor will continue executing instructions after the SLEEP instruction. The instruction directly after the SLEEP instruction will always be executed before branching to the ISR. Refer to **Section 8.0 "Power-Down Mode** (Sleep)" for more details.

#### 7.4 INT Pin

The INT pin can be used to generate an asynchronous edge-triggered interrupt. This interrupt is enabled by setting the INTE bit of the INTCON register. The INTEDG bit of the OPTION\_REG register determines on which edge the interrupt will occur. When the INTEDG bit is set, the rising edge will cause the interrupt. When the INTEDG bit is clear, the falling edge will cause the interrupt. The INTF bit of the INTCON register will be set when a valid edge appears on the INT pin. If the GIE and INTE bits are also set, the processor will redirect program execution to the interrupt vector.

#### 7.5 Automatic Context Saving

Upon entering an interrupt, the return PC address is saved on the stack. Additionally, the following registers are automatically saved in the shadow registers:

- W register
- STATUS register (except for TO and PD)
- BSR register
- FSR registers
- PCLATH register

Upon exiting the Interrupt Service Routine, these registers are automatically restored. Any modifications to these registers during the ISR will be lost. If modifications to any of these registers are desired, the corresponding shadow register should be modified and the value will be restored when exiting the ISR. The shadow registers are available in Bank 31 and are readable and writable. Depending on the user's application, other registers may also need to be saved.

R/W-0/0	R/W-0/0	R-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0				
TMR1GIF	ADIF	RCIF <sup>(1)</sup>	TXIF <sup>(1)</sup>	—	—	TMR2IF	TMR1IF				
bit 7		·					bit 0				
Legend:											
R = Readable	bit	W = Writable	bit								
u = Bit is unch	nanged	x = Bit is unk	nown	U = Unimplei	mented bit, read	as '0'					
'1' = Bit is set		'0' = Bit is cle	ared	-n/n = Value	at POR and BO	R/Value at all c	other Resets				
bit 7	TMR1GIF: T	mer1 Gate Inte	errupt Flag bit								
	1 = Interrupt	1 = Interrupt is pending									
	0 = Interrupt	is not pending									
bit 6	ADIF: ADC Interrupt Flag bit										
	1 = Interrupt is pending										
				<b>`</b>							
DIT 5		RCIF: USART Receive Interrupt Flag bit <sup>(1)</sup>									
	$\perp = Interrupt$	is penaing									
bit 4	TXIF: USAR	T Transmit Inte	rrupt Flag bit <sup>(1</sup>	)							
bit i	1 = Interrupt is pending										
	0 = Interrupt	is not pending									
bit 3-2	Unimplemer	nted: Read as '	0'								
bit 1	TMR2IF: Tim	er2 to PR2 Inte	errupt Flag bit								
	1 = Interrupt	is pending									
	0 = Interrupt	is not pending									
bit 0	TMR1IF: Tim	er1 Overflow I	nterrupt Flag b	it							
	1 = Interrupt	is pending									
	0 = Interrupt	is not pending									
Note 1: PIC	C12(L)F1572 or	nly.									
		2									

## REGISTER 7-5: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

Note:	Interrupt flag bits are set when an interrupt
	condition occurs, regardless of the state of
	its corresponding enable bit or the Global
	Interrupt Enable bit, GIE, of the INTCON
	register. User software should ensure the
	appropriate interrupt flag bits are clear prior
	to enabling an interrupt.

#### 8.3 Register Definitions: Voltage Regulator Control

#### **REGISTER 8-1:** VREGCON: VOLTAGE REGULATOR CONTROL REGISTER<sup>(1)</sup>

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-1/1
—	—	—	—	—	—	VREGPM	Reserved
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

#### bit 7-2 Unimplemented: Read as '0'

bit 1

Unimplemented. Read as 0

VREGPM: Voltage Regulator Power Mode Selection bit

- 1 = Low-Power Sleep mode enabled in Sleep<sup>(2)</sup> Draws lowest current in Sleep, slower wake-up.
- 0 = Normal power mode enabled in Sleep<sup>(2)</sup>
  Draws higher current in Sleep, faster wake-up.

bit 0 **Reserved:** Read as '1', maintain this bit set

**Note 1:** PIC12F1571/2 only.

2: See Section 26.0 "Electrical Specifications"

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	74
IOCAF	_	—	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	122
IOCAN		—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	121
IOCAP		_	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	121
PIE1	TMR1GIE	ADIE	RCIE <sup>(1)</sup>	TXIE <sup>(1)</sup>	—	—	TMR2IE	TMR1IE	75
PIE2	_	—	C1IE	—	—	—	_	—	76
PIE3	_	PWM3IE	PWM2IE	PWM1IE	—	—	_	—	77
PIR1	TMR1GIF	ADIF	RCIF <sup>(1)</sup>	TXIF <sup>(1)</sup>	—	—	TMR2IF	TMR1IF	78
PIR2	_	—	C1IF	—	—	—	_	—	79
PIR3		PWM3IF	PWM2IF	PWM1IF	_	_		_	80
STATUS	_	_	_	TO	PD	Z	DC	С	19
WDTCON	_	_		V	SWDTEN	89			

#### TABLE 8-1: SUMMARY OF REGISTERS ASSOCIATED WITH POWER-DOWN MODE

**Legend:** — = unimplemented, read as '0'. Shaded cells are not used in Power-Down mode.

**Note 1:** PIC12(L)F1572 only.



PIC12(L)F1571/2

## 12.0 INTERRUPT-ON-CHANGE

The PORTA and PORTB pins can be configured to operate as Interrupt-On-Change (IOC) pins. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual port pin, or combination of port pins, can be configured to generate an interrupt. The Interrupt-On-Change module has the following features:

- Interrupt-On-Change enable (Master Switch)
- Individual pin configuration
- · Rising and falling edge detection
- Individual pin interrupt flags

Figure 12-1 is a block diagram of the IOC module.

#### 12.1 Enabling the Module

To allow individual port pins to generate an interrupt, the IOCIE bit of the INTCON register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

#### 12.2 Individual Pin Configuration

For each port pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated bit of the IOCxP register is set. To enable a pin to detect a falling edge, the associated bit of the IOCxN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting both associated bits of the IOCxP and IOCxN registers, respectively.

## 12.3 Interrupt Flags

The IOCAFx and IOCBFx bits located in the IOCAF and IOCBF registers, respectively, are status flags that correspond to the Interrupt-On-Change pins of the associated port. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IOCIF bit of the INTCON register reflects the status of all IOCAFx and IOCBFx bits.

#### 12.4 Clearing Interrupt Flags

The individual status flags, (IOCAFx and IOCBFx bits), can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

#### EXAMPLE 12-1: CLEARING INTERRUPT FLAGS (PORTA EXAMPLE)

MOVLW 0xff XORWF IOCAF, W ANDWF IOCAF, F

## 12.5 Operation in Sleep

The Interrupt-On-Change interrupt sequence will wake the device from Sleep mode, if the IOCIE bit is set.

If an edge is detected while in Sleep mode, the IOCxF register will be updated prior to the first instruction executed out of Sleep.

#### REGISTER 12-3: IOCAF: INTERRUPT-ON-CHANGE PORTA FLAG REGISTER

U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	
—	—		IOCAF<5:0>					
bit 7							bit 0	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-6 Unimplemented: Read as '0'

bit 5-0 **IOCAF<5:0>:** Interrupt-On-Change PORTA Flag bits

1 = An enabled change was detected on the associated pin

Set when IOCAPx = 1 and a rising edge was detected on RAx, or when IOCANx = 1 and a falling edge was detected on RAx.

0 = No change was detected or the user cleared the detected change

#### TABLE 12-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPT-ON-CHANGE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page	
ANSELA		_		ANSA4		ANSA<2:0>			114	
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	74	
IOCAF	—			IOCAF<5:0>						
IOCAN	—	-			IOCA	N<5:0>			121	
IOCAP	—	_		IOCAP<5:0>					121	
TRISA	_	_	TRISA	<5:4>	(1)		TRISA<2:0>	>	113	

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by Interrupt-On-Change.

**Note 1:** Unimplemented, read as '1'.

## 17.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparators are very useful mixed signal building blocks because they provide analog functionality independent of program execution. The analog comparator module includes the following features:

- · Independent comparator control
- · Programmable input selection
- Comparator output is available internally/externally
- · Programmable output polarity
- · Interrupt-On-Change
- · Wake-up from Sleep
- Programmable speed/power optimization
- · PWM shutdown
- · Programmable and Fixed Voltage Reference

#### 17.1 Comparator Overview

A single comparator is shown in Figure 17-2 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

The comparators available for this device are listed in Table 17-1.

#### TABLE 17-1: AVAILABLE COMPARATORS

Device	C1
PIC12(L)F1571	•
PIC12(L)F1572	•



#### FIGURE 17-1: COMPARATOR MODULE SIMPLIFIED BLOCK DIAGRAM

#### 19.5.2.1 T1G Pin Gate Operation

The T1G pin is one source for Timer1 gate control. It can be used to supply an external source to the Timer1 gate circuitry.

#### 19.5.2.2 Timer0 Overflow Gate Operation

When Timer0 increments from FFh to 00h, a low-tohigh pulse will automatically be generated and internally supplied to the Timer1 gate circuitry.

#### 19.5.3 TIMER1 GATE TOGGLE MODE

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full cycle length of a Timer1 gate signal, as opposed to the duration of a single level pulse.

The Timer1 gate source is routed through a flip-flop that changes state on every incrementing edge of the signal. See Figure 19-4 for timing details.

Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When the T1GTM bit is cleared, the flip-flop is cleared and held clear. This is necessary in order to control which edge is measured.

**Note:** Enabling Toggle mode at the same time as changing the gate polarity may result in indeterminate operation.

#### 19.5.4 TIMER1 GATE SINGLE-PULSE MODE

When Timer1 Gate Single-Pulse mode is enabled, it is possible to capture a single-pulse gate event. Timer1 Gate Single-Pulse mode is first enabled by setting the T1GSPM bit in the T1GCON register. Next, the T1GGO/ DONE bit in the T1GCON register must be set. The Timer1 will be fully enabled on the next incrementing edge. On the next trailing edge of the pulse, the T1GGO/ DONE bit will automatically be cleared. No other gate events will be allowed to increment Timer1 until the T1GGO/DONE bit is once again set in software. See Figure 19-5 for timing details.

If the Single-Pulse Gate mode is disabled by clearing the T1GSPM bit in the T1GCON register, the T1GGO/DONE bit should also be cleared.

Enabling the Toggle mode and the Single-Pulse mode simultaneously will permit both sections to work together. This allows the cycle times on the Timer1 gate source to be measured. See Figure 19-6 for timing details.

#### 19.5.5 TIMER1 GATE VALUE STATUS

When Timer1 gate value status is utilized, it is possible to read the most current level of the gate control value. The value is stored in the T1GVAL bit in the T1GCON register. The T1GVAL bit is valid even when the Timer1 gate is not enabled (TMR1GE bit is cleared).

#### 19.5.6 TIMER1 GATE EVENT INTERRUPT

When Timer1 gate event interrupt is enabled, it is possible to generate an interrupt upon the completion of a gate event. When the falling edge of T1GVAL occurs, the TMR1GIF flag bit in the PIR1 register will be set. If the TMR1GIE bit in the PIE1 register is set, then an interrupt will be recognized.

The TMR1GIF flag bit operates even when the Timer1 gate is not enabled (TMR1GE bit is cleared).

#### 21.1 EUSART Asynchronous Mode

The EUSART transmits and receives data using the standard Non-Return-to-Zero (NRZ) format. NRZ is implemented with two levels: a VOH mark state which represents a '1' data bit, and a VOL space state which represents a '0' data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port Idles in the mark state. Each character transmission consists of one Start bit, followed by eight or nine data bits and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is eight bits. Each transmitted bit persists for a period of 1/(Baud Rate). An on-chip dedicated 8-bit/16-bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. See Table 21-5 for examples of baud rate configurations.

The EUSART transmits and receives the LSb first. The EUSART's transmitter and receiver are functionally independent, but share the same data format and baud rate. Parity is not supported by the hardware, but can be implemented in software and stored as the ninth data bit.

#### 21.1.1 EUSART ASYNCHRONOUS TRANSMITTER

The EUSART transmitter block diagram is shown in Figure 21-1. The heart of the transmitter is the serial Transmit Shift Register (TSR), which is not directly accessible by software. The TSR obtains its data from the transmit buffer, which is the TXREG register.

#### 21.1.1.1 Enabling the Transmitter

The EUSART transmitter is enabled for asynchronous operations by configuring the following three control bits:

- TXEN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the TXEN bit of the TXSTA register enables the transmitter circuitry of the EUSART. Clearing the SYNC bit of the TXSTA register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCSTA register enables the EUSART and automatically configures the TX/CK I/O pin as an output. If the TX/CK pin is shared with an analog peripheral, the analog I/O function must be disabled by clearing the corresponding ANSELx bit.

**Note:** The TXIF transmitter interrupt flag is set when the TXEN enable bit is set.

#### 21.1.1.2 Transmitting Data

A transmission is initiated by writing a character to the TXREG register. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the TXREG until the Stop bit of the previous character has been transmitted. The pending character in the TXREG is then transferred to the TSR in one TCY immediately following the Stop bit transmission. The transmission of the Start bit, data bits and Stop bit sequence commences immediately following the transfer of the data to the TSR from the TXREG.

#### 21.1.1.3 Transmit Data Polarity

The polarity of the transmit data can be controlled with the SCKP bit of the BAUDCON register. The default state of this bit is '0' which selects high true transmit ldle and data bits. Setting the SCKP bit to '1' will invert the transmit data resulting in low true ldle and data bits. The SCKP bit controls transmit data polarity in Asynchronous mode only. In Synchronous mode, the SCKP bit has a different function. See **Section 21.5.1.2 "Clock Polarity"**.

#### 21.1.1.4 Transmit Interrupt Flag

The TXIF interrupt flag bit of the PIR1 register is set whenever the EUSART transmitter is enabled and no character is being held for transmission in the TXREG. In other words, the TXIF bit is only clear when the TSR is busy with a character and a new character has been queued for transmission in the TXREG. The TXIF flag bit is not cleared immediately upon writing TXREG. TXIF becomes valid in the second instruction cycle following the write execution. Polling TXIF immediately following the TXREG write will return invalid results. The TXIF bit is read-only, it cannot be set or cleared by software.

The TXIF interrupt can be enabled by setting the TXIE interrupt enable bit of the PIE1 register. However, the TXIF flag bit will be set whenever the TXREG is empty, regardless of the state of the TXIE enable bit.

To use interrupts when transmitting data, set the TXIE bit only when there is more data to send. Clear the TXIE interrupt enable bit upon writing the last character of the transmission to the TXREG.

## 22.0 16-BIT PULSE-WIDTH MODULATION (PWM) MODULE

The Pulse-Width Modulation (PWM) module generates a pulse-width modulated signal determined by the phase, duty cycle, period and offset event counts that are contained in the following registers:

- PWMxPH register
- PWMxDC register
- PWMxPR register
- PWMxOF register

Figure 22-1 shows a simplified block diagram of the PWM operation.

Each PWM module has four modes of operation:

- Standard
- Set On Match
- Toggle On Match
- · Center-Aligned

For a more detailed description of each PWM mode, refer to **Section 22.2** "**PWM Modes**".

Each PWM module has four Offset modes:

- Independent Run
- Slave Run with Synchronous Start
- · One-Shot Slave with Synchronous Start
- Continuous Run Slave with Synchronous Start and Timer Reset

Using the Offset modes, each PWM module can offset its waveform relative to any other PWM module in the same device. For a more detailed description of the Offset modes, refer to **Section 22.3 "Offset Modes"**.

Every PWM module has a configurable reload operation to ensure all event count buffers change at the end of a period, thereby avoiding signal glitches. Figure 22-2 shows a simplified block diagram of the reload operation. For a more detailed description of the reload operation, refer to **Section 22.4 "Reload Operation"**.



Note 1: A PWM module cannot trigger from its own offset match event. The input corresponding to a PWM module's own offset match is reserved.

#### FIGURE 22-1: 16-BIT PWM BLOCK DIAGRAM

#### Rev. 10-000 146B 7/8/201 5 Period Duty Cycle Phase Offset PWMxCLK PWMxPR 10 PWMxPH 3 PWMxDC 5 PWMxOF 2 PWMxTMR 2 3 5 6 8 9 10 0 2 3 4 5 6 0 4 7 1 PWMxOUT OFx\_match PHx\_match DCx\_match PRx\_match PWMyTMR 3 0 3 2 0 2 0 2 4 2 0 3 4 1 4 1 1 PWMyPR 4 PWMyPH PWMyDC 1 PWMyOUT Note: PWMx = Master, PWMy = Slave

#### **FIGURE 22-8:**

#### INDEPENDENT RUN MODE TIMING DIAGRAM

PIC12(L )F1571,



#### TABLE 26-17: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)									
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Conditions			
US120	TCKH2DTV	SYNC XMIT (Master and Slave)		80	ns	$3.0V \le V\text{DD} \le 5.5V$			
		Clock High to Data-Out Valid		100	ns	$1.8V \leq V\text{DD} \leq 5.5V$			
US121	TCKRF	Clock Out Rise Time and Fall Time (Master mode)	—	45	ns	$3.0V \leq V\text{DD} \leq 5.5V$			
			—	50	ns	$1.8V \leq V\text{DD} \leq 5.5V$			
US122	TDTRF	Data-Out Rise Time and Fall Time		45	ns	$3.0V \leq V\text{DD} \leq 5.5V$			
				50	ns	$1.8V \le V\text{DD} \le 5.5V$			

#### FIGURE 26-14: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



#### TABLE 26-18: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)										
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Conditions				
US125	TDTV2CKL	SYNC RCV (Master and Slave) Data-Hold before CK $\downarrow$ (DT hold time)	10		ns					
US126	TCKL2DTL	Data-Hold after CK $\downarrow$ (DT hold time)	15		ns					



FIGURE 27-11: IDD TYPICAL, EC OSCILLATOR, HIGH-POWER MODE, PIC12F1571/2 ONLY



FIGURE 27-12: IDD MAXIMUM, EC OSCILLATOR, HIGH-POWER MODE, PIC12F1571/2 ONLY

# PIC12(L)F1571/2











FIGURE 27-28: IPD, BROWN-OUT RESET (BOR), BORV = 1, PIC12F1571/2 ONLY



# 28.0 DEVELOPMENT SUPPORT

The PIC<sup>®</sup> microcontrollers (MCU) and dsPIC<sup>®</sup> digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
- MPLAB<sup>®</sup> X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM<sup>™</sup> Assembler
  - MPLINK<sup>™</sup> Object Linker/ MPLIB<sup>™</sup> Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- · Simulators
  - MPLAB X SIM Software Simulator
- · Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

#### 28.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows<sup>®</sup>, Linux and Mac OS<sup>®</sup> X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- · Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- · Call graph window
- Project-Based Workspaces:
- · Multiple projects
- Multiple tools
- · Multiple configurations
- · Simultaneous debugging sessions

File History and Bug Tracking:

- · Local file history feature
- Built-in support for Bugzilla issue tracker

# TABLE 29-1:8-LEAD 3x3x0.9 DFN (MF) TOP<br/>MARKING

Part Number	Marking		
PIC12F1571-E/MF	MFY0/YYWW/NNN		
PIC12F1572-E/MF	MGA0/YYWW/NNN		
PIC12F1571-I/MF	MFZ0		
PIC12F1572-I/MF	MGB0		
PIC12LF1571-E/MF	MGC0		
PIC12LF1572-E/MF	MGE0		
PIC12LF1571-I/MF	MGD0		
PIC12LF1572-I/MF	MGF0		

# TABLE 29-2:8-LEAD 3x3x0.5 UDFN (RF)TOP MARKING

Part Number	Marking		
PIC12F1571-E/MF	MFY0/YYWW/NNN		
PIC12F1572-E/MF	MGA0/YYWW/NNN		
PIC12F1571-I/MF	MFZ0		
PIC12F1572-I/MF	MGB0		
PIC12LF1571-E/MF	MGC0		
PIC12LF1572-E/MF	MGE0		
PIC12LF1571-I/MF	MGD0		
PIC12LF1572-I/MF	MGF0		

#### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension	Limits	MIN	NOM	MAX	
Number of Pins	N	8			
Pitch	е	1.27 BSC			
Overall Height	Α	-	-	1.75	
Molded Package Thickness	A2	1.25	-	-	
Standoff §	A1	0.10	-	0.25	
Overall Width	E	6.00 BSC			
Molded Package Width	E1	3.90 BSC			
Overall Length	D	4.90 BSC			
Chamfer (Optional)	h	0.25	-	0.50	
Foot Length	L	0.40	-	1.27	
Footprint	L1	1.04 REF			
Foot Angle	$\varphi$	0°	-	8°	
Lead Thickness	С	0.17	-	0.25	
Lead Width	b	0.31	-	0.51	
Mold Draft Angle Top	α	5°	-	15°	
Mold Draft Angle Bottom	β	5°	-	15°	

#### Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.

- 4. Dimensioning and tolerancing per ASME Y14.5M
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

## 8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (RF) - 3x3x0.50 mm Body [UDFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-254A Sheet 1 of 2