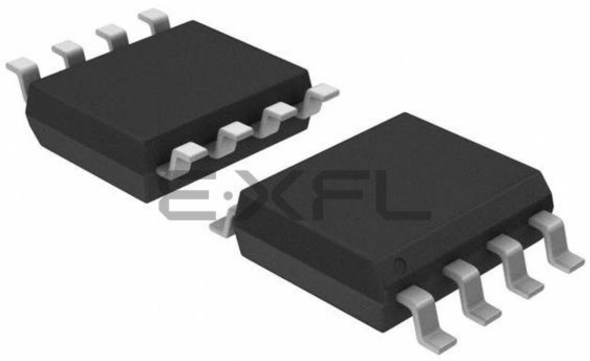


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	6
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 4x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12lf1571-e-sn

1.0 DEVICE OVERVIEW

The PIC12(L)F1571/2 devices are described within this data sheet. The block diagram of these devices is shown in Figure 1-1, the available peripherals are shown in Table 1-1 and the pinout descriptions are shown in Table 1-2.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC12(L)F1571	PIC12(L)F1572
Analog-to-Digital Converter (ADC)		●	●
Complementary Wave Generator (CWG)		●	●
Digital-to-Analog Converter (DAC)		●	●
Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)			●
Fixed Voltage Reference (FVR)		●	●
Temperature Indicator		●	●
Comparators			
	C1	●	●
PWM Modules			
	PWM1	●	●
	PWM2	●	●
	PWM3	●	●
Timers			
	Timer0	●	●
	Timer1	●	●
	Timer2	●	●

1.1 Register and Bit Naming Conventions

1.1.1 REGISTER NAMES

When there are multiple instances of the same peripheral in a device, the peripheral control registers will be depicted as the concatenation of a peripheral identifier, peripheral instance and control identifier. The control registers section will show just one instance of all the register names with an ‘x’ in the place of the peripheral instance number. This naming convention may also be applied to peripherals when there is only one instance of that peripheral in the device to maintain compatibility with other devices in the family that contain more than one.

1.1.2 BIT NAMES

There are two variants for bit names:

- Short name: Bit function abbreviation
- Long name: Peripheral abbreviation + short name

1.1.2.1 Short Bit Names

Short bit names are an abbreviation for the bit function. For example, some peripherals are enabled with the EN bit. The bit names shown in the registers are the short name variant.

Short bit names are useful when accessing bits in C programs. The general format for accessing bits by the short name is *RegisterName*bits.*ShortName*. For example, the enable bit, EN, in the COG1CON0 register can be set in C programs with the instruction, `COG1CON0bits.EN = 1`.

Short names are generally not useful in assembly programs because the same name may be used by different peripherals in different bit positions. When this occurs, during the include file generation, all instances of that short bit name are appended with an underscore, plus the name of the register in which the bit resides, to avoid naming contentions.

TABLE 3-10: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on All Other Resets
Bank 2											
10Ch	LATA	—	—	LATA<5:4>		—	LATA<2:0>			`--xx -xxx`	`--uu -uuu`
10Dh	—	Unimplemented								—	—
10Eh	—	Unimplemented								—	—
10Fh	—	Unimplemented								—	—
110h	—	Unimplemented								—	—
111h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	—	C1SP	C1HYS	C1SYNC	`0000 -100`	`0000 -100`
112h	CM1CON1	C1INTP	C1INTN	C1PCH<1:0>		—	C1NCH<2:0>			`0000 -000`	`0000 -000`
113h	—	Unimplemented								—	—
114h	—	Unimplemented								—	—
115h	CMOUT	—	—	—	—	—	—	—	MC1OUT	`---- ---0`	`---- ---0`
116h	BORCON	SBOREN	BORFS	—	—	—	—	—	BORRDY	`10-- ---q`	`uu-- ---u`
117h	FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		`0q00 0000`	`0q00 0000`
118h	DAC1CON0	DACEN	—	DACOE	—	DACPSS<1:0>		—	—	`0-0- 00--`	`0-0- 00--`
119h	DAC1CON1	—	—	—	DACR<4:0>					`---0 0000`	`---0 0000`
11Ah to 11Ch	—	Unimplemented								—	—
11Dh	APFCON	RXDTSEL	CWGASEL	CWGBSEL	—	T1GSEL	TXCKSEL	P2SEL	P1SEL	`000- 0000`	`000- 0000`
11Eh	—	Unimplemented								—	—
11Fh	—	Unimplemented								—	—
Bank 3											
18Ch	ANSELA	—	—	—	ANSA4	—	ANSA<2:0>			`---1 -111`	`---1 -111`
18Dh	—	Unimplemented								—	—
18Eh	—	Unimplemented								—	—
18Fh	—	Unimplemented								—	—
190h	—	Unimplemented								—	—
191h	PMADRL	Flash Program Memory Address Register Low Byte								`0000 0000`	`0000 0000`
192h	PMADRH	—(3)	Flash Program Memory Address Register High Byte							`1000 0000`	`1000 0000`
193h	PMDATL	Flash Program Memory Read Data Register Low Byte								`xxxx xxxx`	`uuuu uuuu`
194h	PMDATH	—	—	Flash Program Memory Read Data Register High Byte						`--xx xxxx`	`--uu uuuu`
195h	PMCON1	—(3)	CFGS	LWLO	FREE	WRERR	WREN	WR	RD	`1000 x000`	`1000 q000`
196h	PMCON2	Flash Program Memory Control Register 2								`0000 0000`	`0000 0000`
197h	VREGCON(1)	—	—	—	—	—	—	VREGPM	Reserved	`---- --01`	`---- --01`
198h	—	Unimplemented								—	—
199h	RCREG	USART Receive Data Register								`0000 0000`	`0000 0000`
19Ah	TXREG	USART Transmit Data Register								`0000 0000`	`0000 0000`
19Bh	SPBRGL	Baud Rate Generator Data Register Low								`0000 0000`	`0000 0000`
19Ch	SPBRGH	Baud Rate Generator Data Register High								`0000 0000`	`0000 0000`
19Dh	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	`0000 000x`	`0000 000x`
19Eh	TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	`0000 0010`	`0000 0010`
19Fh	BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	`01-0 0-00`	`01-0 0-00`

Legend: x = unknown; u = unchanged; q = value depends on condition; — = unimplemented; `r` = reserved. Shaded locations are unimplemented, read as '0'.
Note 1: PIC12F1571/2 only.
2: PIC12(L)F1572 only.
3: Unimplemented, read as '1'.

TABLE 3-10: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on All Other Resets
Bank 4											
20Ch	WPUA	—	—	WPUA<5:0>						--11 1111	--11 1111
20Dh	—	Unimplemented								—	—
20Eh to 21Fh	—	Unimplemented								—	—
Bank 5											
28Ch	ODCONA	—	—	ODA<5:4>		—	ODA<2:0>			--11 -111	--11 -111
28Dh to 29Fh	—	Unimplemented								—	—
Bank 6											
30Ch	SLRCONA	—	—	SLRA<5:4>		—	SLRA<2:0>			--11 -111	--11 -111
30Dh to 31Fh	—	Unimplemented								—	—
Bank 7											
38Ch	INLVLA	—	—	INLVLA<5:0>						--11 1111	--11 1111
38Dh to 390h	—	Unimplemented								—	—
391h	IOCAP	—	—	IOCAP<5:0>						--00 0000	--00 0000
392h	IOCAN	—	—	IOCAN<5:0>						--00 0000	--00 0000
393h	IOCAF	—	—	IOCAF<5:0>						--00 0000	--00 0000
394h to 39Fh	—	Unimplemented								—	—
Bank 8											
40Ch to 41Fh	—	Unimplemented								—	—
Bank 9											
48Ch to 49Fh	—	Unimplemented								—	—

Legend: x = unknown; u = unchanged; q = value depends on condition; — = unimplemented; r = reserved. Shaded locations are unimplemented, read as '0'.
Note 1: PIC12F1571/2 only.
2: PIC12(L)F1572 only.
3: Unimplemented, read as '1'.

TABLE 3-10: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

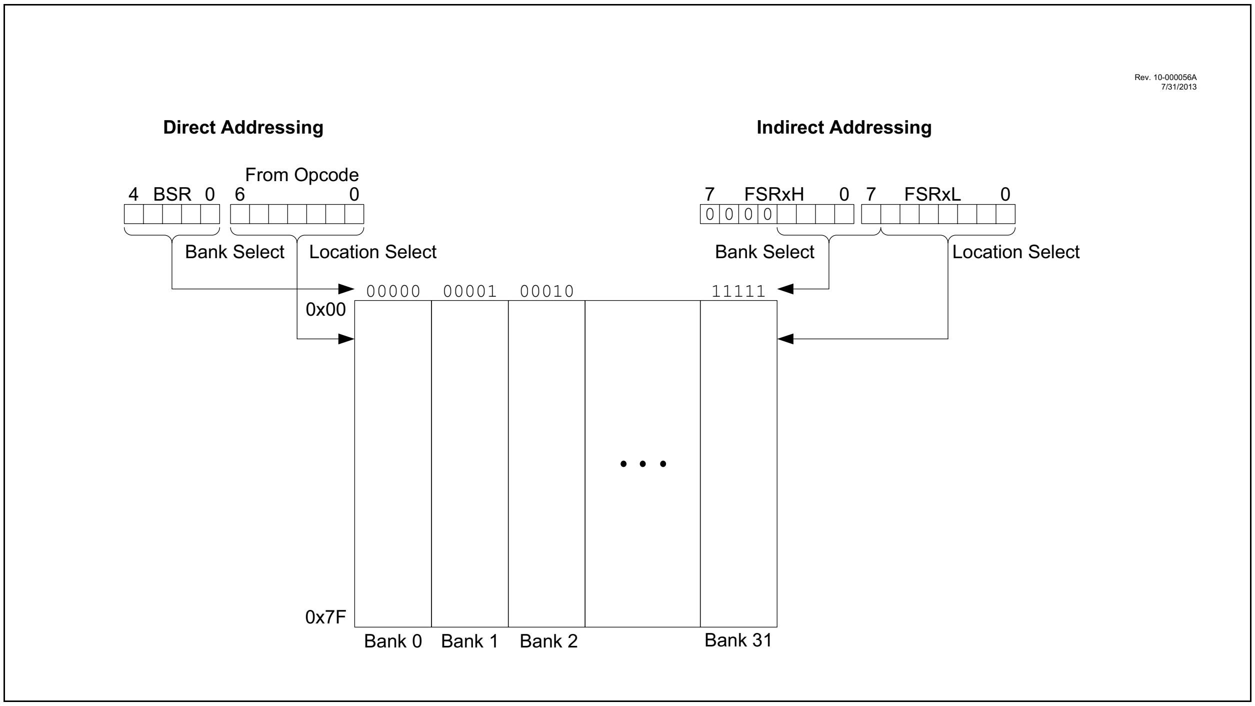
Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on All Other Resets
Bank 27											
D8Ch	—	Unimplemented								—	—
D8Dh	—	Unimplemented								—	—
D8Eh	PWMEN	—	—	—	—	—	PWM3EN_A	PWM2EN_A	PWM1EN_A	---- -000	---- -000
D8Fh	PWMLD	—	—	—	—	—	PWM3LDA_A	PWM2LDA_A	PWM1LDA_A	---- -000	---- -000
D90h	PWMOUT	—	—	—	—	—	PWM3OUT_A	PWM2OUT_A	PWM1OUT_A	---- -000	---- -000
D91h	PWM1PHL	PH<7:0>								xxxx xxxx	uuuu uuuu
D92h	PWM1PHH	PH<15:8>								xxxx xxxx	uuuu uuuu
D93h	PWM1DCL	DC<7:0>								xxxx xxxx	uuuu uuuu
D94h	PWM1DCH	DC<15:8>								xxxx xxxx	uuuu uuuu
D95h	PWM1PRL	PR<7:0>								xxxx xxxx	uuuu uuuu
D96h	PWM1PRH	PR<15:8>								xxxx xxxx	uuuu uuuu
D97h	PWM1OFL	OF<7:0>								xxxx xxxx	uuuu uuuu
D98h	PWM1OFH	OF<15:8>								xxxx xxxx	uuuu uuuu
D99h	PWM1TMRL	TMR<7:0>								xxxx xxxx	uuuu uuuu
D9Ah	PWM1TMRH	TMR<15:8>								xxxx xxxx	uuuu uuuu
D9Bh	PWM1CON	PWM1EN	PWM1OE	PWM1OUT	PWM1POL	PWM1MODE<1:0>		—	—	0000 00--	0000 00--
D9Ch	PWM1INTE	—	—	—	—	PWM1OFIE	PWM1PHIE	PWM1DCIE	PWM1PRIE	---- 000	---- 000
D9Dh	PWM1INTF	—	—	—	—	PWM1OFIF	PWM1PHIF	PWM1DCIF	PWM1PRIF	---- 000	---- 000
D9Eh	PWM1CLKCON	—	PWM1PS<2:0>			—	—	PWM1CS<1:0>		-000 -000	-000 --00
D9Fh	PWM1LDCON	PWM1LDA	PWM1LDT	—	—	—	—	PWM1LDS<1:0>		00-- -000	00-- --00
DA0h	PWM1OFCON	—	PWM1OFM<1:0>		PWM1OFO	—	—	PWM1OFS<1:0>		-000 -000	-000 --00
DA1h	PWM2PHL	PH<7:0>								xxxx xxxx	uuuu uuuu
DA2h	PWM2PHH	PH<15:8>								xxxx xxxx	uuuu uuuu
DA3h	PWM2DCL	DC<7:0>								xxxx xxxx	uuuu uuuu
DA4h	PWM2DCH	DC<15:8>								xxxx xxxx	uuuu uuuu
DA5h	PWM2PRL	PR<7:0>								xxxx xxxx	uuuu uuuu
DA6h	PWM2PRH	PR<15:8>								xxxx xxxx	uuuu uuuu
DA7h	PWM2OFL	OF<7:0>								xxxx xxxx	uuuu uuuu
DA8h	PWM2OFH	OF<15:8>								xxxx xxxx	uuuu uuuu
DA9h	PWM2TMRL	TMR<7:0>								xxxx xxxx	uuuu uuuu
DAAh	PWM2TMRH	TMR<15:8>								xxxx xxxx	uuuu uuuu
DABh	PWM2CON	PWM2EN	PWM2OE	PWM2OUT	PWM2POL	PWM2MODE<1:0>		—	—	0000 00--	0000 00--
DACh	PWM2INTE	—	—	—	—	PWM2OFIE	PWM2PHIE	PWM2DCIE	PWM2PRIE	---- 000	---- 000
DADh	PWM2INTF	—	—	—	—	PWM2OFIF	PWM2PHIF	PWM2DCIF	PWM2PRIF	---- 000	---- 000
DAEh	PWM2CLKCON	—	PWM2PS<2:0>			—	—	PWM2CS<1:0>		-000 -000	-000 --00
DAFh	PWM2LDCON	PWM2LDA	PWM2LDT	—	—	—	—	PWM2LDS<1:0>		00-- -000	00-- --00

Legend: x = unknown; u = unchanged; q = value depends on condition; — = unimplemented; r = reserved. Shaded locations are unimplemented, read as ‘0’.
Note 1: PIC12F1571/2 only.
2: PIC12(L)F1572 only.
3: Unimplemented, read as ‘1’.

3.6.1 TRADITIONAL DATA MEMORY

The traditional data memory is a region from FSR address, 0x000, to FSR address, 0xFFF. The addresses correspond to the absolute addresses of all SFR, GPR and common registers.

FIGURE 3-10: TRADITIONAL DATA MEMORY MAP



REGISTER 5-3: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	TUN<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **TUN<5:0>:** Frequency Tuning bits
`100000` = Minimum frequency
•
•
•
`111111` =
`000000` = Oscillator module is running at the factory-calibrated frequency
`000001` =
•
•
•
`011110` =
`011111` = Maximum frequency

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	SPLLEN	IRCF<3:0>				—	SCS<1:0>		55
OSCSTAT	—	PLLR	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS	56
OSCTUNE	—	—	TUN<5:0>						57
T1CON	TMR1CS<1:0>		T1CKPS<1:0>		—	$\overline{\text{T1SYNC}}$	—	TMR1ON	167

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used by clock sources.

TABLE 5-3: SUMMARY OF CONFIGURATION WORD WITH CLOCK SOURCES

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	—	—	$\overline{\text{CLKOUTEN}}$	BOREN<1:0>		—	42
	7:0	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE<1:0>		—	FOSC<1:0>		

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used by clock sources.

6.13 Power Control (PCON) Register

The Power Control (PCON) register contains flag bits to differentiate between a:

- Power-on Reset ($\overline{POR}$)
- Brown-out Reset ($\overline{BOR}$)
- RESET Instruction Reset ($\overline{RI}$)
- $\overline{MCLR}$ Reset ($\overline{RMCLR}$)
- Watchdog Timer Reset ($\overline{RWDT}$)
- Stack Underflow Reset (STKUNF)
- Stack Overflow Reset (STKOVF)

The PCON register bits are shown in Register 6-2.

6.14 Register Definitions: Power Control

REGISTER 6-2: PCON: POWER CONTROL REGISTER

R/W/HS-0/q	R/W/HS-0/q	U-0	R/W/HC-1/q	R/W/HC-1/q	R/W/HC-1/q	R/W/HC-q/u	R/W/HC-q/u
STKOVF	STKUNF	—	$\overline{RWDT}$	$\overline{RMCLR}$	$\overline{RI}$	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **STKOVF:** Stack Overflow Reset Flag bit
1 = A Stack Overflow Reset occurred
0 = A Stack Overflow Reset has not occurred or is cleared by firmware

bit 6 **STKUNF:** Stack Underflow Reset Flag bit
1 = A Stack Underflow Reset occurred
0 = A Stack Underflow Reset has not occurred or is cleared by firmware

bit 5 **Unimplemented:** Read as '0'

bit 4 **$\overline{RWDT}$:** Watchdog Timer Reset Flag bit
1 = A Watchdog Timer Reset has not occurred or is set by firmware
0 = A Watchdog Timer Reset has occurred (cleared by hardware)

bit 3 **$\overline{RMCLR}$:** $\overline{MCLR}$ Reset Flag bit
1 = A $\overline{MCLR}$ Reset has not occurred or is set by firmware
0 = A $\overline{MCLR}$ Reset has occurred (cleared by hardware)

bit 2 **$\overline{RI}$:** RESET Instruction Flag bit
1 = A RESET instruction has not been executed or set by firmware
0 = A RESET instruction has been executed (cleared by hardware)

bit 1 **$\overline{POR}$:** Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Power-on Reset or Brown-out Reset occurs)

REGISTER 7-2: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
TMR1GIE	ADIE	RCIE(1)	TXIE(1)	—	—	TMR2IE	TMR1IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **TMR1GIE:** Timer1 Gate Interrupt Enable bit
1 = Enables the Timer1 gate acquisition interrupt
0 = Disables the Timer1 gate acquisition interrupt

bit 6 **ADIE:** Analog-to-Digital Converter (ADC) Interrupt Enable bit
1 = Enables the ADC interrupt
0 = Disables the ADC interrupt

bit 5 **RCIE:** USART Receive Interrupt Enable bit(1)
1 = Enables the USART receive interrupt
0 = Disables the USART receive interrupt

bit 4 **TXIE:** USART Transmit Interrupt Enable bit(1)
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1 **TMR2IE:** TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the Timer2 to PR2 match interrupt
0 = Disables the Timer2 to PR2 match interrupt

bit 0 **TMR1IE:** Timer1 Overflow Interrupt Enable bit
1 = Enables the Timer1 overflow interrupt
0 = Disables the Timer1 overflow interrupt

Note 1: PIC12(L)F1572 only.
2: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

Note:	Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 15-2: ADCON1: ADC CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
ADFM	ADCS<2:0>			—	—	ADPREF<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **ADFM:** ADC Result Format Select bit
1 = Right justified; six Most Significant bits of ADRESH are set to ‘0’ when the conversion result is loaded
0 = Left justified; six Least Significant bits of ADRESL are set to ‘0’ when the conversion result is loaded

bit 6-4 **ADCS<2:0>:** ADC Conversion Clock Select bits
000 = FOSC/2
001 = FOSC/8
010 = FOSC/32
011 = FRC (clock supplied from an internal RC oscillator)
100 = FOSC/4
101 = FOSC/16
110 = FOSC/64
111 = FRC (clock supplied from an internal RC oscillator)

bit 3-2 **Unimplemented**: Read as ‘0’

bit 1-0 **ADPREF<1:0>:** ADC Positive Voltage Reference Configuration bits
00 = VRPOS is connected to VDD
01 = Reserved
10 = VRPOS is connected to external VREF+ pin(1)
11 = VRPOS is connected to internal Fixed Voltage Reference (FVR)

Note 1: When selecting the VREF+ pin as the source of the positive reference, be aware that a minimum voltage specification exists. See **Section 26.0 “Electrical Specifications”** for details.

TABLE 15-3: SUMMARY OF REGISTERS ASSOCIATED WITH ADC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON0	—	CHS<4:0>					GO/$\overline{DONE}$	ADON	135
ADCON1	ADFM	ADCS<2:0>			—	—	ADPREF<1:0>		136
ADCON2	TRIGSEL<3:0>				—	—	—	—	137
ADRESH	ADC Result Register High								138, 139
ADRESL	ADC Result Register Low								138, 139
ANSELA	—	—	—	ANSA4	—	ANSA<2:0>			114
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	74
PIE1	TMR1GIE	ADIE	RCIE(2)	TXIE(2)	—	—	TMR2IE	TMR1IE	75
PIR1	TMR1GIF	ADIF	RCIF(2)	TXIF(2)	—	—	TMR2IF	TMR1IF	78
TRISA	—	—	TRISA5	TRISA4	—(1)	TRISA<2:0>			113
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		125

Legend: — = unimplemented, read as ‘0’. Shaded cells are not used for the ADC module.

Note 1: Unimplemented, read as ‘1’.

2: PIC12(L)F1572 only.

17.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparators are very useful mixed signal building blocks because they provide analog functionality independent of program execution. The analog comparator module includes the following features:

- Independent comparator control
- Programmable input selection
- Comparator output is available internally/externally
- Programmable output polarity
- Interrupt-On-Change
- Wake-up from Sleep
- Programmable speed/power optimization
- PWM shutdown
- Programmable and Fixed Voltage Reference

17.1 Comparator Overview

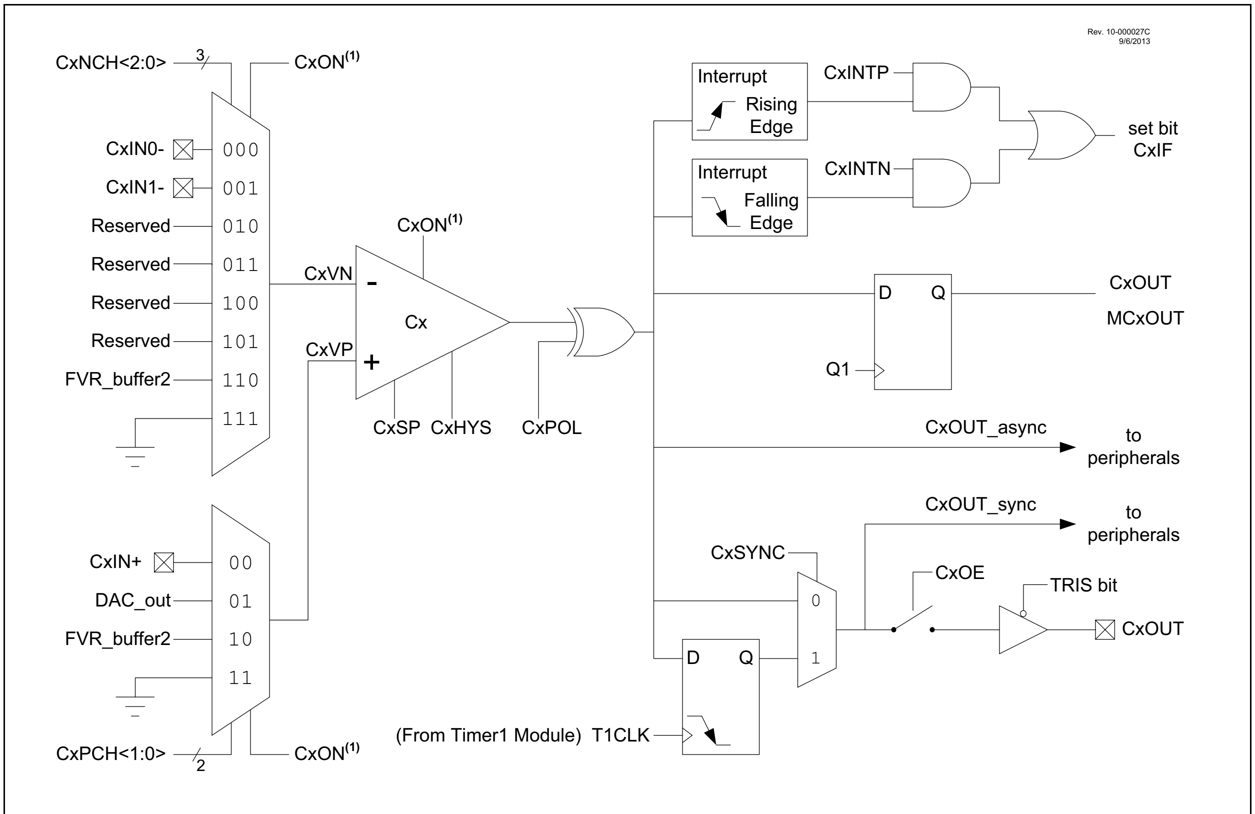
A single comparator is shown in Figure 17-2 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

The comparators available for this device are listed in Table 17-1.

TABLE 17-1: AVAILABLE COMPARATORS

Device	C1
PIC12(L)F1571	●
PIC12(L)F1572	●

FIGURE 17-1: COMPARATOR MODULE SIMPLIFIED BLOCK DIAGRAM



Note 1: When CxON = 0, all multiplexer inputs are disconnected and the Comparator will produce a '0' at the output.

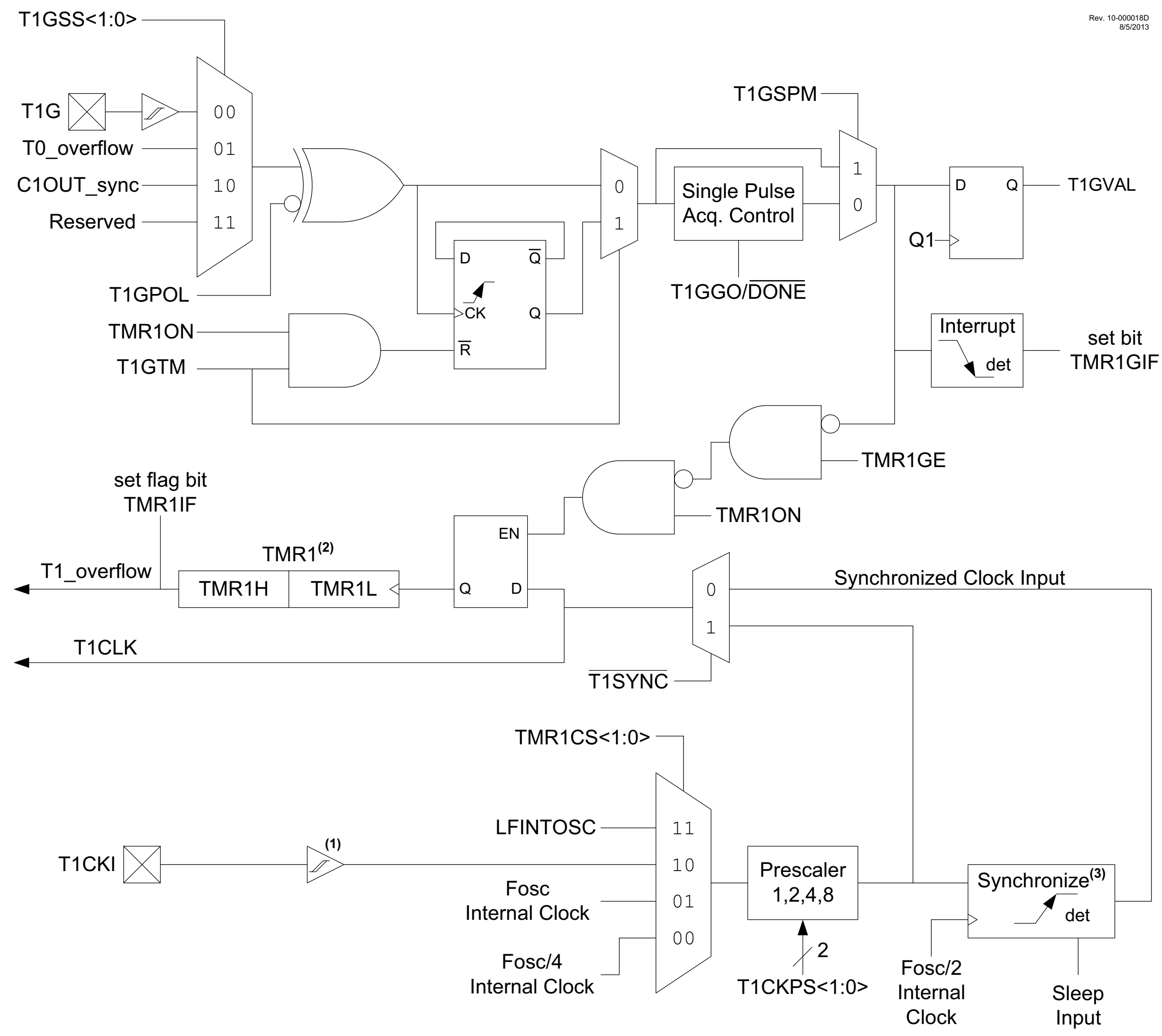
19.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module is a 16-bit timer/counter with the following features:

- 16-bit Timer/Counter register pair (TMR1H:TMR1L)
- Programmable internal or external clock source
- 2-bit prescaler
- Optionally synchronized comparator out
- Multiple Timer1 gate (count enable) sources
- Interrupt on overflow
- Wake-up on overflow (external clock, Asynchronous mode only)
- ADC auto-conversion trigger(s)
- Selectable gate source polarity
- Gate Toggle mode
- Gate Single-Pulse mode
- Gate value status
- Gate event interrupt

Figure 19-1 is a block diagram of the Timer1 module.

FIGURE 19-1: TIMER1 BLOCK DIAGRAM



Note 1: ST Buffer is high speed type when using T1CKI.
2: Timer1 register increments on rising edge.
3: Synchronize does not operate while in Sleep.

FIGURE 19-3: TIMER1 GATE ENABLE MODE

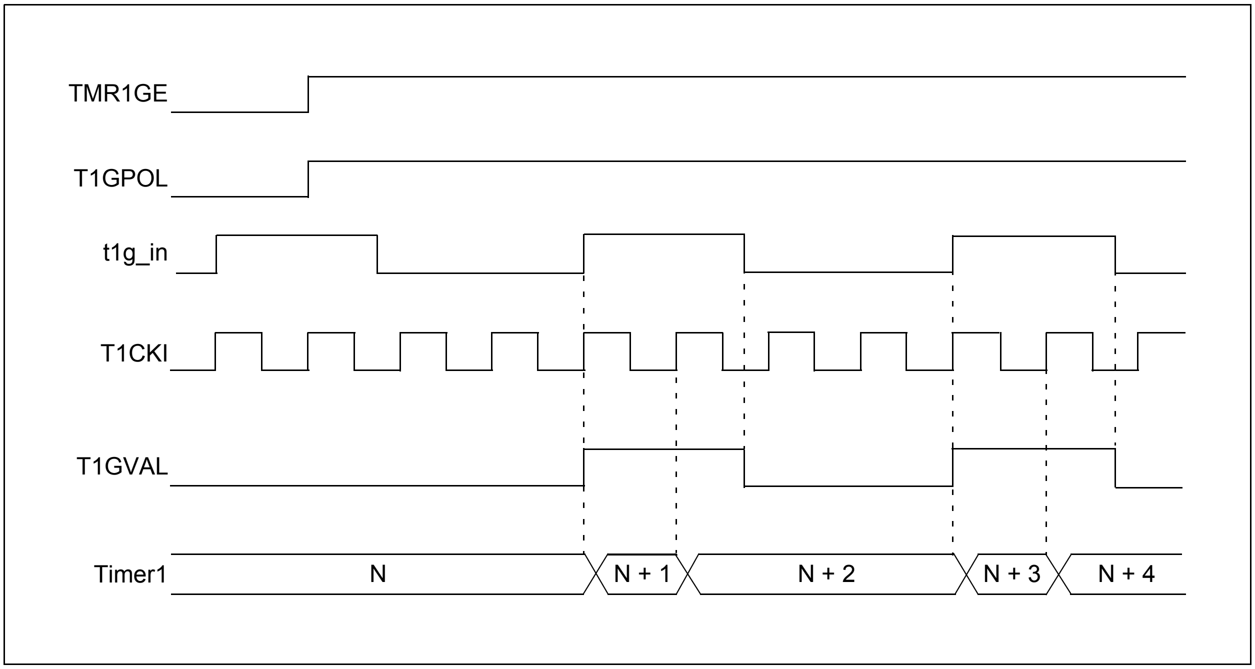
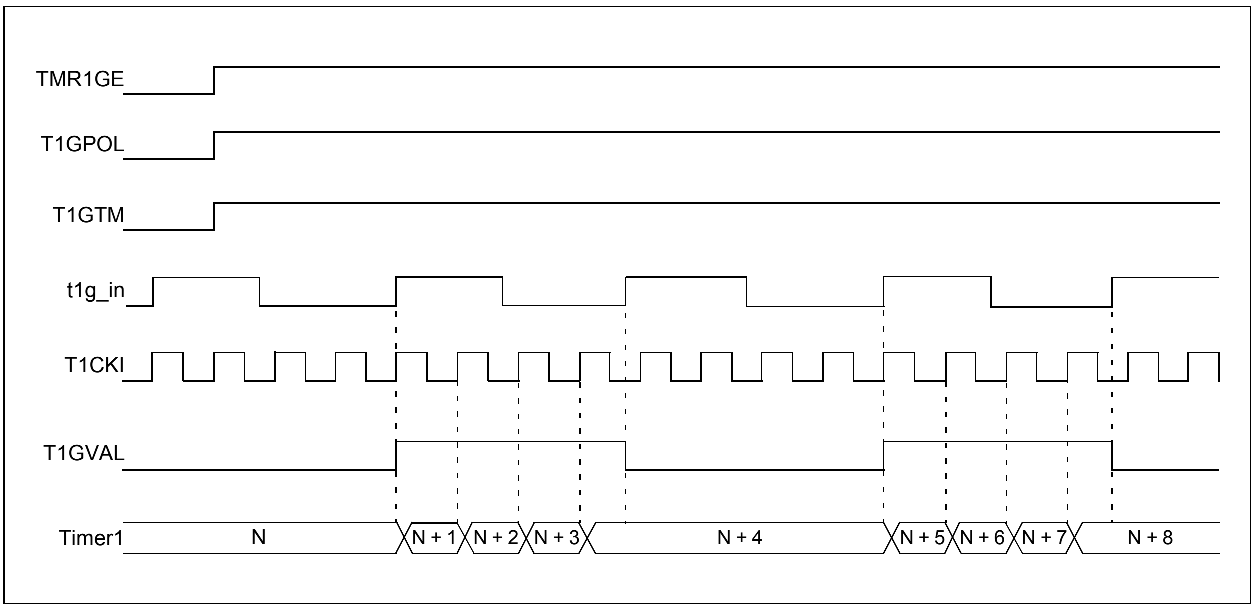


FIGURE 19-4: TIMER1 GATE TOGGLE MODE



21.3 Register Definitions: EUSART Control

REGISTER 21-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-1/1	R/W-0/0
CSRC	TX9	TXEN(1)	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **CSRC:** Clock Source Select bit
Asynchronous mode:
Don’t care.
Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

bit 6 **TX9:** 9-Bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5 **TXEN:** Transmit Enable bit(1)
1 = Transmit is enabled
0 = Transmit is disabled

bit 4 **SYNC:** EUSART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode

bit 3 **SENDB:** Send Break Character bit
Asynchronous mode:
1 = Sends Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission completed
Synchronous mode:
Don’t care.

bit 2 **BRGH:** High Baud Rate Select bit
Asynchronous mode:
1 = High speed
0 = Low speed
Synchronous mode:
Unused in this mode.

bit 1 **TRMT:** Transmit Shift Register Status bit
1 = TSR is empty
0 = TSR is full

bit 0 **TX9D:** Ninth bit of Transmit Data
Can be address/data bit or a parity bit.

Note 1: SREN/CREN overrides TXEN in Sync mode.

NOTES:

22.4 Reload Operation

Four of the PWM module control register pairs and one control bit are double-buffered so that all can be updated simultaneously. These include:

- PWMxPHH:PWMxPHL register pair
- PWMxDCH:PWMxDCL register pair
- PWMxPRH:PWMxPRL register pair
- PWMxOFH:PWMxOFL register pair
- OFO control bit

When written to, these registers do not immediately affect the operation of the PWM. By default, writes to these registers will not be loaded into the PWM Operating Buffer registers until after the arming conditions are met. The arming control has two methods of operation:

- Immediate
- Triggered

The LDT bit of the PWMxLDCON register controls the arming method. Both methods require the LDA bit to be set. All four buffer pairs will load simultaneously at the loading event.

22.4.1 IMMEDIATE RELOAD

When the LDT bit is clear, then the immediate mode is selected and the buffers will be loaded at the first period event after the LDA bit is set. Immediate reloading is used when a PWM module is operating stand-alone or when the PWM module is operating as a master to other slave PWM modules.

22.4.2 TRIGGERED RELOAD

When the LDT bit is set, then the Triggered mode is selected and a trigger event is required for the LDA bit to take effect. The trigger source is the buffer load event of one of the other PWM modules in the device. The triggering source is selected by the LDS<1:0> bits of the PWMxLDCON register. The buffers will be loaded at the first period event following the trigger event. Triggered reloading is used when a PWM module is operating as a slave to another PWM and it is necessary to synchronize the buffer reloads in both modules.

Note 1:	The buffer load operation clears the LDA bit.
2:	If the LDA bit is set at the same time as PWMxTMR = PWMxPR, the LDA bit is ignored until the next period event. Such is the case when triggered reload is selected and the triggering event occurs simultaneously with the target's period event.

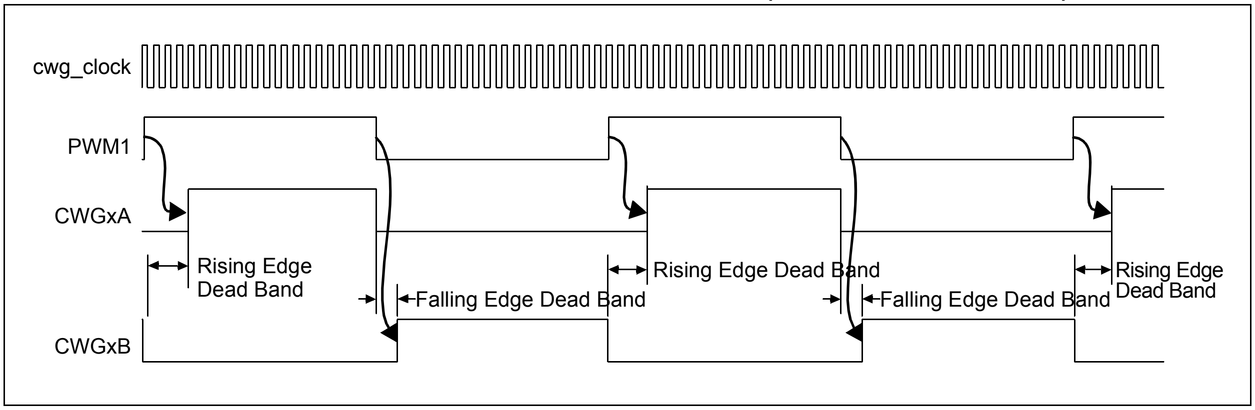
22.5 Operation in Sleep Mode

Each PWM module will continue to operate in Sleep mode when either the HFINTOSC or LFINTOSC is selected as the clock source by PWMxCLKCON<1:0>.

22.6 Interrupts

Each PWM module has four independent interrupts based on the phase, duty cycle, period and offset match events. The interrupt flag is set on the rising edge of each of these signals. Refer to Figures 22-12 and 22-13 for detailed timing diagrams of the match signals.

FIGURE 23-2: TYPICAL CWG OPERATION WITH PWM1 (NO AUTO-SHUTDOWN)



23.5 Dead-Band Control

Dead-band control provides for non-overlapping output signals to prevent shoot-through current in power switches. The CWG contains two 6-bit dead-band counters. One dead-band counter is used for the rising edge of the input source control. The other is used for the falling edge of the input source control.

Dead band is timed by counting CWG clock periods from zero, up to the value in the rising or falling Dead-Band Counter registers. See the CWGxDBR and CWGxDBF registers (Register 23-4 and Register 23-5, respectively).

23.6 Rising Edge Dead Band

The rising edge dead band delays the turn-on of the CWGxA output from when the CWGxB output is turned off. The rising edge dead-band time starts when the rising edge of the input source signal goes true. When this happens, the CWGxB output is immediately turned off and the rising edge dead-band delay time starts. When the rising edge dead-band delay time is reached, the CWGxA output is turned on.

The CWGxDBR register sets the duration of the dead-band interval on the rising edge of the input source signal. This duration is from 0 to 64 counts of dead band.

Dead band is always counted off the edge on the input source signal. A count of 0 (zero), indicates that no dead band is present.

If the input source signal is not present for enough time for the count to be completed, no output will be seen on the respective output.

23.7 Falling Edge Dead Band

The falling edge dead band delays the turn-on of the CWGxB output from when the CWGxA output is turned off. The falling edge dead-band time starts when the falling edge of the input source goes true. When this happens, the CWGxA output is immediately turned off and the falling edge dead-band delay time starts. When the falling edge dead-band delay time is reached, the CWGxB output is turned on.

The CWGxDBF register sets the duration of the dead-band interval on the falling edge of the input source signal. This duration is from 0 to 64 counts of dead band.

Dead band is always counted off the edge on the input source signal. A count of 0 (zero), indicates that no dead band is present.

If the input source signal is not present for enough time for the count to be completed, no output will be seen on the respective output.

Refer to Figure 23-3 and Figure 23-4 for examples.

23.8 Dead-Band Uncertainty

When the rising and falling edges of the input source triggers the dead-band counters, the input may be asynchronous. This will create some uncertainty in the dead-band time delay. The maximum uncertainty is equal to one CWG clock period. Refer to Equation 23-1 for more detail.

EQUATION 23-1: DEAD-BAND UNCERTAINTY

$$T_{DEADBAND\_UNCERTAINTY} = \frac{1}{Fcwg\_clock}$$

Example:

$$Fcwg\_clock = 16\ MHz$$

Therefore:

$$T_{DEADBAND\_UNCERTAINTY} = \frac{1}{Fcwg\_clock}$$

$$= \frac{1}{16\ MHz}$$

$$= 62.5ns$$

23.9 Auto-Shutdown Control

Auto-shutdown is a method to immediately override the CWG output levels with specific overrides that allow for safe shutdown of the circuit. The shutdown state can be either cleared automatically or held until cleared by software.

23.9.1 SHUTDOWN

The shutdown state can be entered by either of the following two methods:

- Software generated
- External Input

23.9.1.1 Software Generated Shutdown

Setting the GxASE bit of the CWGxCON2 register will force the CWG into the shutdown state.

When auto-restart is disabled, the shutdown state will persist as long as the GxASE bit is set.

When auto-restart is enabled, the GxASE bit will clear automatically and resume operation on the next rising edge event. See Figure 23-6.

23.9.1.2 External Input Source

External shutdown inputs provide the fastest way to safely suspend CWG operation in the event of a Fault condition. When any of the selected shutdown inputs goes active, the CWG outputs will immediately go to the selected override levels without software delay. Any combination of two input sources can be selected to cause a shutdown condition. The sources are:

- Comparator C1 – C1OUT_async
- $\overline{\text{CWG1FLT}}$

Shutdown inputs are selected in the CWGxCON2 register (Register 23-3).

Note:	Shutdown inputs are level sensitive, not edge sensitive. The shutdown state cannot be cleared, except by disabling auto-shutdown, as long as the shutdown input level persists.

26.3 DC Characteristics

TABLE 26-1: SUPPLY VOLTAGE

PIC12LF1571/2			Standard Operating Conditions (unless otherwise stated)				
PIC12F1571/2							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**					
			VDDMIN 1.8 2.5	 — —	VDDMAX 3.6 3.6	 V V	 FOSC ≤ 16 MHz FOSC ≤ 32 MHz **(Note 3)**
D001			2.3 2.5	— —	5.5 5.5	V V	FOSC ≤ 16 MHz FOSC ≤ 32 MHz **(Note 3)**
D002*	VDR	**RAM Data Retention Voltage(1)**					
			1.5	—	—	V	Device in Sleep mode
D002*			1.7	—	—	V	Device in Sleep mode
D002A*	VPOR	**Power-on Reset Release Voltage(2)**					
			—	1.6	—	V	
D002A*			—	1.6	—	V	
D002B*	VPORR*	**Power-on Reset Rearm Voltage(2)**					
			—	0.8	—	V	
D002B*			—	1.5	—	V	
D003	VFVR	**Fixed Voltage Reference Voltage**	—	1.024	—	V	-40°C ≤ TA ≤ +85°C
D003A	VADFVR	**FVR Gain Voltage Accuracy for ADC**	-4	—	+4	%	1x VFVR, ADFVR = 01, VDD ≥ 2.5V 2x VFVR, ADFVR = 10, VDD ≥ 2.5V 4x VFVR, ADFVR = 11, VDD ≥ 4.75V
D003B	VCDAFVR	**FVR Gain Voltage Accuracy for Comparator**	-4	—	+4	%	1x VFVR, CDAFVR = 01, VDD ≥ 2.5V 2x VFVR, CDAFVR = 10, VDD ≥ 2.5V 4x VFVR, CDAFVR = 11, VDD ≥ 4.75V
D004*	SVDD	**VDD Rise Rate(2)**	0.05	—	—	V/ms	Ensures that the Power-on Reset signal is released properly

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: See Figure 26-3, POR and POR Rearm with Slow Rising VDD.

3: PLL required for 32 MHz operation.

FIGURE 27-27: IPD, BROWN-OUT RESET (BOR), BORV = 1, PIC12LF1571/2 ONLY

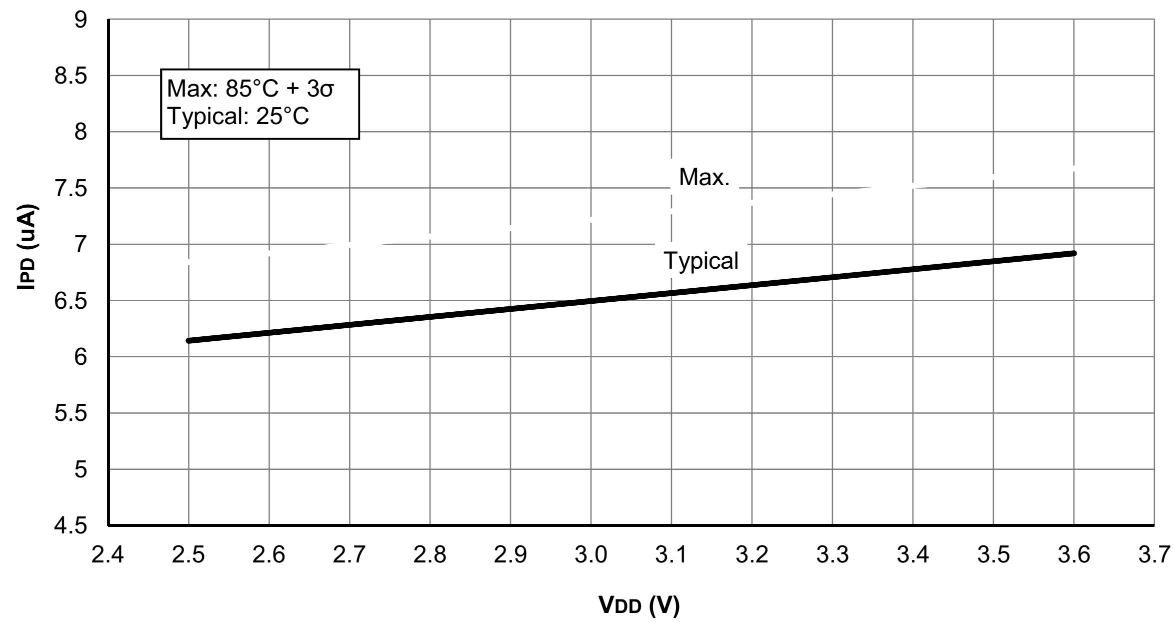


FIGURE 27-28: IPD, BROWN-OUT RESET (BOR), BORV = 1, PIC12F1571/2 ONLY