What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	LINbus, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	6
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 4x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12lf1572-i-mf

3.3.6 CORE FUNCTION REGISTERS SUMMARY

The Core Function registers listed in Table 3-9 can be addressed from any bank.

TABLE 3-9: CORE FUNCTION REGISTERS SUMMARY

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on All Other Resets
Bank 0-31											
x00h or x80h	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
x01h or x81h	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
x02h or x82h	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
x03h or x83h	STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
x04h or x84h	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
x05h or x85h	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
x06h or x86h	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
x07h or x87h	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
x08h or x88h	BSR	—	—	—	BSR<4:0>					---0 0000	---0 0000
x09h or x89h	WREG	Working Register								0000 0000	uuuu uuuu
x0Ah or x8Ah	PCLATH	—	Write Buffer for the Upper 7 bits of the Program Counter							-000 0000	-000 0000
x0Bh or x8Bh	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000

Legend: x = unknown; u = unchanged; q = value depends on condition; — = unimplemented, read as '0'; r = reserved.
Shaded locations are unimplemented, read as '0'.

5.0   OSCILLATOR MODULE

5.1   Overview

The oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications, while maximizing performance and minimizing power consumption. Figure 5-1 illustrates a block diagram of the oscillator module.

Clock sources can be supplied from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system clock source can be supplied from one of two internal oscillators and PLL circuits, with a choice of speeds selectable via software. Additional clock features include:

• Selectable system clock source between external or internal sources via software
• Oscillator Start-up Timer (OST) ensures stability of crystal oscillator sources

The oscillator module can be configured in one of the following clock modes:

1. ECL – External Clock Low-Power mode (0 MHz to 0.5 MHz)
2. ECM – External Clock Medium Power mode (0.5 MHz to 4 MHz)
3. ECH – External Clock High-Power mode (4 MHz to 32 MHz)
4. INTOSC – Internal Oscillator (31 kHz to 32 MHz)

Clock Source modes are selected by the FOSC<1:0> bits in the Configuration Words. The FOSC bits determine the type of oscillator that will be used when the device is first powered.

The ECH, ECM, and ECL Clock modes rely on an external logic level signal as the device clock source.

The INTOSC internal oscillator block produces low, medium and high-frequency clock sources, designated as LFINTOSC, MFINTOSC and HFINTOSC (see Internal Oscillator Block, Figure 5-1). A wide selection of device clock frequencies may be derived from these three clock sources.

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TABLE 9-3: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	SPLLEN	IRCF<3:0>				—	SCS<1:0>		55
PCON	STKOVF	STKUNF	—	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	66
STATUS	—	—	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	19
WDTCON	—	—	WDTPS<4:0>					SWDTEN	89

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by the Watchdog Timer.

TABLE 9-4: SUMMARY OF CONFIGURATION WORD WITH WATCHDOG TIMER

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	—	—	$\overline{\text{CLKOUTEN}}$	BOREN<1:0>		—	42
	7:0	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE<1:0>		—	FOSC<1:0>		

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by the Watchdog Timer.

REGISTER 11-4: LATA: PORTA DATA LATCH REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	U-0	R/W-x/u	R/W-x/u	R/W-x/u
—	—	LATA<5:4>[1]		—	LATA<2:0>[1]		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-6   **Unimplemented:** Read as '0'

bit 5-4   **LATA<5:4>**: RA<5:4> Output Latch Value bits[1]

bit 3   **Unimplemented:** Read as '0'

bit 2-0   **LATA<2:0>**: RA<2:0> Output Latch Value bits[1]

Note 1: Writes to PORTA are actually written to corresponding LATA register. Reads from the PORTA register are the return of actual I/O pin values.

REGISTER 11-5: ANSELA: PORTA ANALOG SELECT REGISTER

U-0	U-0	U-0	R/W-1/1	U-0	R/W-1/1	R/W-1/1	R/W-1/1
—	—	—	ANSA4	—	ANSA<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-5   **Unimplemented:** Read as '0'

bit 4   **ANSA4**: Analog Select Between Analog or Digital Function on RA4 Pins (respectively) bit

         1 = Analog input; pin is assigned as analog input, digital input buffer is disabled[1]
         0 = Digital I/O; pin is assigned to port or digital special function

bit 3   **Unimplemented:** Read as '0'

bit 2-0   **ANSA<2:0>**: Analog Select Between Analog or Digital Function on RA<2:0> pins (respectively) bits

         1 = Analog input; pin is assigned as analog input, digital input buffer is disabled[1]
         0 = Digital I/O; pin is assigned to port or digital special function

Note 1: When setting a pin to an analog input, the corresponding TRISx bit must be set to Input mode in order to allow external control of the voltage on the pin.

13.0 FIXED VOLTAGE REFERENCE (FVR)

The Fixed Voltage Reference (FVR) is a stable voltage reference, independent of V_{DD}, with a nominal output level (V_{FVR}) of 1.024V. The output of the FVR can be configured to supply a reference voltage to the following:

• ADC input channel
• Comparator positive input
• Comparator negative input

The FVR can be enabled by setting the FVREN bit of the FVRCON register.

13.1 Independent Gain Amplifier

The output of the FVR supplied to the peripherals, (listed above), is routed through a programmable gain amplifier. Each amplifier can be programmed for a gain of 1x, 2x or 4x, to produce the three possible voltage levels.

The ADFVR<1:0> bits of the FVRCON register are used to enable and configure the gain amplifier settings for the reference supplied to the ADC module. Reference **Section 15.0 "Analog-to-Digital Converter (ADC) Module"** for additional information.

The CDAFVR<1:0> bits of the FVRCON register are used to enable and configure the gain amplifier settings for the reference supplied to the comparator modules. Reference **Section 17.0 "Comparator Module"** for additional information.
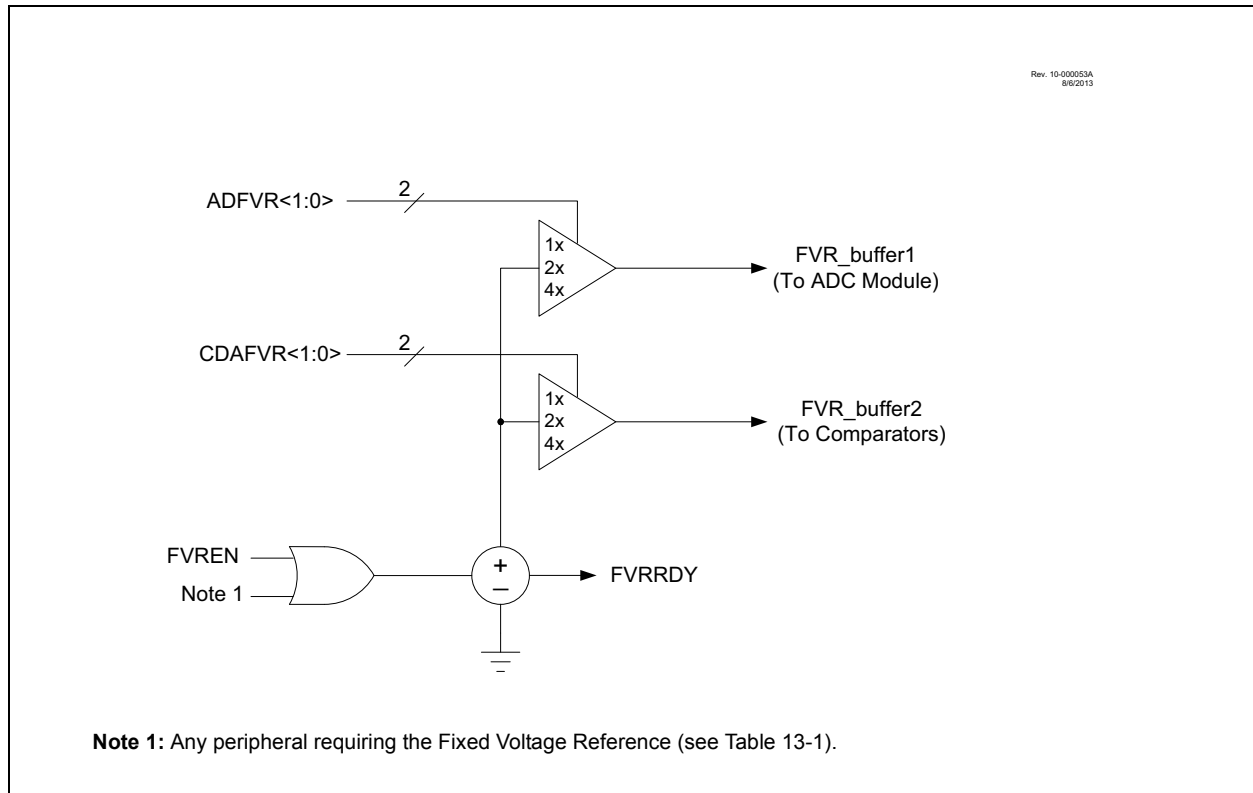
To minimize current consumption when the FVR is disabled, the FVR buffers should be turned off by clearing the Buffer Gain Selection bits.

13.2 FVR Stabilization Period

The FVR can be enabled by setting the FVREN bit of the FVRCON register.

When the Fixed Voltage Reference module is enabled, it requires time for the reference and amplifier circuits to stabilize. Once the circuits stabilize and are ready for use, the FVRRDY bit of the FVRCON register will be set. See the FVR Stabilization Period characterization graph, Figure 27-21.

FIGURE 13-1: VOLTAGE REFERENCE BLOCK DIAGRAM

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ADFVR<1:0> — 2

1x 2x 4x → FVR_buffer1 (To ADC Module)

CDAFVR<1:0> — 2

1x 2x 4x → FVR_buffer2 (To Comparators)

FVREN
Note 1
+ − → FVRRDY

Note 1: Any peripheral requiring the Fixed Voltage Reference (see Table 13-1).

TABLE 13-1: PERIPHERALS REQUIRING THE FIXED VOLTAGE REFERENCE (FVR)

Peripheral	Conditions	Description
HFINTOSC	FOSC<2:0> = `010` and IRCF<3:0> = `000x`	INTOSC is active and device is not in Sleep.
BOR	BOREN<1:0> = `11`	BOR is always enabled.
	BOREN<1:0> = `10` and BORFS = `1`	BOR is disabled in Sleep mode, BOR Fast Start is enabled.
	BOREN<1:0> = `01` and BORFS = `1`	BOR under software control, BOR Fast Start is enabled.
LDO	All PIC12F1571/2 devices, when VREGPM = `1` and not in Sleep	The device runs off of the Low-Power Regulator when in Sleep mode.

14.0 TEMPERATURE INDICATOR MODULE

This family of devices is equipped with a temperature circuit designed to measure the operating temperature of the silicon die. The circuit's range of operating temperature falls between -40°C and +85°C. The output is a voltage that is proportional to the device temperature. The output of the temperature indicator is internally connected to the device ADC.

The circuit may be used as a temperature threshold detector or a more accurate temperature indicator, depending on the level of calibration performed. A one-point calibration allows the circuit to indicate a temperature closely surrounding that point. A two-point calibration allows the circuit to sense the entire range of temperature more accurately. Reference Application Note AN1333, "*Use and Calibration of the Internal Temperature Indicator*" (DS00001333) for more details regarding the calibration process.

14.1 Circuit Operation

Figure 14-1 shows a simplified block diagram of the temperature circuit. The proportional voltage output is achieved by measuring the forward voltage drop across multiple silicon junctions.

Equation 14-1 describes the output characteristics of the temperature indicator.

EQUATION 14-1: V_{OUT} RANGES

$$\text{High Range: } V_{OUT} = V_{DD} - 4\ V_T$$

$$\text{Low Range: } V_{OUT} = V_{DD} - 2\ V_T$$

The temperature sense circuit is integrated with the Fixed Voltage Reference (FVR) module. See **Section 13.0 "Fixed Voltage Reference (FVR)"** for more information.

The circuit is enabled by setting the TSEN bit of the FVRCON register. When disabled, the circuit draws no current.

The circuit operates in either high or low range. The high range, selected by setting the TSRNG bit of the FVRCON register, provides a wider output voltage. This provides more resolution over the temperature range, but may be less consistent from part to part. This range requires a higher bias voltage to operate and thus, a higher V_{DD} is needed.

The low range is selected by clearing the TSRNG bit of the FVRCON register. The low range generates a lower voltage drop and thus, a lower bias voltage is needed to operate the circuit. The low range is provided for low-voltage operation.

FIGURE 14-1: TEMPERATURE CIRCUIT DIAGRAM
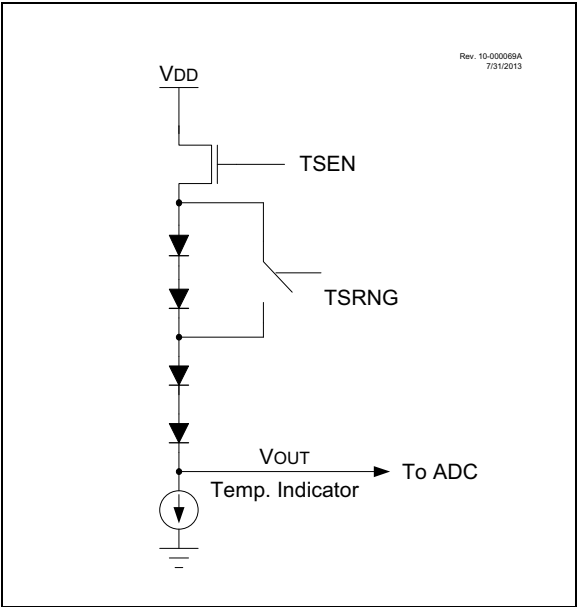
14.2 Minimum Operating V_{DD}

When the temperature circuit is operated in low range, the device may be operated at any operating voltage that is within specifications.

When the temperature circuit is operated in high range, the device operating voltage, V_{DD}, must be high enough to ensure that the temperature circuit is correctly biased.

Table 14-1 shows the recommended minimum V_{DD} vs. range setting.

TABLE 14-1: RECOMMENDED V_{DD} VS. RANGE

Min. V_{DD}, TSRNG = 1	Min. V_{DD}, TSRNG = 0
3.6V	1.8V

14.3 Temperature Output

The output of the circuit is measured using the internal Analog-to-Digital Converter. A channel is reserved for the temperature circuit output. Refer to **Section 15.0 "Analog-to-Digital Converter (ADC) Module"** for detailed information.

14.4 ADC Acquisition Time

To ensure accurate temperature measurements, the user must wait at least 200 µs after the ADC input multiplexer is connected to the temperature indicator output before the conversion is performed. In addition, the user must wait 200 µs between sequential conversions of the temperature indicator output.

20.1 Timer2 Operation

The clock input to the Timer2 module is the system instruction clock (F$_{OSC}$/4).

TMR2 increments from 00h on each clock edge.

A 4-bit counter/prescaler on the clock input allows direct input, divide-by-4 and divide-by-16 prescale options. These options are selected by the prescaler control bits, T2CKPS<1:0> of the T2CON register. The value of TMR2 is compared to that of the Period register, PR2, on each clock cycle. When the two values match, the comparator generates a match signal as the timer output. This signal also resets the value of TMR2 to 00h on the next cycle and drives the output counter/postscaler (see **Section 20.2 "Timer2 Interrupt"**).

The TMR2 and PR2 registers are both directly readable and writable. The TMR2 register is cleared on any device Reset, whereas the PR2 register initializes to FFh. Both the prescaler and postscaler counters are cleared on the following events:

• A write to the TMR2 register
• A write to the T2CON register
• Power-on Reset (POR)
• Brown-out Reset (BOR)
• MCLR Reset
• Watchdog Timer (WDT) Reset
• Stack Overflow Reset
• Stack Underflow Reset
• RESET Instruction

> **Note:** TMR2 is not cleared when T2CON is written.

20.2 Timer2 Interrupt

Timer2 can also generate an optional device interrupt. The Timer2 output signal (T2_match) provides the input for the 4-bit counter/postscaler. This counter generates the TMR2 match interrupt flag which is latched in TMR2IF of the PIR1 register. The interrupt is enabled by setting the TMR2 Match Interrupt Enable bit, TMR2IE of the PIE1 register.

A range of 16 postscale options (from 1:1 through 1:16 inclusive) can be selected with the postscaler control bits, T2OUTPS<3:0>, of the T2CON register.

20.3 Timer2 Output

The output of TMR2 is T2_match.

The T2_match signal is synchronous with the system clock. Figure 20-3 shows two examples of the timing of the T2_match signal relative to F$_{OSC}$ and prescale value, T2CKPS<1:0>. The upper diagram illustrates 1:1 prescale timing and the lower diagram, 1:X prescale timing.

FIGURE 20-3: T2_MATCH TIMING DIAGRAM
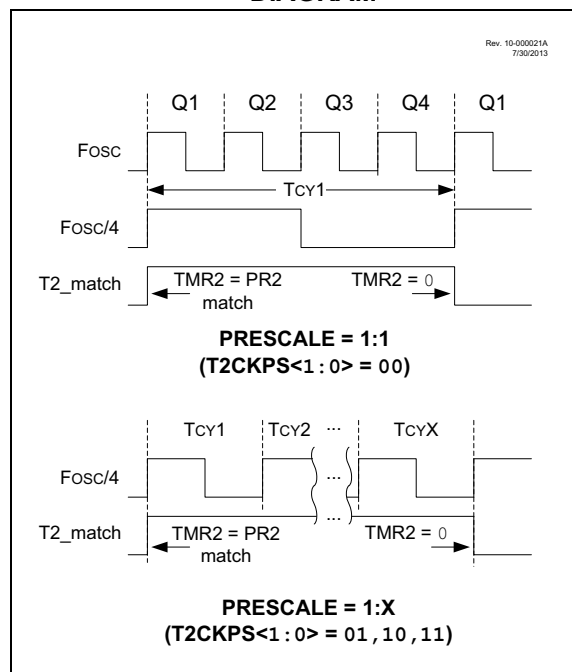
20.4 Timer2 Operation During Sleep

Timer2 cannot be operated while the processor is in Sleep mode. The contents of the TMR2 and PR2 registers will remain unchanged while the processor is in Sleep mode.

21.5.1.5   Synchronous Master Reception

Data is received at the RX/DT pin. The RX/DT pin output driver is automatically disabled when the EUSART is configured for synchronous master receive operation.

In Synchronous mode, reception is enabled by setting either the Single Receive Enable bit (SREN of the RCSTA register) or the Continuous Receive Enable bit (CREN of the RCSTA register).

When SREN is set and CREN is clear, only as many clock cycles are generated as there are data bits in a single character. The SREN bit is automatically cleared at the completion of one character. When CREN is set, clocks are continuously generated until CREN is cleared. If CREN is cleared in the middle of a character, the CK clock stops immediately and the partial character is discarded. If SREN and CREN are both set, then SREN is cleared at the completion of the first character and CREN takes precedence.

To initiate reception, set either SREN or CREN. Data is sampled at the RX/DT pin on the trailing edge of the TX/CK clock pin and is shifted into the Receive Shift Register (RSR). When a complete character is received into the RSR, the RCIF bit is set and the character is automatically transferred to the two-character receive FIFO. The Least Significant eight bits of the top character in the receive FIFO are available in RCREG. The RCIF bit remains set as long as there are unread characters in the receive FIFO.

> **Note:**   If the RX/DT function is on an analog pin, the corresponding ANSELx bit must be cleared for the receiver to function.

21.5.1.6   Slave Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a slave receives the clock on the TX/CK line. The TX/CK pin output driver is automatically disabled when the device is configured for synchronous slave transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One data bit is transferred for each clock cycle. Only as many clock cycles should be received as there are data bits.

> **Note:**   If the device is configured as a slave and the TX/CK function is on an analog pin, the corresponding ANSELx bit must be cleared.

21.5.1.7   Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before RCREG is read to access the FIFO. When this happens, the OERR bit of the RCSTA register is set. Previous data in the FIFO will not be overwritten. The two characters in the FIFO buffer can be read, however, no additional characters will be received until the error is cleared. The OERR bit can only be cleared by clearing the overrun condition. If the overrun error occurred when the SREN bit is set and CREN is clear, then the error is cleared by reading RCREG. If the overrun occurred when the CREN bit is set, then the error condition is cleared by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.
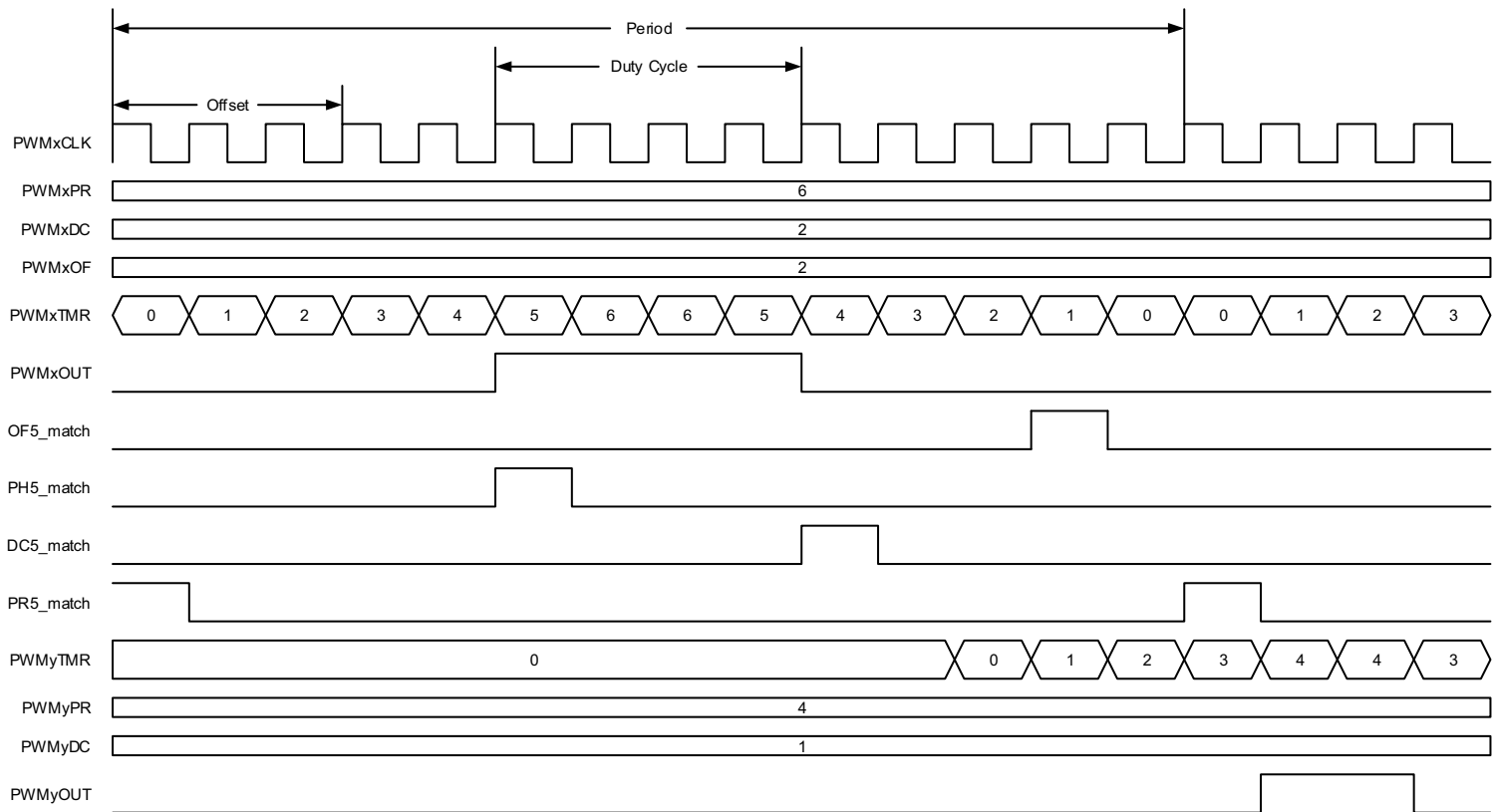
21.5.1.8   Receiving 9-Bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set the EUSART will shift 9 bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth, and Most Significant, data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREG.

21.5.1.9   Synchronous Master Reception Setup

1. Initialize the SPBRGH/SPBRGL register pair for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
2. Clear the ANSELx bit for the RX pin (if applicable).
3. Enable the synchronous master serial port by setting bits, SYNC, SPEN and CSRC.
4. Ensure bits, CREN and SREN, are clear.
5. If interrupts are desired, set the RCIE bit of the PIE1 register, and the GIE and PEIE bits of the INTCON register.
6. If 9-bit reception is desired, set bit, RX9.
7. Start reception by setting the SREN bit or for continuous reception, set the CREN bit.
8. Interrupt flag bit, RCIF, will be set when reception of a character is complete. An interrupt will be generated if the enable bit, RCIE, was set.
9. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
10. Read the 8-bit received data by reading the RCREG register.
11. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

FIGURE 22-13: **OFFSET MATCH ON DECREMENTING TIMER TIMING DIAGRAM**

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7/9/2015

Period

Duty Cycle

Offset

PWMxCLK

PWMxPR   6

PWMxDC   2

PWMxOF   2

PWMxTMR   0 1 2 3 4 5 6 6 5 4 3 2 1 0 0 1 2 3

PWMxOUT

OF5_match

PH5_match

DC5_match

PR5_match

PWMyTMR   0   0 1 2 3 4 4 3

PWMyPR   4

PWMyDC   1

PWMyOUT

Note: Master = PWMx, Slave = PWMy

REGISTER 22-9: PWMxDCH: PWMx DUTY CYCLE COUNT HIGH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
DC<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-0 **DC<15:8>**: PWMx Duty Cycle High bits
Upper eight bits of PWM duty cycle count.

REGISTER 22-10: PWMxDCL: PWMx DUTY CYCLE COUNT LOW REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
DC<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-0 **DC<7:0>**: PWMx Duty Cycle Low bits
Lower eight bits of PWM duty cycle count.

TABLE 22-2: **SUMMARY OF REGISTERS ASSOCIATED WITH PWM**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	SPLLEN	IRCF<3:0>				—	SCS<1:0>		55
PIE3	—	PWM3IE	PWM2IE	PWM1IE	—	—	—	—	77
PIR3	—	PWM3IF	PWM2IF	PWM1IF	—	—	—	—	80
PWMEN	—	—	—	—	—	PWM3EN_A	PWM2EN_A	PWM1EN_A	227
PWMLD	—	—	—	—	—	PWM3LDA_A	PWM2LDA_A	PWM1LDA_A	227
PWMOUT	—	—	—	—	—	PWM3OUT_A	PWM2OUT_A	PWM1OUT_A	227
PWM1PHL	PH<7:0>								222
PWM1PHH	PH<15:8>								222
PWM1DCL	DC<7:0>								223
PWM1DCH	DC<15:8>								223
PWM1PRH	PR<7:0>								224
PWM1PRL	PR<15:8>								224
PWM1OFH	OF<7:0>								225
PWM1OFL	OF<15:8>								225
PWM1TMRH	TMR<7:0>								226
PWM1TMRL	TMR<15:8>								226
PWM1CON	EN	OE	OUT	POL	MODE<1:0>		—	—	216
PWM1INTE	—	—	—	—	OFIE	PHIE	DCIE	PRIE	217
PWM1INTF	—	—	—	—	OFIF	PHIF	DCIF	PRIF	218
PWM1CLKCON	—	PS<2:0>			—	—	CS<1:0>		219
PWM1LDCON	LDA	LDT	—	—	—	—	LDS<1:0>		220
PWM1OFCON	—	OFM<1:0>		OFO	—	—	OFS<1:0>		221
PWM2PHL	PH<7:0>								222
PWM2PHH	PH<15:8>								222
PWM2DCL	DC<7:0>								223
PWM2DCH	DC<15:8>								223
PWM2PRL	PR<7:0>								224
PWM2PRH	PR<15:8>								224
PWM2OFL	OF<7:0>								225
PWM2OFH	OF<15:8>								225
PWM2TMRL	TMR<7:0>								226
PWM2TMRH	TMR<15:8>								226
PWM2CON	EN	OE	OUT	POL	MODE<1:0>		—	—	216
PWM2INTE	—	—	—	—	OFIE	PHIE	DCIE	PRIE	217
PWM2INTF	—	—	—	—	OFIF	PHIF	DCIF	PRIF	218
PWM2CLKCON	—	PS<2:0>			—	—	CS<1:0>		219
PWM2LDCON	LDA	LDT	—	—	—	—	LDS<1:0>		220
PWM2OFCON	—	OFM<1:0>		OFO	—	—	OFS<1:0>		221
PWM3PHL	PH<7:0>								222
PWM3PHH	PH<15:8>								222
PWM3DCL	DC<7:0>								223
PWM3DCH	DC<15:8>								223
PWM3PRL	PR<7:0>								224
PWM3PRH	PR<15:8>								224
PWM3OFL	OF<7:0>								225
PWM3OFH	OF<15:8>								225
PWM3TMRL	TMR<7:0>								226
PWM3TMRH	TMR<15:8>								226
PWM3CON	EN	OE	OUT	POL	MODE<1:0>		—	—	216

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by the PWM.

26.4 AC Characteristics

Timing Parameter Symbology has been created with one of the following formats:

1. TppS2ppS
2. TppS

| T				
F	Frequency		T	Time

Lowercase letters (pp) and their meanings:

pp				
cc	CCP1		osc	CLKIN
ck	CLKOUT		rd	$\overline{RD}$
cs	$\overline{CS}$		rw	$\overline{RD}$ or $\overline{WR}$
di	SDIx		sc	SCKx
do	SDO		ss	$\overline{SS}$
dt	Data in		t0	T0CKI
io	I/O PORT		t1	T1CKI
mc	$\overline{MCLR}$		wr	$\overline{WR}$

Uppercase letters and their meanings:

S				
F	Fall		P	Period
H	High		R	Rise
I	Invalid (High-impedance)		V	Valid
L	Low		Z	High-impedance

FIGURE 26-4:   LOAD CONDITIONS

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8/1/2013

Load Condition

Pin

CL

VSS

Legend: CL=50 pF for all pins
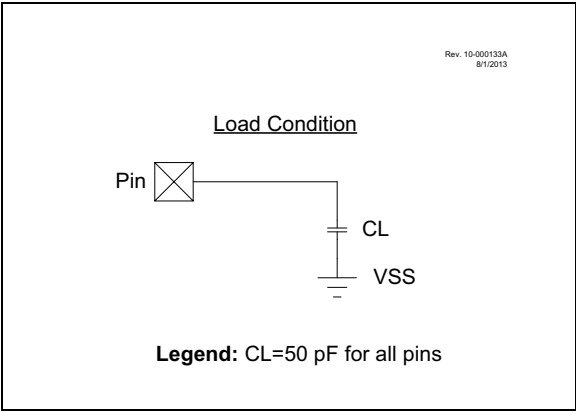
FIGURE 26-5: **CLOCK TIMING**

Note 1: See Table 26-10.
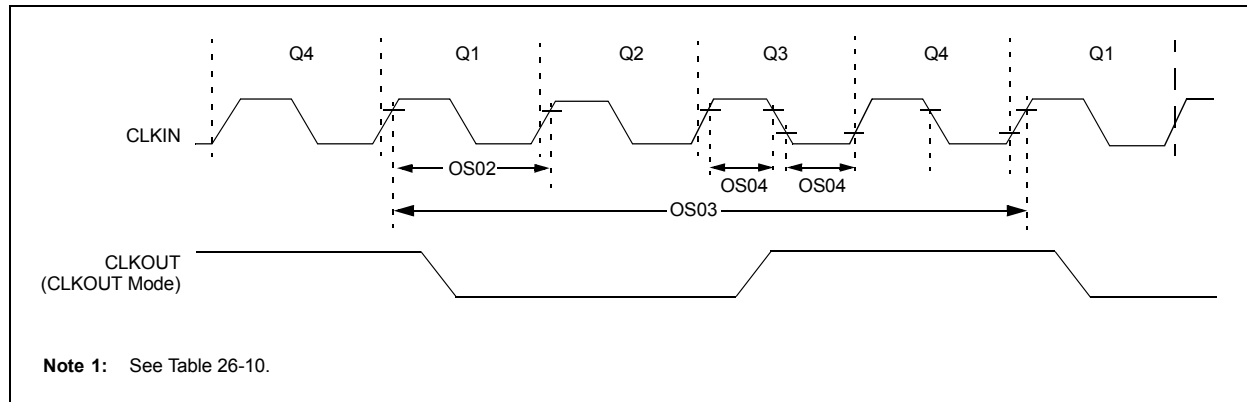
TABLE 26-7: **CLOCK OSCILLATOR TIMING REQUIREMENTS**

Standard Operating Conditions (unless otherwise stated)

Param. No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
OS01	F_{OSC}	External CLKIN Frequency[1]	DC	—	0.5	MHz	External Clock (ECL)
			DC	—	4	MHz	External Clock (ECM)
			DC	—	20	MHz	External Clock (ECH)
OS02	T_{OSC}	External CLKIN Period[1]	50	—	∞	ns	External Clock (EC)
OS03	T_{CY}	Instruction Cycle Time[1]	200	T_{CY}	DC	ns	T_{CY} = 4/F_{OSC}

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (T_{CY}) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the CLKIN pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

FIGURE 27-7: IDD TYPICAL, EC OSCILLATOR, MEDIUM POWER MODE, PIC12F1571/2 ONLY
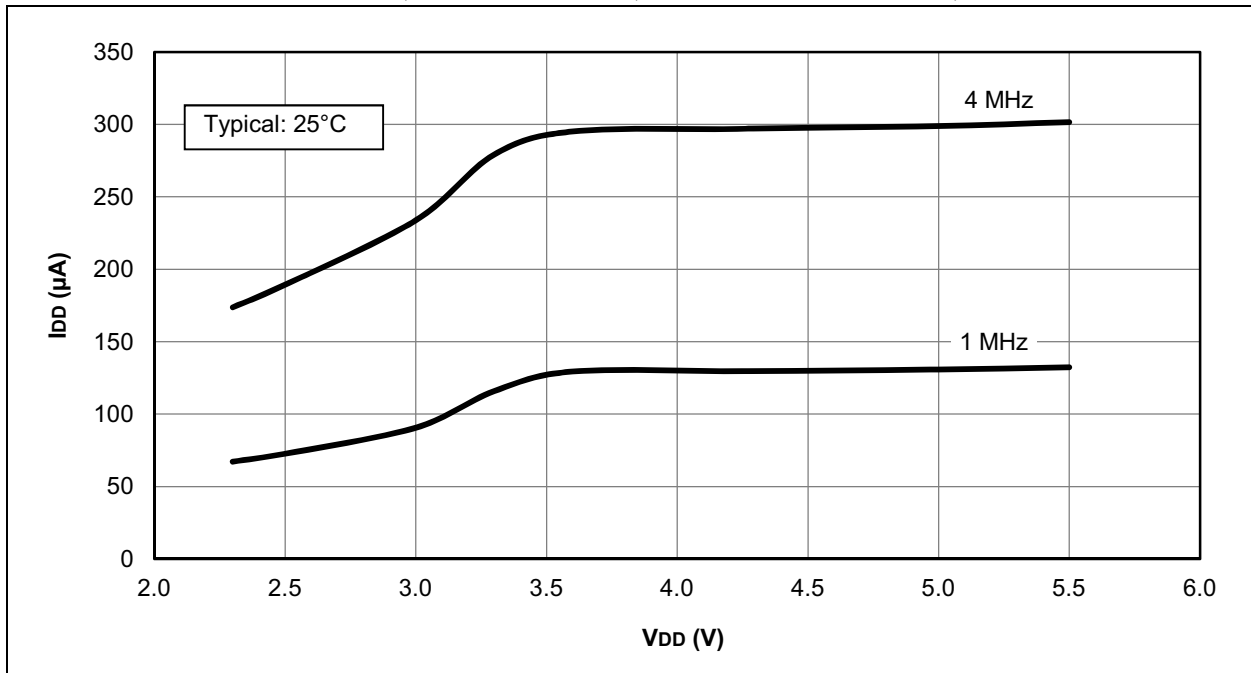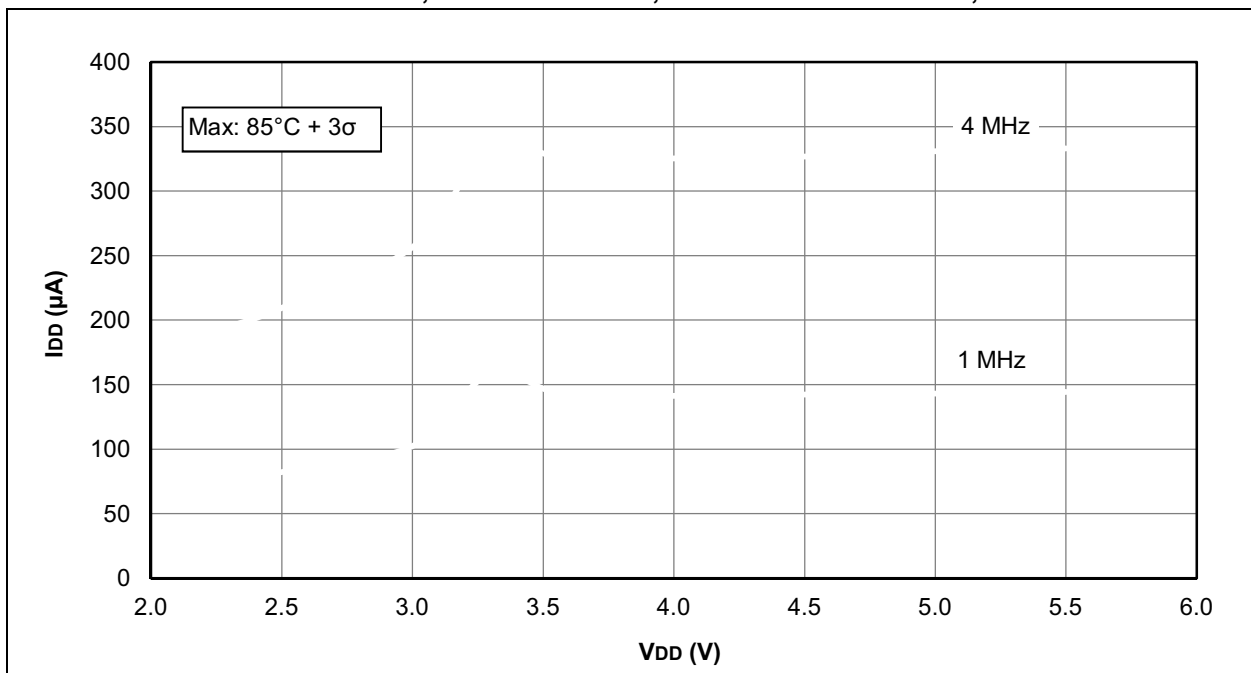

FIGURE 27-8: IDD MAXIMUM, EC OSCILLATOR, MEDIUM POWER MODE, PIC12F1571/2 ONLY

28.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

28.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
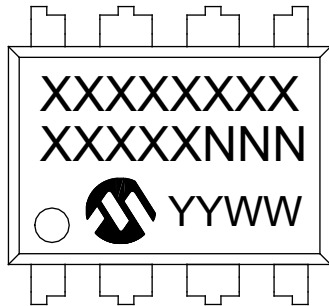- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
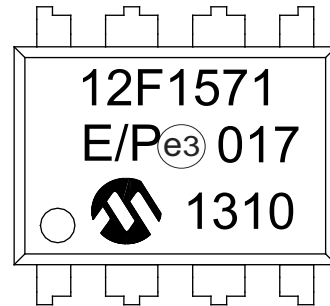- Built-in support for Bugzilla issue tracker

29.0 PACKAGING INFORMATION
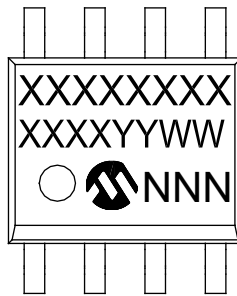
29.1 Package Marking Information
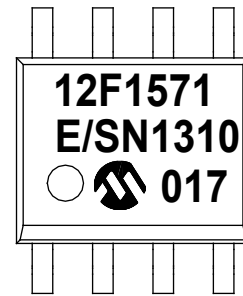
8-Lead PDIP (300 mil)   Example

```
XXXXXXXX                           12F1571
XXXXXNNN                           E/P(e3) 017
   ⬤  🅜 YYWW                         ⬤  🅜 1310
```

8-Lead SOIC (3.90 mm)   Example

```
XXXXXXXX                           12F1571
XXXXXYYWW                          E/SN1310
   ◯  🅜 NNN                         ◯  🅜 017
```

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

PIC12(L)F1571/2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

> **Note:** For the most current package drawings, please see the Microchip Packaging Specification located at
> http://www.microchip.com/packaging
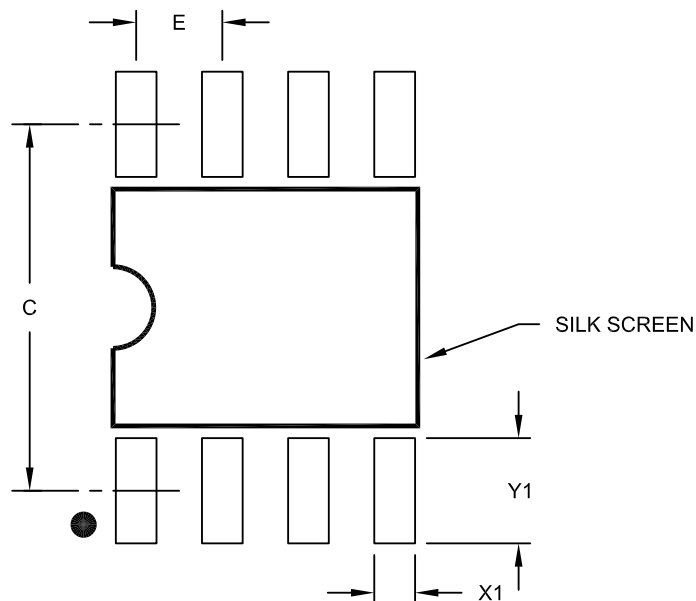
RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X][1]	-	X	/XX	XXX
Device	**Tape and Reel Option**		**Temperature Range**	**Package**	**Pattern**

Device:	PIC12LF1571, PIC12F1571 PIC12LF1572, PIC12F1572
Tape and Reel Option:	Blank = Standard packaging (tube or tray) T = Tape and Reel[1]
Temperature Range:	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)
Package:[2]	MF = Micro Lead Frame (DFN) 3x3x0.9 mm MS = MSOP P = Plastic DIP SN = SOIC RF = Micro Lead Frame (UDFN) 3x3x0.5 mm
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)

Examples:

a) PIC12LF1571T - I/SO
   Tape and Reel,
   Industrial temperature,
   SOIC package

b) PIC12F1572 - I/P
   Industrial temperature,
   PDIP package

c) PIC12F1571-E/MF
   Extended Temperature,
   DFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: For other small form-factor package availability and marking information, please visit www.microchip.com/packaging or contact your local sales office.

NOTES: