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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	ARM® Cortex®-A53, ARM® Cortex®-M4
Number of Cores/Bus Width	4 Core, 64-Bit/1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	DDR3, DDR3L, LPDDR2
Graphics Acceleration	Yes
Display & Interface Controllers	APEX2-CL, DCU (2D-ACE), ISP, LCD, MIPICSI2, Video, VIU
Ethernet	1Gbps
SATA	-
USB	-
Voltage - I/O	1V, 1.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	AES, ARM TZ, Boot, CSE, OCOTP_CTRL, System JTAG
Package / Case	621-FBGA, FCBGA
Supplier Device Package	621-FCPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32v234bln1vub

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1 Block diagram

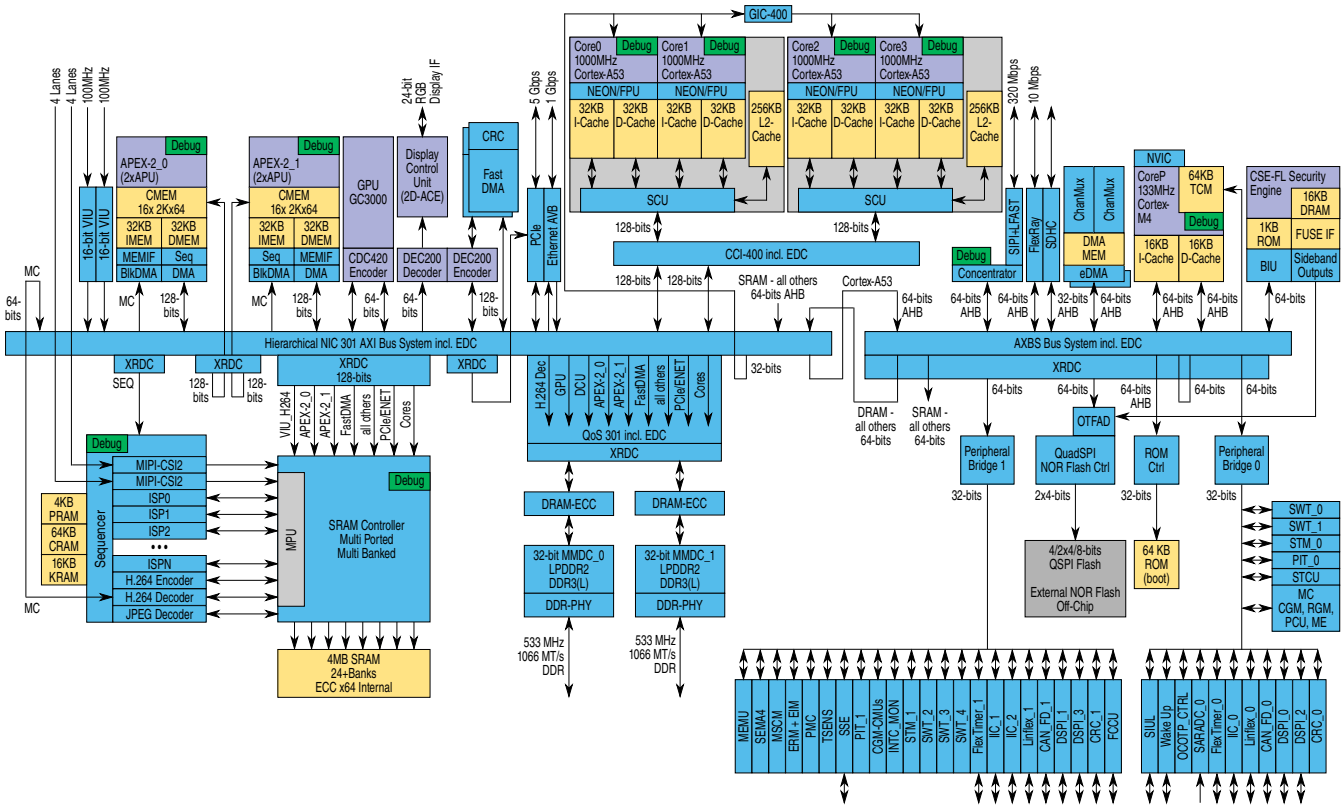


Figure 1. Block diagram

2 Family comparison

2.1 Feature Set

This family of devices supports the following features:

Table 1. Feature Set

Feature	S32V234	S32V232
ARM Cortex-A53 Core	• Up to 1000 MHz Quad ARM Cortex-A53 • 32 KB/32 KB I-/D- L1 Cache • NEON MPE co-processor • Dual precision FPU • 256 KB L2 Cache per cluster • MMU • GIC interrupt controller	• Up to 800 MHz Dual ARM Cortex-A53 (single cluster) • Rest all features same as S32V234

Table continues on the next page...

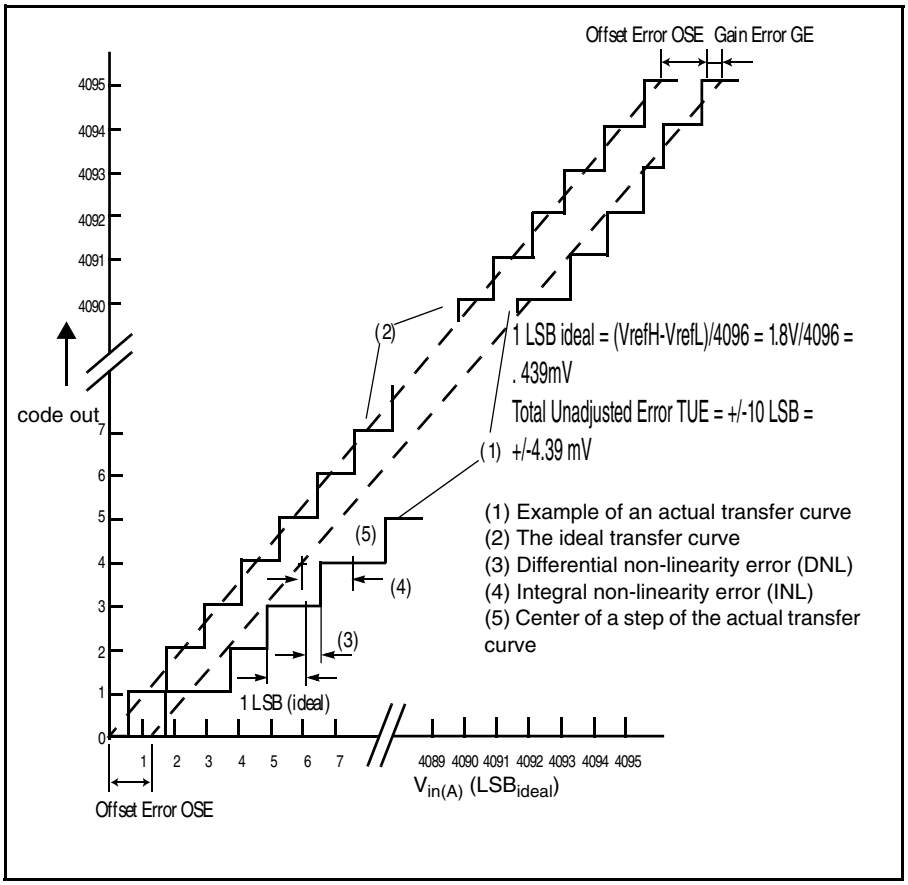


Figure 2. ADC characteristics and error definitions

NOTE

While measuring scaled supply voltages on ADC Channels, Maximum (+5/-10%) variation can be expected .

1. Please see description of Clock & reset section in ADC chapter in Reference Manual for details. User need to generate AD_clk = 40 MHz for 0.5 MSPS operation. For example, if f_{ck} = 80 MHz, configure MCR[8].ADCLKSE = 0 and MCR[4].ADCLKDIV = 0 (default).
2. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming. For internal ADC channels, the minimum sampling time required is 3 microsecond.
3. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
4. Specifications are quoted here for input signal ranging from 150 mV to VDD_HV_ADC - 150 mV. For signals outside this range, the Specifications may degrade beyond limits specified in this table.

6.1.2 Thermal Monitoring Unit (TMU)

The following table describes TMU electrical characteristics.

Table 17. TMU electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
T_j	Temperature monitoring range	—	-40	—	125	°C
T_{SENS}	Sensitivity	—	—	2.5	—	mV/°C
T_{ACC}	Accuracy	T_J = -40 °C to 40 °C	-10	—	+10	°C
		T_J = 40 °C to 125 °C	-6	—	+6	°C

6.2 Clocks and PLL interfaces modules

6.2.1 Main oscillator electrical characteristics

The device provides an oscillator/resonator driver of a Pierce-type structure.

Table 18. Main oscillator electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$f_{FXOSCHS}$	Oscillator frequency	—	—	40.0	n/a	MHz
$T_{FXOSCHSSU}$	Oscillator start-up time	$f_{FXOSCHS}$ = 40 MHz	—	—	2[1]	ms
V_{IH}	Input high level CMOS Schmitt Trigger	Vref = 0.5*VDD_HV_OSC where VDD_HV_OSC is FXOSC HV Supply	Vref+0.5	—	VDD_HV_OSC	V
V_{IL}	Input low level CMOS Schmitt Trigger	Vref = 0.5*VDD_HV_OSC where VDD_HV_OSC is FXOSC HV Supply	0	—	Vref – 0.5	V

1. The start-up time is dependent upon crystal characteristics, board leakage, etc, high ESR and excessive capacitive loads can cause long start-up time

Following crystals are used in internal crystal oscillator validation:

- NX3225 – 40 MHz; Load capacitance = 8 pF
- NX5032 – 40 MHz; Load capacitance = 8 pF

6.2.2 48 MHz FIRC electrical characteristics

Table 19. FIRC electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
F_{Target}	FIRC target frequency (trimmed)	—	—	48	—	MHz
δF_{var_T}	FIRC frequency variation with respect to supply and temperature after process trimming	—	-10	—	+10	%

6.2.3 PLL electrical specifications

Table 20. PLL electrical characteristics [1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLLIN}	PLL input clock[2]	—	20[3]	—	40[3]	MHz
Δ_{PLLIN}	PLL input clock duty cycle [2]	—	40	—	60	%
$t_{PLLLOCK}$	PLL lock time	—	—	—	100	µs
Δ_{PLLT}	Period jitter	—	—	—	150	ps
Δ_{PLLTIE}	TIE	—	—	—	560	ps
f_{PLLMOD}	SSCG modulation frequency	—	—	—	32	kHz
δ_{PLLMOD}	SSCG modulation depth (Down Spread)	—	0.50	—	2.7[4]	%

1. The jitter values are gauranteed for following conditions:
   1. Measurement being done on LFAST TX pad with observed frequency greater than 250 M and less than 320 M
   2. Minimum SOC activity - Operations required to observe clock must be functional.
   3. Maximum frequency change in SSCG modulation is limited by following relation: Modulation Depth * VCO Frequency < PLL Reference (PFD) Frequency
2. PLL0IN clock retrieved from either internal RCOSC or external FXOSC clock. Input characteristics are granted when using internal RCOSC or external oscillator is used in functional mode.
3. The PLLIN clock is the frequency after the PREDIV(Pre-divider) value division, and before the Phase detector block. Please refer to the PLLs section of clocking chapter in the Reference Manual.

6.3 Memory interfaces

6.3.1 QuadSPI AC specifications

- Measurements are with a load of 35 pF on output pins. Input slew: 1 ns, DSE[2:0] = 111, and FSEL[1:0] = 11
- QuadSPI input timing is with 15 pF load on flash output.
- QuadSPI_MCR[DQS_EN] must be set as 1 for SDR READ

The following table lists various QuadSPI modes and their corresponding configurations. Please refer to the device Reference Manual for register and bit descriptions.

Table 23. QuadSPI read/write settings

Modes supported by QuadSPI		QuadSPI_MCR[DDR_EN]	QuadSPI_MCR[DQS_EN]	QuadSPI_MCR [DQS_CD]	QuadSPI_MCR [REFCLK_SEL]	QuadSPI_MCR [DQS_MDSL]	QuadSPI_SOCCR [FDCC_FB]	QuadSPI_SOCCR [FDCC_FA]	QuadSPI_FLSHCR[TDH]
SDR mode	Internal DQS mode	0	1	000	1	1	39h @ 3.3 V 3Fh @ 1.8 V	39h @ 3.3 V 3Fh @ 1.8 V	00
DDR mode	Internal DQS mode	1	1	000	0	1	4Ah @ 3.3 V 50h @ 1.8 V	4Ah @ 3.3 V 50h @ 1.8 V	01
	External DQS mode (supported by HyperFlash)	1	1	000	0	0	00h	00h	01

SDR mode

For SDR mode, QuadSPI_MCR[DQS_EN] must be set as '1'.

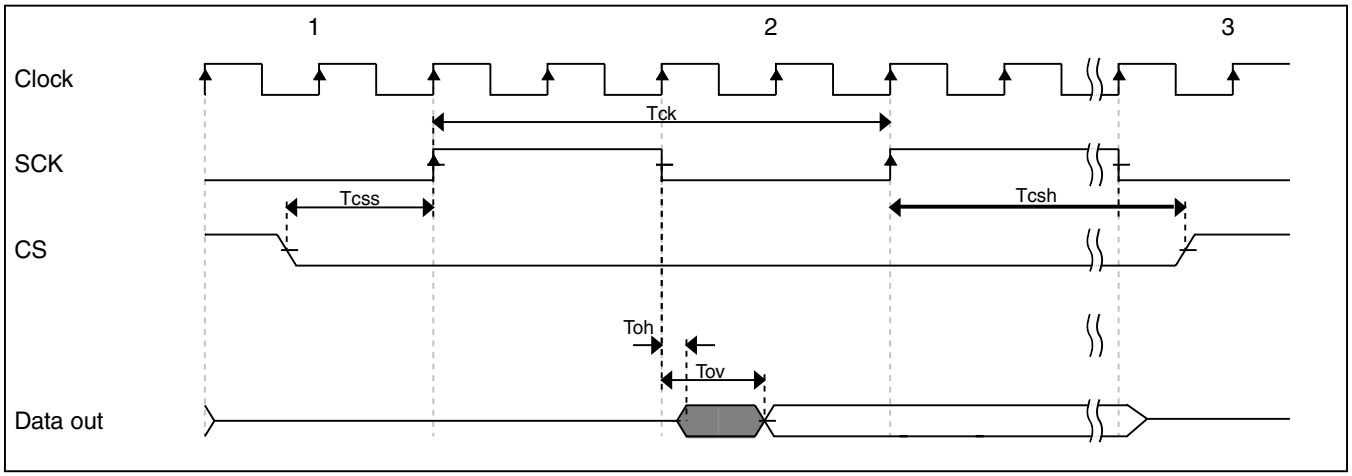


Figure 5. QuadSPI output timing (SDR mode) diagram

Table 25. QuadSPI output timing (SDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{ov}	Output Data Valid	—	1.5	ns
T_{oh}	Output Data Hold	–1.5	—	ns
F_{SCK}	SCK clock frequency	—	104	MHz
T_{css}	Chip select output setup time	2	—	ns
T_{csh}	Chip select output hold time	1	—	ns

NOTE

For any frequency setup and hold specifications of the memory should be met.

DDR mode

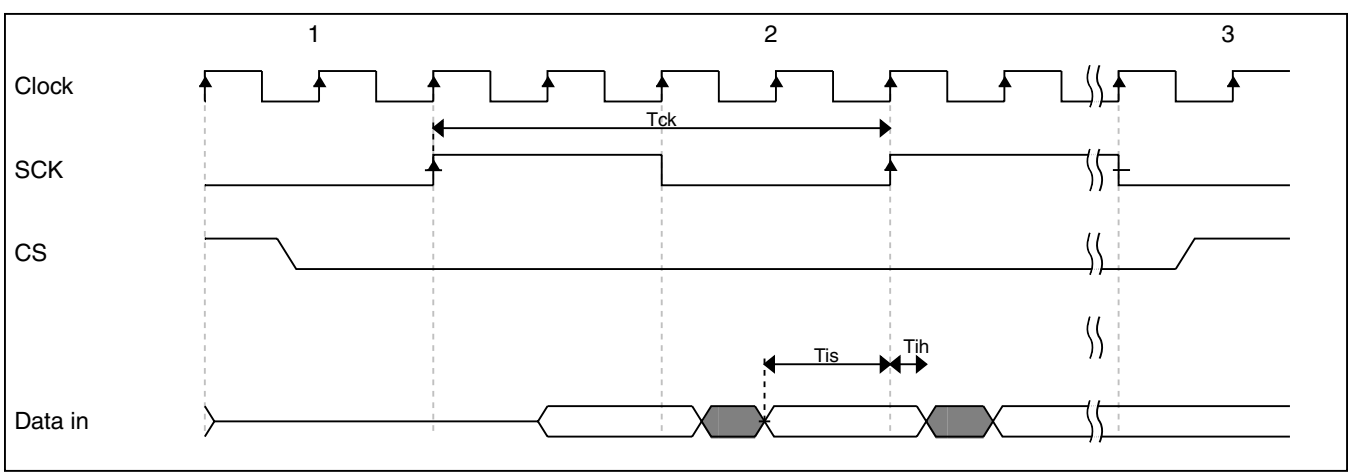


Figure 6. QuadSPI input timing (DDR mode) diagram

4. This value of 16 ns is with the configuration prescaler values: SPI_CTARn[PASC] - "After SCK Delay Prescaler" configuration is "3" (01h) and SPI_CTARn[ASC] - "After SCK Delay Scaler" configuration is "2" (0000h).

NOTE

DSPI Timing specs on this chip are valid with Slave in Classic Mode only.

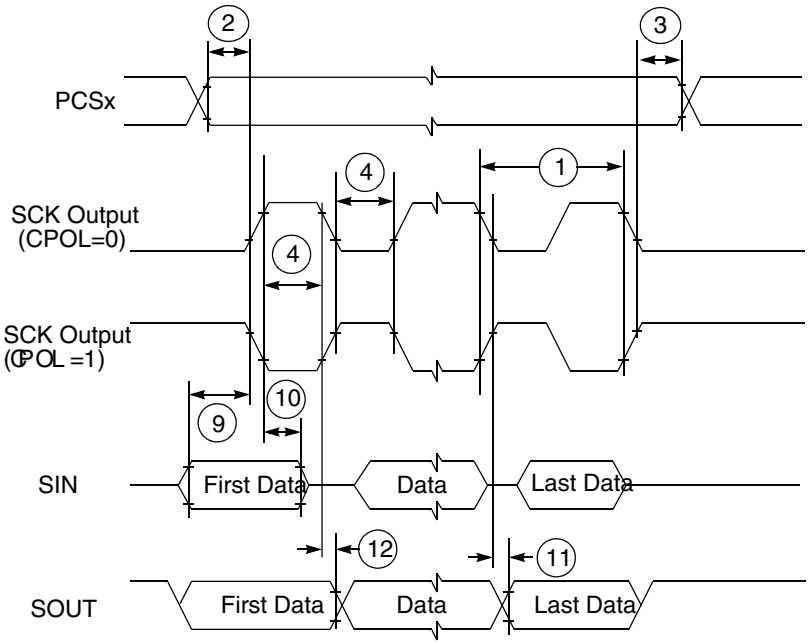


Figure 16. DSPI classic SPI timing — master, CPHA = 0

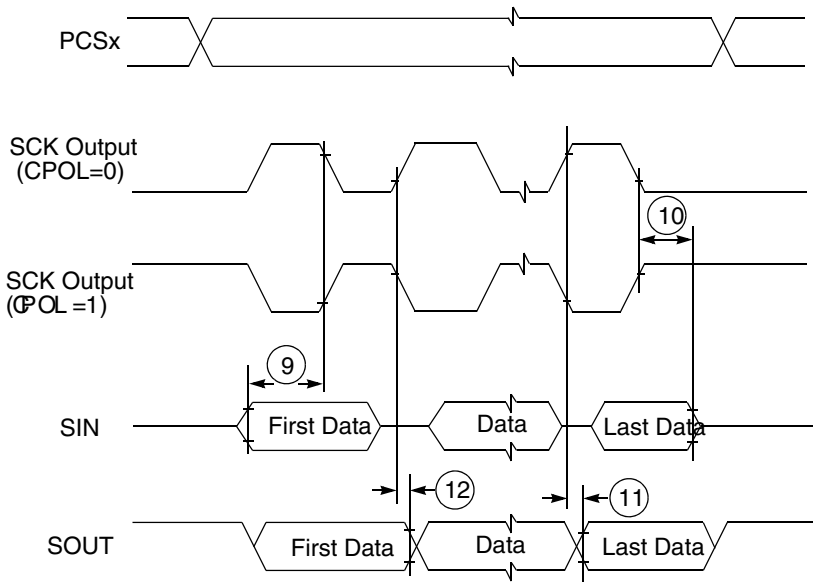


Figure 17. DSPI classic SPI timing — master, CPHA = 1

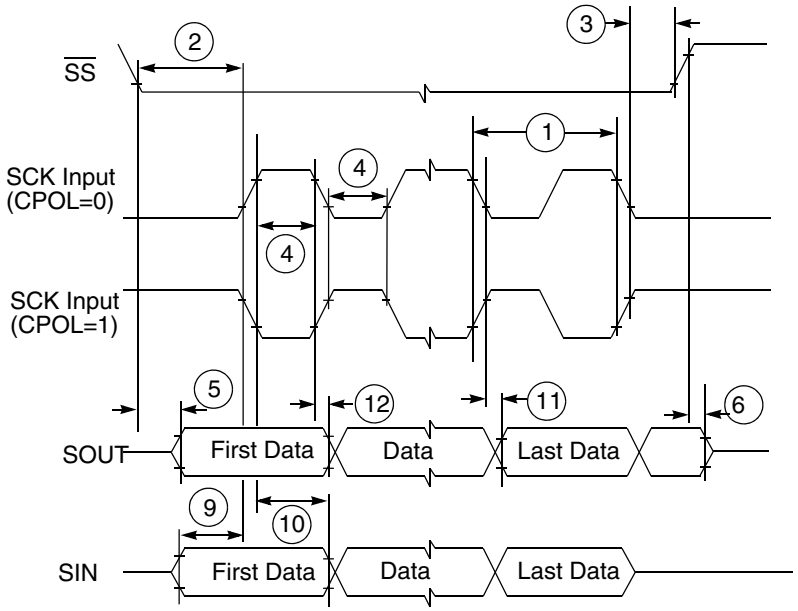


Figure 18. DSPI classic SPI timing — slave, CPHA = 0

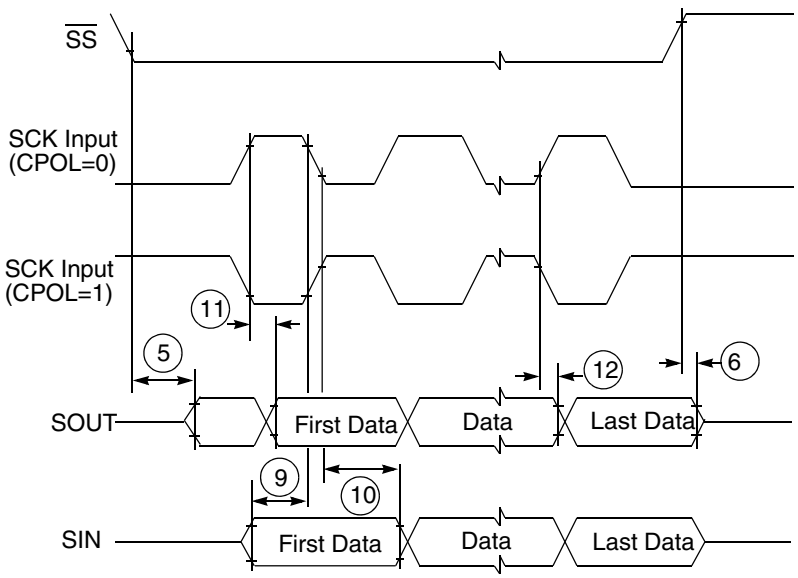


Figure 19. DSPI classic SPI timing — slave, CPHA = 1

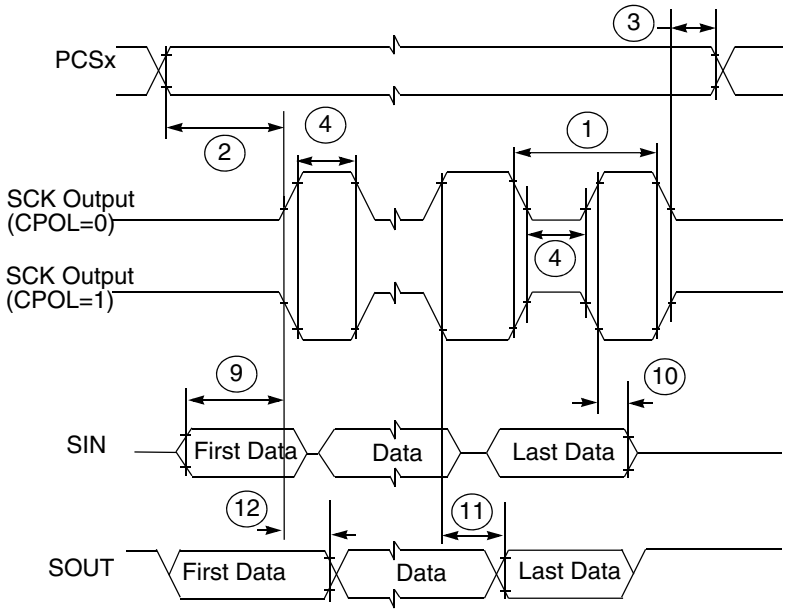


Figure 20. DSPI modified transfer format timing — master, CPHA = 0

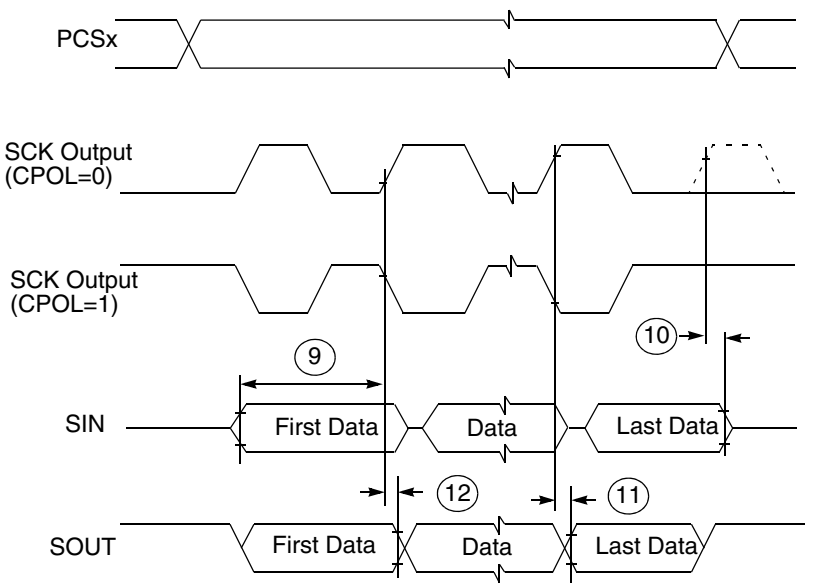


Figure 21. DSPI modified transfer format timing — master, CPHA = 1

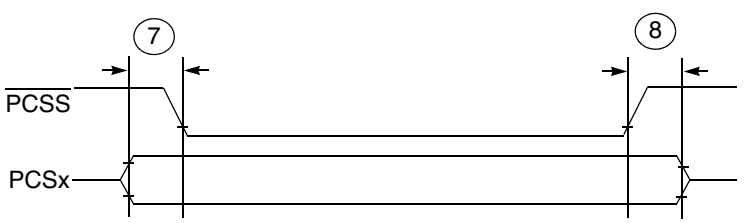


Figure 22. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

6.5.3 LFAST electrical characteristics

6.5.3.1 LFAST interface timing diagrams

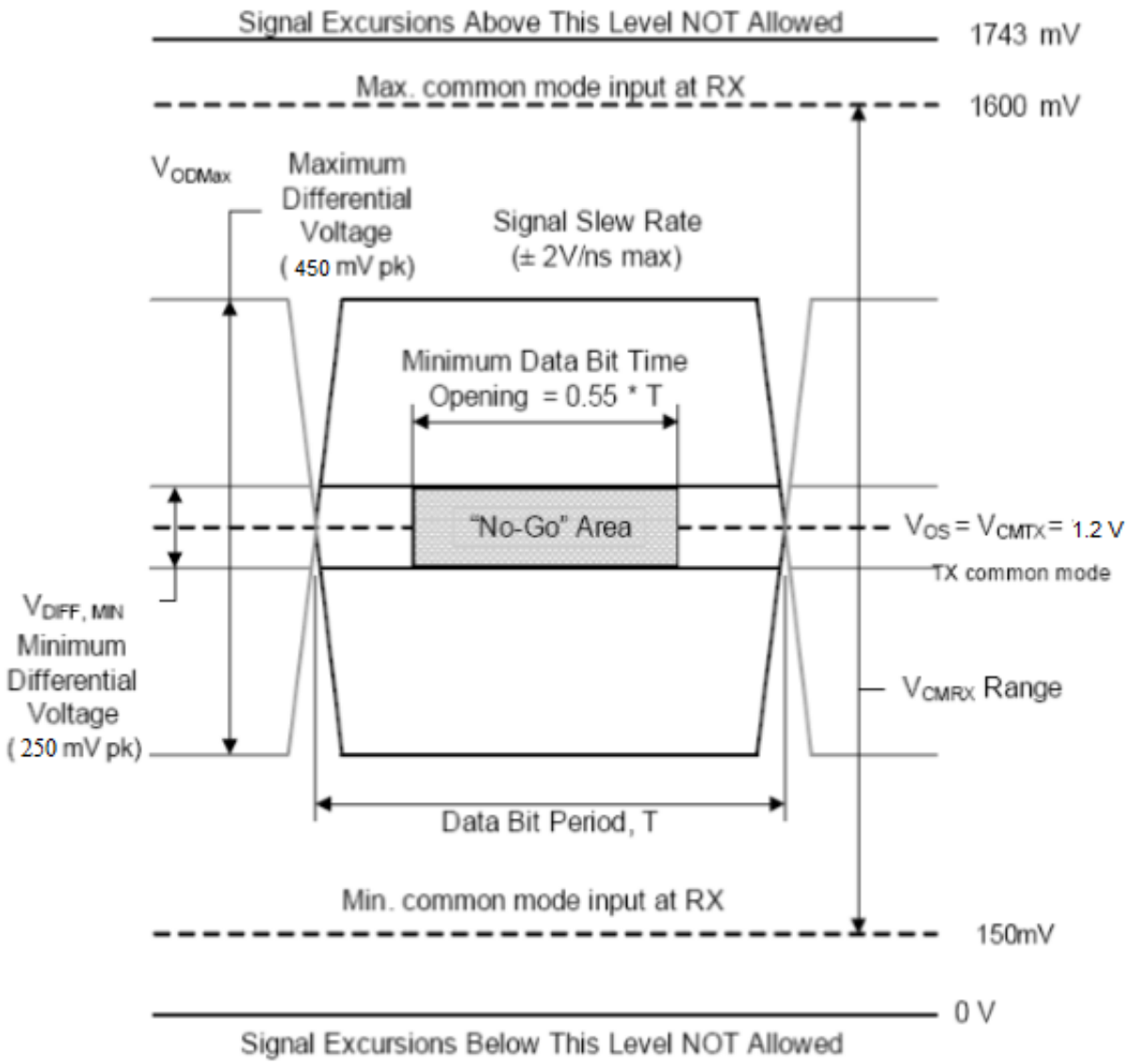


Figure 29. LFAST timing definition

7. Total capacitance including silicon, package pin and bond wire
8. Total inductance including silicon, package pin and bond wire

6.5.4 FlexRay

6.5.4.1 FlexRay timing parameters

This section provides the FlexRay interface timing characteristics for the input and output signals. These numbers are recommended per the FlexRay Electrical Physical Layer Specification, Version 3.0.1, and subject to change per the final timing analysis of the device.

6.5.4.2 TxEN

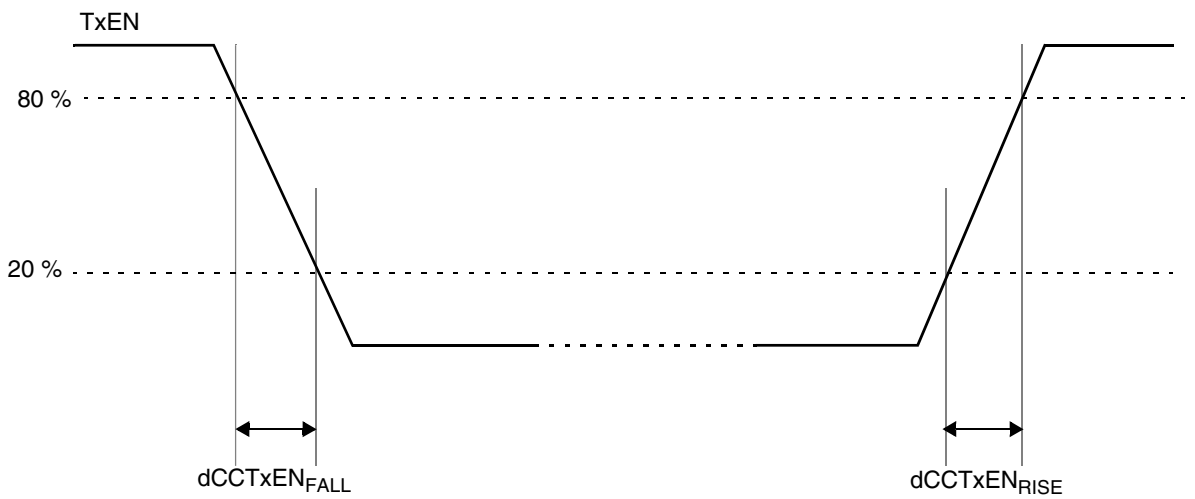


Figure 31. TxEN signal

Table 40. TxEN output characteristics[1]

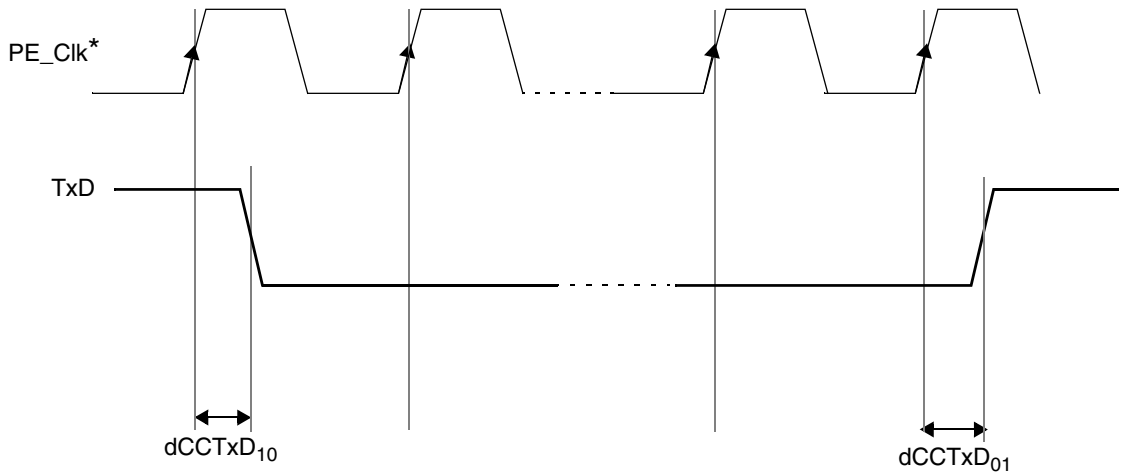
Name	Description	Min	Max	Unit
$dCCTxEN_{RISE25}$	Rise time of TxEN signal at CC	-	9	ns
$dCCTxEN_{FALL25}$	Fall time of TxEN signal at CC	-	9	ns
$dCCTxEN_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	-	25	ns
$dCCTxEN_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	-	25	ns

1. TxEN pin load maximum 25 pF.

Table 41. TxD output characteristics (continued)

Name	Description[1]	Min	Max	Unit
$dCCTxD_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	-	25	ns
$dCCTxD_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	-	25	ns

1. TxD pin load maximum 25 pF.



*FlexRay Protocol Engine Clock

Figure 34. TxD signal propagation delays

6.5.4.4 RxD

Table 42. RxD input characteristics

Name	Description	Min	Max	Unit
C_CCRxD	Input capacitance on RxD pin	-	7	pF
uCCLogic_1	Threshold for detecting logic high	35	70	%
uCCLogic_0	Threshold for detecting logic low	30	65	%
$dCCRxD_{01}$	Sum of delay from actual input to the D input of the first FF, rising edge	-	10	ns
$dCCRxD_{10}$	Sum of delay from actual input to the D input of the first FF, falling edge	-	10	ns

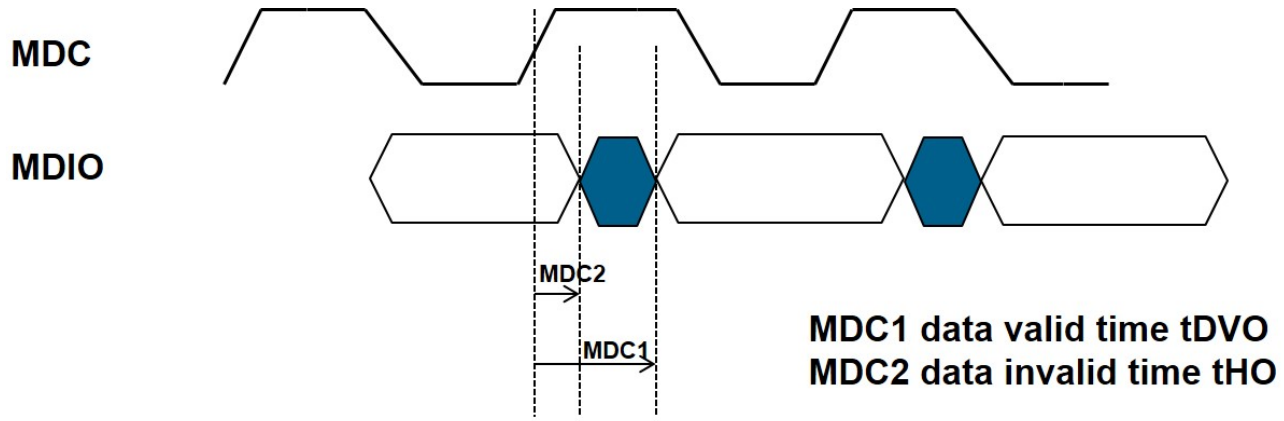


Figure 42. MDIO output timing

Table 47. MDIO interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
MDCO	Clock Duty Cycle	t_{MDC}	40	60	%
MDIO Output Timing					
MDC1	MDC to MDIO Valid	t_{DVO}	—	50	ns
MDC2	MDC to MDIO Invalid	t_{HO}	10	—	ns
MDIO Input Timing					
MDC3	MDIO Input Setup time	t_{SUI}	50	—	ns
MDC4	MDIO Input Hold time	t_{HI}	0	—	ns

6.5.6 PCI Express specifications

The PCI Express link conforms to the *PCI Express Base Specification*, Revision 2.1. The following summary of Transmitter and Receiver specifications are copied directly from the Base Specification. Consult the Base Specification for additional details.

Table 48. PCI Express transmitter specifications[1]

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps
$V_{TX\text{-}DIFF\text{-}PP}$	Differential p-p Tx voltage swing	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V
$V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	Tx de-emphasis level ratio	3.0 (min) 4.0 (max)	3.0 (min) 4.0 (max)	dB
$V_{TX\text{-}DE\text{-}RATIO\text{-}6dB}$	Tx de-emphasis level	N/A	5.5 (min) 6.5 (max)	dB
$T_{MIN\text{-}PULSE}$	Instantaneous lone pulse width	Not specified	0.9 (min)	UI

Table continues on the next page...

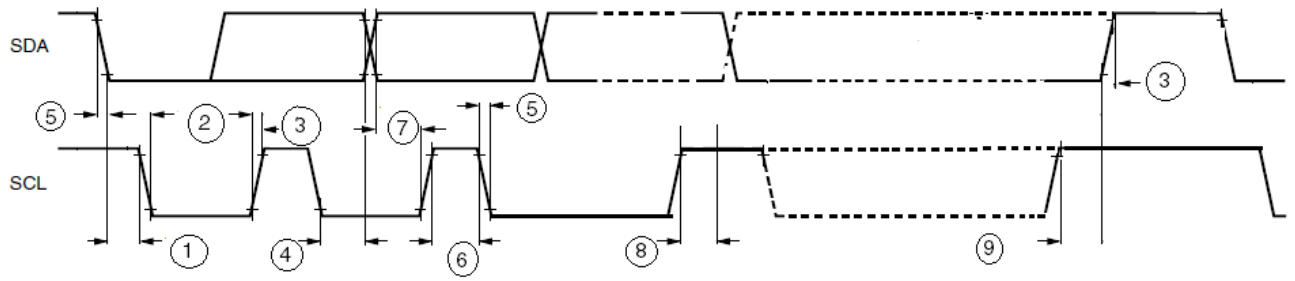


Figure 43. IIC input/output timing

6.5.8 LINFlex timing

The maximum bit rate is 1.875 MBit/s.

6.6 Display modules

6.6.1 Display Control Unit (2D-ACE) Parameters

6.6.1.1 Interface to TFT panels

This section provides the LCD interface timing for a generic active matrix color TFT panel. Measurements are with a load of 20 pF on output pins. Input slew = 1 ns, DSE[2:0] = 111, and FSEL[1:0] = 11. In the figure below[1], signals are shown with positive polarity. The sequence of events for active matrix interface timing:

- PCLK latches data into the panel on its positive edge (when positive polarity is selected). In active mode, PCLK runs continuously. This signal frequency could be from 5 to 150 MHz depending on the panel type.
- HSYNC causes the panel to start a new line. It always encompasses at least one PCLK pulse.
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.
- DE acts like an output enable signal to the LCD panel. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

1. LD[23:0]" signal is "line data," an aggregation of the 2D-ACE's RGB signals—R[0:7], G[0:7] and B[0:7].

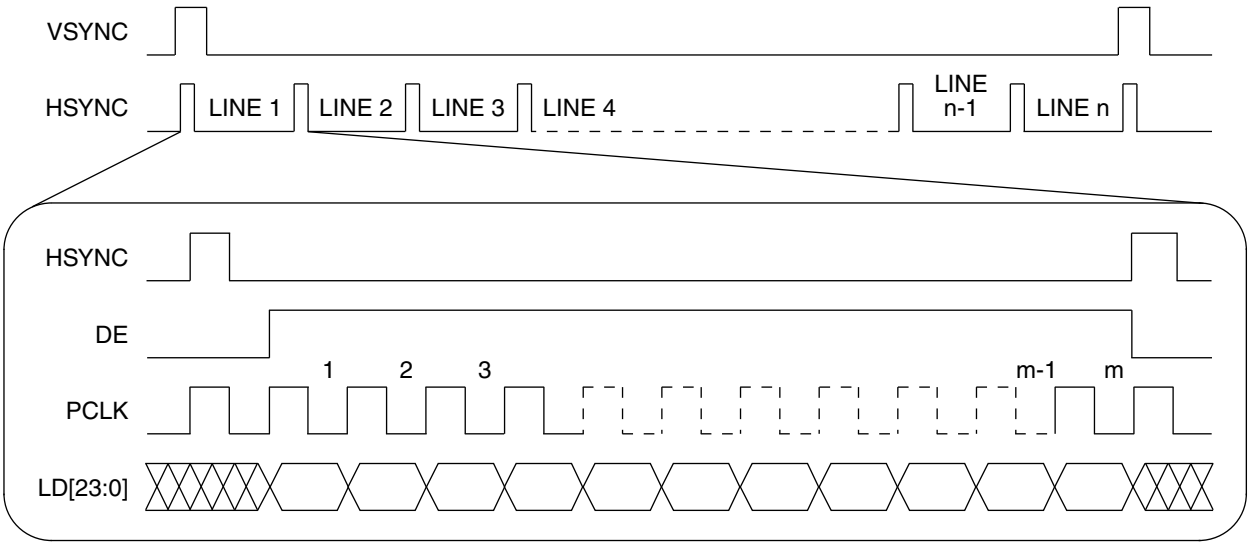


Figure 44. TFT LCD interface timing overview

6.6.1.2 Interface to TFT LCD Panels—Pixel Level Timings

This section provides the horizontal timing (timing of one line), including both the horizontal sync pulse and data. All parameters shown in the figure below are programmable. This timing diagram corresponds to positive polarity of the PCLK signal (meaning the data and sync signals change on the rising edge) and active-high polarity of the HSYNC, VSYNC and DE signals. The user can select the polarity of the HSYNC and VSYNC signals via the SYN_POL register, whether active-high or active-low. The default is active-high. The DE signal is always active-high. Pixel clock inversion and a flexible programmable pixel clock delay are also supported. They are programmed via the clock divide . The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register. The PW_H, BP_H and FP_H parameters are programmed via the HSYN PARA register. The PW_V, BP_V and FP_V parameters are programmed via the VSYN_PARA register.

Table 52. LCD interface timing parameters—horizontal and vertical

Symbol	Characteristic		Unit
t_{PCP}	Display pixel clock period	6.66	ns
t_{PWH}	HSYNC pulse width	PW_H * t_{PCP}	ns
t_{BPH}	HSYNC back porch width	BP_H * t_{PCP}	ns
t_{FPH}	HSYNC front porch width	FP_H * t_{PCP}	ns
t_{SW}	Screen width	DELTA_X * t_{PCP}	ns
t_{HSP}	HSYNC (line) period	(PW_H + BP_H + FP_H + DELTA_X) * t_{PCP}	ns
t_{PWV}	VSYNC pulse width	PWV * t_{HSP}	ns
t_{BPV}	VSYNC back porch width	BP_V * t_{HSP}	ns
t_{FPV}	VSYNC front porch width	FP_V * t_{HSP}	ns

Table continues on the next page...

Table 53. LCD Interface Timing Parameters—Access Level (continued)

Symbol	Description	Min	Max	Unit
t^{DV}	TFT interface VSYNC valid after pixel clock	_	3	ns
t^{DV}	TFT interface DE valid after pixel clock	_	3	ns
t^{HO}	TFT interface output hold time for data and control bits	0	_	ns
	Relative skew between the data bits	_	1.5	ns

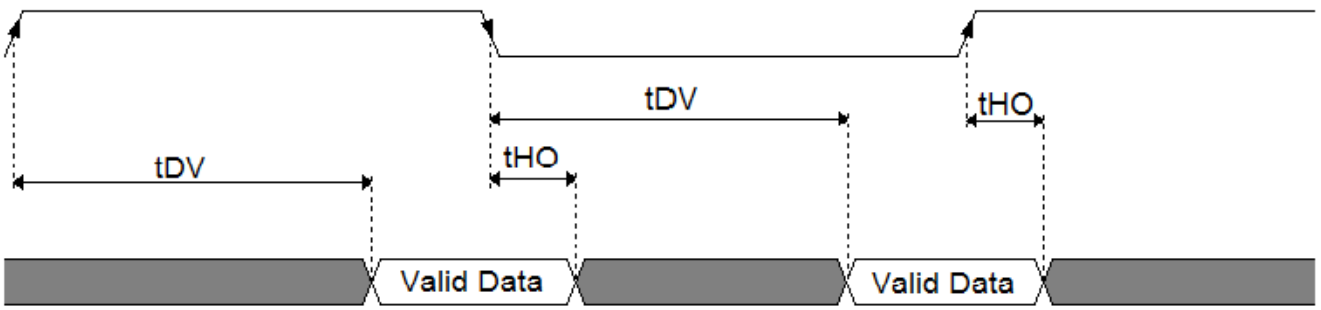


Figure 47. LCD Interface Timing Parameters—Access Level

6.6.2 Video input unit (VIU) timing specifications

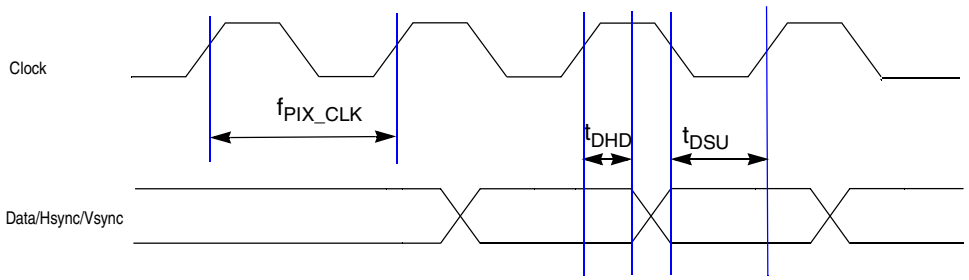


Figure 48. VIU timing diagram

Table 54. VIU timing parameters

Parameter	Description	Min	Typ	Max	Unit
f_{PIX_CK}	VIU pixel clock frequency	—	—	100	MHz
t_{DSU}	VIU Data/Hsync/ Vsync setup time	3	—	—	ns
t_{DHD}	VIU Data/Hsync/ Vsync hold time	1	—	—	ns

Table 60. PCIe JTAG AC electrical characteristics[1] (continued)

#	Symbol	Characteristic	Min	Max	Unit
14	t_{BSDST}	Boundary Scan Input Valid to TCK Rising Edge	15	-	ns
15	t_{BSDHT}	TCK Rising Edge to Boundary Scan Input Invalid	15	-	ns

1. These specifications apply to boundary scan, JTAG and CJTAG, and serial wire debug modes.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
3. Cycle time is 25 ns assuming full cycle timing. Cycle time is 50 ns assuming half cycle timing.
4. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
5. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

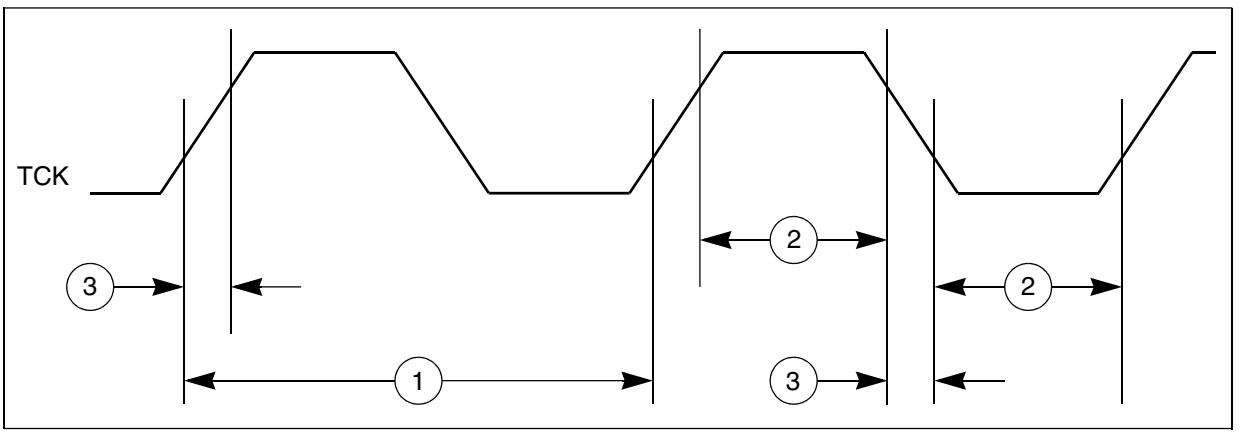


Figure 52. JTAG test clock input timing

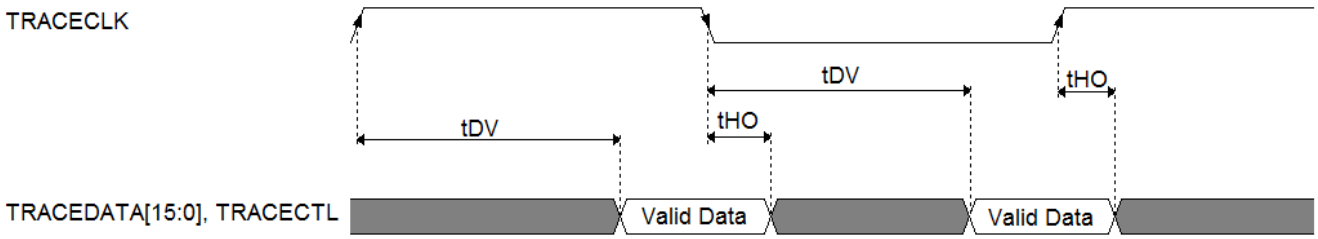


Figure 56. TRACE_CLKOUT specifications

6.8 Wakeup Unit (WKPU) AC specifications

Table 62. WKPU glitch filter specifications

Symbol	Parameter	Min	Typ	Max	Unit
W_{FNMI}	NMI pulse width that is rejected	-	-	20	ns
W_{NFNMI}	NMI pulse width that is passed	400	-	-	ns

6.9 RESET pin glitch filter specifications

Table 63. RESET pin glitch filter specifications

Symbol	Parameter	Min	Typ	Max	Unit
W_{FRESET}	RESET pulse width that is rejected	-	-	20	ns
$W_{NFRESET}$	RESET pulse width that is passed	400	-	-	ns

6.10 External interrupt timing (IRQ pin)

Table 64. External interrupt timing

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	IRQ pulse width low	-	3	-	t_{CYC}
2	t_{IPWH}	IRQ pulse width high	-	3	-	t_{CYC}
3	t_{ICYC}	IRQ edge to edge time[1]	-	6	-	t_{CYC}

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

Table 69. Revision history

Revision	Date	Description of changes

		• In Table 13, removed parameter “Rod_keep”. Updated minimum, typical, and maximum value of parameter Rkeep.
		• In Table 14, removed parameter “Rod_keep”.
		• In Table 15, removed parameter “Rod_keep” and deleted footnote “Note that the Jedec LPDDR2 specification (JESD209-2B) supersedes any specification in this document”.
		• In Table 16
		  • updated ADC Input Clock frequency
		  • added ADC Conversion clock frequency
		  • removed conditions of Sample time and Conversion time
		  • removed all information about parameter “Max positive/negative injection” and modified “Total unadjusted error” in “TUE”.
		• In Table 18, modified the minimum and maximum values of V_{IH} and V_{IL}.
		• In Table 20 :
		  • Changed maximum value of SSCG modulation depth from -6% to -5.4%, and added condition STEPSIZE x STEPNO < 18432.
		  • Removed “PLL VCO frequency” and “PLL output clock PHI0”, and deleted footnote "All PLLs have same specifications. PLL programming should take maximum clock frequencies as per Reference Manual recommendation”.
		• Added Table 20.
		• In Table 22 :
		  • unit for Total Jitter has been changed from ps to ns.
		  • removed max Deterministic and max Random jitter specifications; added footnote in max Total Jitter.
		• In Table 23 :
		  • Made modification in DDR mode.
		  • Updated values of QuadSPI_SOCCR[FDCC_FB] and QuadSPI_SOCCR[FDCC_FA] for SDR and DDR mode (internal DQS Mode) and added footnote “Device qualification is not complete.”
		• Deleted Table "QuadSPI input timing (DDR mode) specifications with learning"
		• In Table 25 changed Minimum value of Chip select output setup time and Chip select output hold time.
		• In Table 26
		  • changed maximum value of SCK Clock Frequency and updated configuration. Also, changed table caption
		  • changed the minimum value of "Setup time for incoming data".
		• In Table 27 :
		  • deleted "Chip select output setup time" and "Chip select output hold time".
		  • changed the maximum value of "Output Data Valid" and minimum value of "Output Data Hold".
		• In Table 28, updated minimum value of parameters “Setup time for incoming data” and “Hold time for incoming data”.
		• In Table 29, updated maximum value of “Ck to Ck2 skew max” and minimum value of “Ck to Ck2 skew min”.
		• In Table 30 changed symbol and minimum value of DDR4, DDR5, DDR6, and DDR7.
		• In Table 31 modified minimum value of DDR26 from 540 to 563 ps.
		• In Table 32 changed the symbol and minimum value of DDR17 and DDR18.
		• In Table 33 changed the symbol and minimum value of parameters CKE setup time, CKE hold time, CA setup time, and CA hold time.
		• In Table 34 changed the minimum value of LP26.
		• In Table 35 changed the symbol and minimum value of LP17 and LP18.
		• In Table 36 :
		  • Updated footnotes to include changes in PCSSCK, CSSCK, PASC, ASC values.
		  • Updated footnotes in minimum timing of parameter DSPI cycle time, PCS to SCK delay, and After SCK delay.

Table continues on the next page...