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C161S

16-Bit Single-Chip Microcontroller

Microcontrollers

Never stop thinking.

This document describes several derivatives of the C161 group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

Table 1 C161S Derivative Synopsis

Derivative	Max. Operating Frequency	Operating Voltage	Ambient Temperature
SAB-C161S-L25M	25 MHz	4.5 to 5.5 V (Standard)	0 to 70 °C
SAF-C161S-L25M	25 MHz	4.5 to 5.5 V (Standard)	-40 to 85 °C
SAB-C161S-LM3V	20 MHz	3.0 to 3.6 V (Reduced)	0 to 70 °C
SAF-C161S-LM3V	20 MHz	3.0 to 3.6 V (Reduced)	-40 to 85 °C

For simplicity all versions are referred to by the term **C161S** throughout this document.

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the C161S please refer to the **“Product Catalog Microcontrollers”**, which summarizes all available microcontroller variants.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

3.1 Memory Organization

The memory space of the C161S is configured in a von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 16 Mbytes. The entire memory space can be accessed bytewise or wordwise. Particular portions of the on-chip memory have additionally been made directly bitaddressable.

The C161S is prepared to incorporate on-chip program memory (not in the ROM-less derivatives, of course) for code or constant data. The internal ROM area can be mapped either to segment 0 or segment 1.

2 Kbytes of on-chip Internal RAM (IRAM) are provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, …, RL7, RH7) so-called General Purpose Registers (GPRs).

1024 bytes (2×512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the C166 Family.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 16 Mbytes of external RAM and/or ROM can be connected to the microcontroller. The maximum contiguous external address space is 4 Mbytes, i.e. this is the maximum address window size. Using the chip-select lines (multiple windows) this results in a maximum usable external address space of 16 Mbytes.

3.3 Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C161S's instructions can be executed in just one machine cycle which requires 100 ns at 20 MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16 × 16 bit multiplication in 5 cycles and a 32-/16-bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.

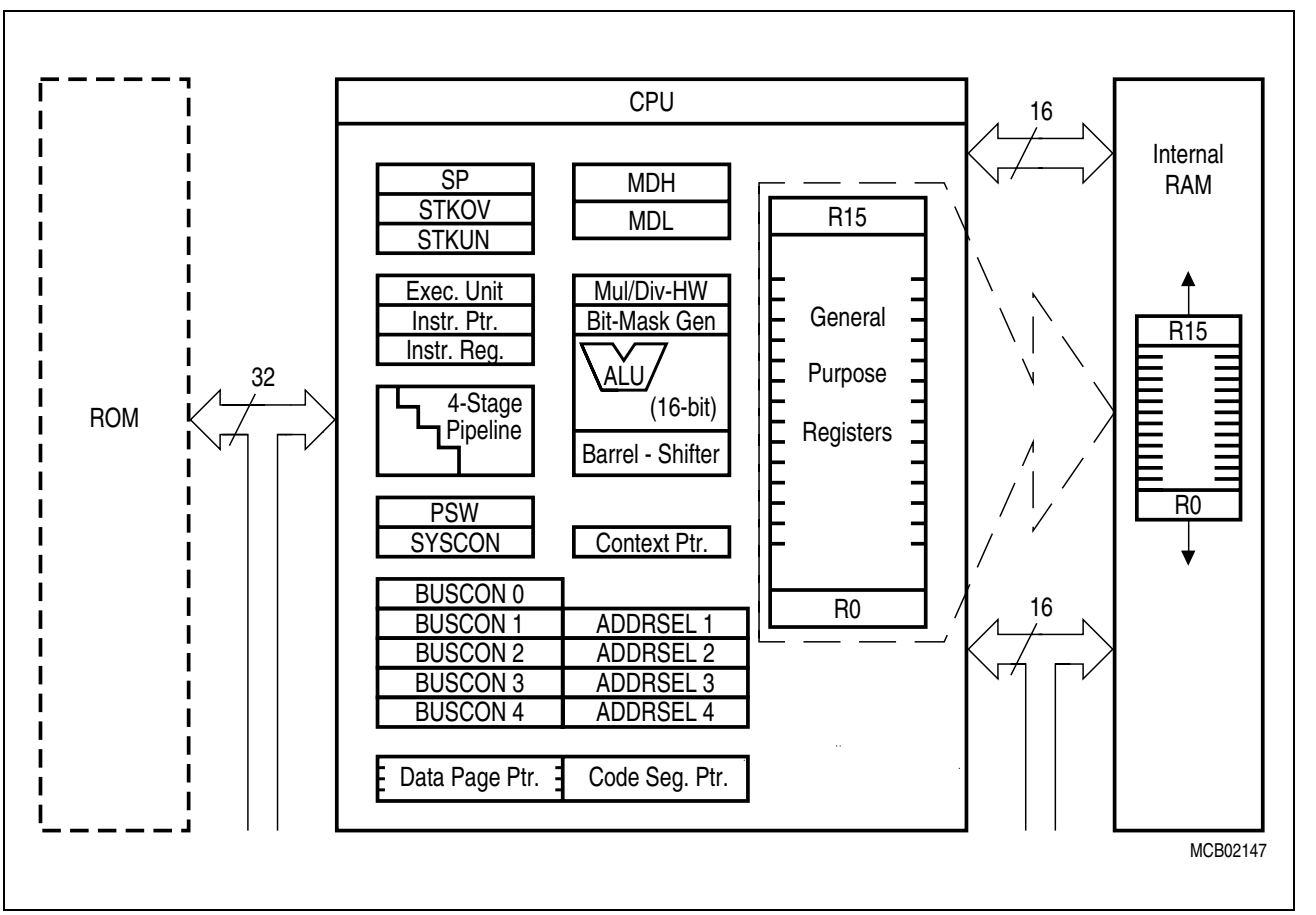

Figure 4 CPU Block Diagram

The CPU has a register context consisting of up to 16 wordwide GPRs at its disposal. These 16 GPRs are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

Table 3 C161S Interrupt Nodes

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
Unassigned node	CC8IR	CC8IE	CC8INT	$00'0060_H$	18_H
External Interrupt 1	CC9IR	CC9IE	CC9INT	$00'0064_H$	19_H
External Interrupt 2	CC10IR	CC10IE	CC10INT	$00'0068_H$	$1A_H$
External Interrupt 3	CC11IR	CC11IE	CC11INT	$00'006C_H$	$1B_H$
External Interrupt 4	CC12IR	CC12IE	CC12INT	$00'0070_H$	$1C_H$
External Interrupt 5	CC13IR	CC13IE	CC13INT	$00'0074_H$	$1D_H$
External Interrupt 6	CC14IR	CC14IE	CC14INT	$00'0078_H$	$1E_H$
External Interrupt 7	CC15IR	CC15IE	CC15INT	$00'007C_H$	$1F_H$
GPT1 Timer 2	T2IR	T2IE	T2INT	$00'0088_H$	22_H
GPT1 Timer 3	T3IR	T3IE	T3INT	$00'008C_H$	23_H
GPT1 Timer 4	T4IR	T4IE	T4INT	$00'0090_H$	24_H
GPT2 Timer 5	T5IR	T5IE	T5INT	$00'0094_H$	25_H
GPT2 Timer 6	T6IR	T6IE	T6INT	$00'0098_H$	26_H
GPT2 CAPREL Reg.	CRIR	CRIE	CRINT	$00'009C_H$	27_H
Unassigned node	ADCIR	ADCIE	ADCINT	$00'00A0_H$	28_H
Unassigned node	ADEIR	ADEIE	ADEINT	$00'00A4_H$	29_H
ASC0 Transmit	S0TIR	S0TIE	S0TINT	$00'00A8_H$	$2A_H$
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	$00'011C_H$	47_H
ASC0 Receive	S0RIR	S0RIE	S0RINT	$00'00AC_H$	$2B_H$
ASC0 Error	S0EIR	S0EIE	S0EINT	$00'00B0_H$	$2C_H$
SSC Transmit	SCTIR	SCTIE	SCTINT	$00'00B4_H$	$2D_H$
SSC Receive	SCRIR	SCRIE	SCRINT	$00'00B8_H$	$2E_H$
SSC Error	SCEIR	SCEIE	SCEINT	$00'00BC_H$	$2F_H$
Unassigned node	XP0IR	XP0IE	XP0INT	$00'0100_H$	40_H
Unassigned node	XP1IR	XP1IE	XP1INT	$00'0104_H$	41_H
Unassigned node	XP2IR	XP2IE	XP2INT	$00'0108_H$	42_H
PLL/OWD and RTC	XP3IR	XP3IE	XP3INT	$00'010C_H$	43_H
Unassigned node	CC29IR	CC29IE	CC29INT	$00'0110_H$	44_H
Unassigned node	CC30IR	CC30IE	CC30INT	$00'0114_H$	45_H
Unassigned node	CC31IR	CC31IE	CC31INT	$00'0118_H$	46_H

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

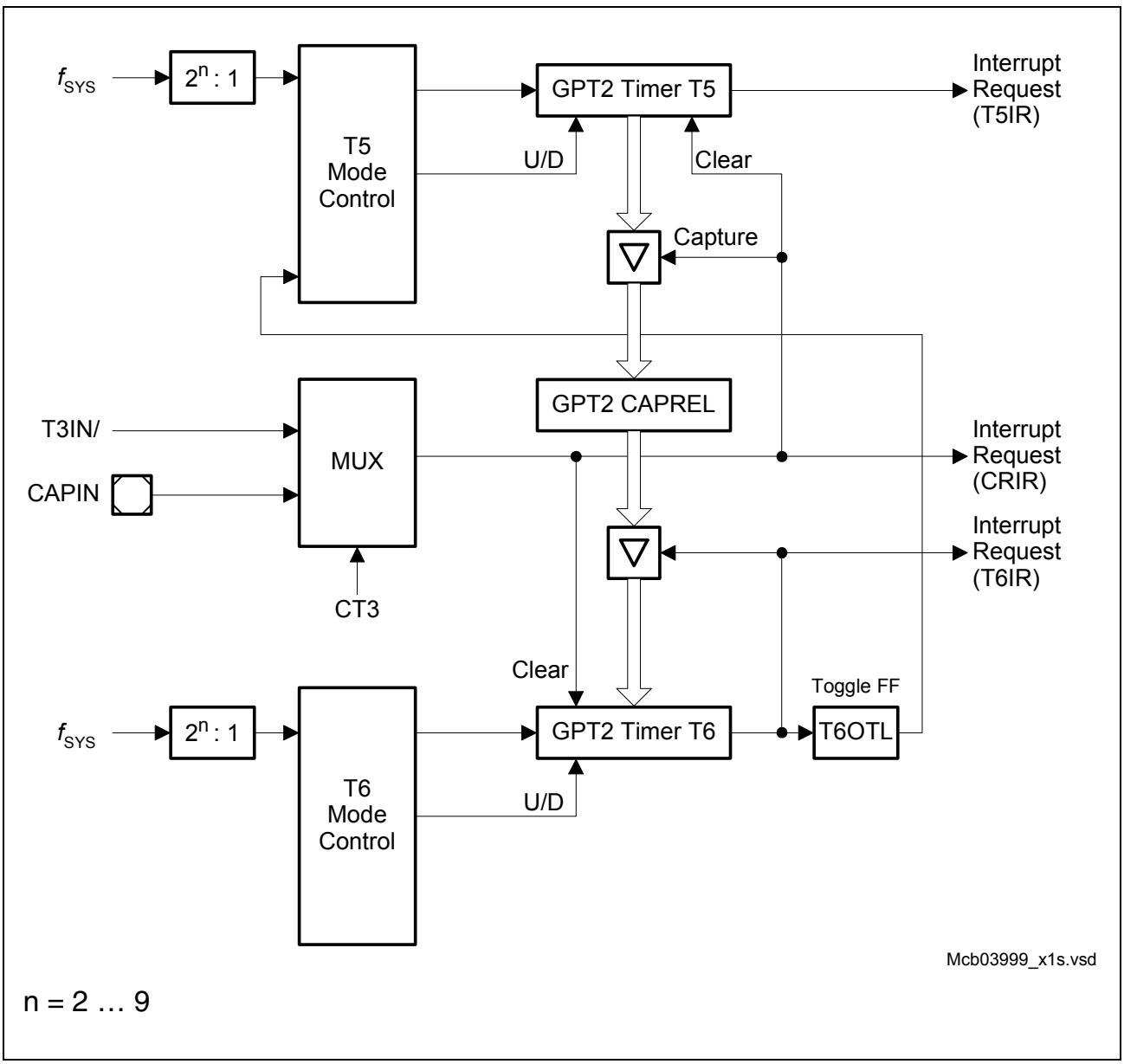

Figure 6 Block Diagram of GPT2

3.10 Power Management

The C161S provides several means to control the power it consumes either at a given time or averaged over a certain timespan. Three mechanisms can be used (partly in parallel):

- **Power Saving Modes** switch the C161S into a special operating mode (control via instructions).
  Idle Mode stops the CPU while the peripherals can continue to operate.
  Power Down Mode stops all clock signals and all operation (RTC may optionally continue running).
- **Clock Generation Management** controls the distribution and the frequency of internal and external clock signals (control via register SYSCON2).
  Slow Down Mode lets the C161S run at a CPU clock frequency of f_{OSC} / 1 … 32 (half for prescaler operation) which drastically reduces the consumed power. The PLL can be optionally disabled while operating in Slow Down Mode.
- **Peripheral Management** permits temporary disabling of peripheral modules (control via register SYSCON3).
  Each peripheral can separately be disabled/enabled. A group control option disables a major part of the peripheral set by setting one single bit.

The on-chip RTC supports intermittent operation of the C161S by generating cyclic wake-up signals. This offers full performance to quickly react on action requests while the intermittent sleep phases greatly reduce the average power consumption of the system.

Table 6 C161S Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
CP	$FE10_H$	08_H	CPU Context Pointer Register	$FC00_H$
CRIC **b**	$FF6A_H$	$B5_H$	GPT2 CAPREL Interrupt Ctrl. Reg.	0000_H
CSP	$FE08_H$	04_H	CPU Code Seg. Pointer Reg. (read only)	0000_H
DP0H **b**	$F102_H$ **E**	81_H	P0H Direction Control Register	00_H
DP0L **b**	$F100_H$ **E**	80_H	P0L Direction Control Register	00_H
DP1H **b**	$F106_H$ **E**	83_H	P1H Direction Control Register	00_H
DP1L **b**	$F104_H$ **E**	82_H	P1L Direction Control Register	00_H
DP2 **b**	$FFC2_H$	$E1_H$	Port 2 Direction Control Register	0000_H
DP3 **b**	$FFC6_H$	$E3_H$	Port 3 Direction Control Register	0000_H
DP4 **b**	$FFCA_H$	$E5_H$	Port 4 Direction Control Register	00_H
DP6 **b**	$FFCE_H$	$E7_H$	Port 6 Direction Control Register	00_H
DPP0	$FE00_H$	00_H	CPU Data Page Pointer 0 Reg. (10 bits)	0000_H
DPP1	$FE02_H$	01_H	CPU Data Page Pointer 1 Reg. (10 bits)	0001_H
DPP2	$FE04_H$	02_H	CPU Data Page Pointer 2 Reg. (10 bits)	0002_H
DPP3	$FE06_H$	03_H	CPU Data Page Pointer 3 Reg. (10 bits)	0003_H
EXICON **b**	$F1C0_H$ **E**	$E0_H$	External Interrupt Control Register	0000_H
IDCHIP	$F07C_H$ **E**	$3E_H$	Identifier	$05XX_H$
IDMANUF	$F07E_H$ **E**	$3F_H$	Identifier	1820_H
IDMEM	$F07A_H$ **E**	$3D_H$	Identifier	0000_H
IDMEM2	$F076_H$ **E**	$3B_H$	Identifier	0000_H
IDPROG	$F078_H$ **E**	$3C_H$	Identifier	0000_H
ISNC **b**	$F1DE_H$ **E**	EF_H	Interrupt Subnode Control Register	0000_H
MDC **b**	$FF0E_H$	87_H	CPU Multiply Divide Control Register	0000_H
MDH	$FE0C_H$	06_H	CPU Multiply Divide Reg. – High Word	0000_H
MDL	$FE0E_H$	07_H	CPU Multiply Divide Reg. – Low Word	0000_H
ODP2 **b**	$F1C2_H$ **E**	$E1_H$	Port 2 Open Drain Control Register	0000_H
ODP3 **b**	$F1C6_H$ **E**	$E3_H$	Port 3 Open Drain Control Register	0000_H
ODP6 **b**	$F1CE_H$ **E**	$E7_H$	Port 6 Open Drain Control Register	00_H
ONES **b**	$FF1E_H$	$8F_H$	Constant Value 1's Register (read only)	$FFFF_H$
P0H **b**	$FF02_H$	81_H	Port 0 High Reg. (Upper half of PORT0)	00_H

4 Electrical Parameters

4.1 Absolute Maximum Ratings

Table 7 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_J	-40	150	°C	under bias
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	-0.5	6.5	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	V_{DD} + 0.5	V	–
Input current on any pin during overload condition	I_{OV}	-10	10	mA	–
Absolute sum of all input currents during overload condition	$\Sigma\|I_{OV}\|$	–	100	mA	–
Power dissipation	P_{DISS}	–	1.5	W	–

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

4.2 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C161S. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 8 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Standard digital supply voltage	V_{DD}	4.5	5.5	V	Active mode, f_{CPUmax} = 25 MHz
		2.5[1)]	5.5	V	Power down mode
Reduced digital supply voltage	V_{DD}	3.0	3.6	V	Active mode, f_{CPUmax} = 20 MHz
		2.5[1)]	3.6	V	Power down mode
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	–	±5	mA	Per pin[2)3)]
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	–	50	mA	[3)]
External Load Capacitance	C_L	–	100	pF	–
Ambient temperature	T_A	0	70	°C	SAB-C161S …
		-40	85	°C	SAF-C161S …
		-40	125	°C	SAK-C161S …

1) Output voltages and output currents will be reduced when V_{DD} leaves the range defined for active mode.

2) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD}$ + 0.5 V or $V_{OV} < V_{SS}$ - 0.5 V). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltage must remain within the specified limits. Proper operation is not guaranteed if overload conditions occur on functional pins such as XTAL1, $\overline{RD}$, $\overline{WR}$, etc.

3) Not subject to production test, verified by design/characterization.

4.3 Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C161S and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the C161S will provide signals with the respective timing characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective timing characteristics to the C161S.

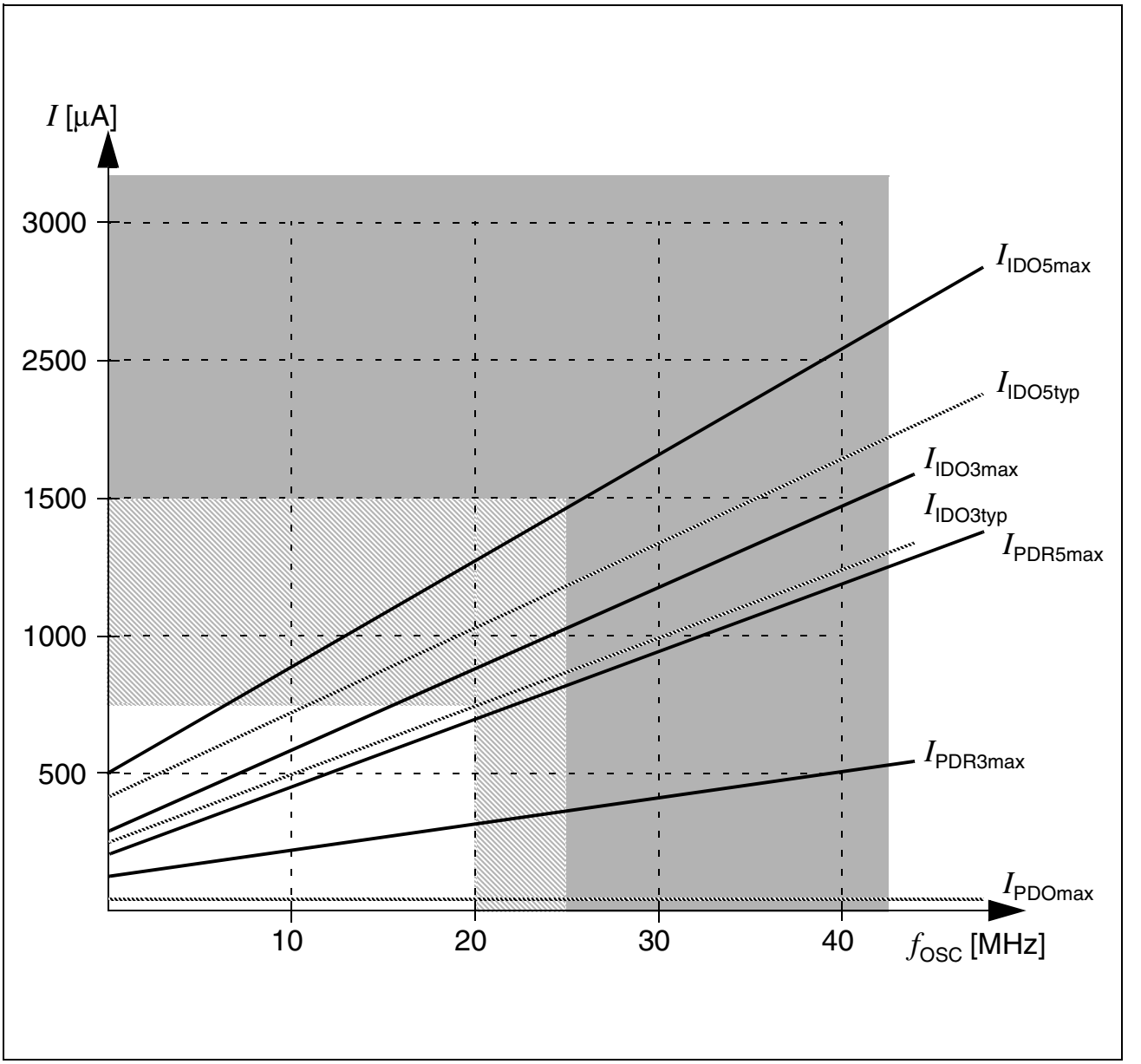

Figure 9 **Sleep and Power Down Supply Current as a Function of Oscillator Frequency**

The timings listed in the AC Characteristics that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances.

The actual minimum value for TCL depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCL is lower than for one single TCL (see formula and **Figure 11**).
For a period of **N** × TCL the minimum value is computed using the corresponding deviation D_N:

$$(\mathbf{N} \times \mathrm{TCL})_{min} = \mathbf{N} \times \mathrm{TCL}_{NOM} - D_N,\ D_N\ [\mathrm{ns}] = \pm(13.3 + \mathbf{N} \times 6.3) / f_{CPU}\ [\mathrm{MHz}] \quad (1)$$

where **N** = number of consecutive TCLs and $1 \le \mathbf{N} \le 40$.

So for a period of 3 TCLs @ 20 MHz (i.e. **N** = 3): $D_3 = (13.3 + \mathbf{3} \times 6.3) / 20 = 1.61$ ns, and $(3\mathrm{TCL})_{min} = 3\mathrm{TCL}_{NOM} - 1.61$ ns = 73.39 ns (@ f_{CPU} = 20 MHz).

This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

*Note: For all periods longer than 40 TCL the N = 40 value can be used (see **Figure 11**).*

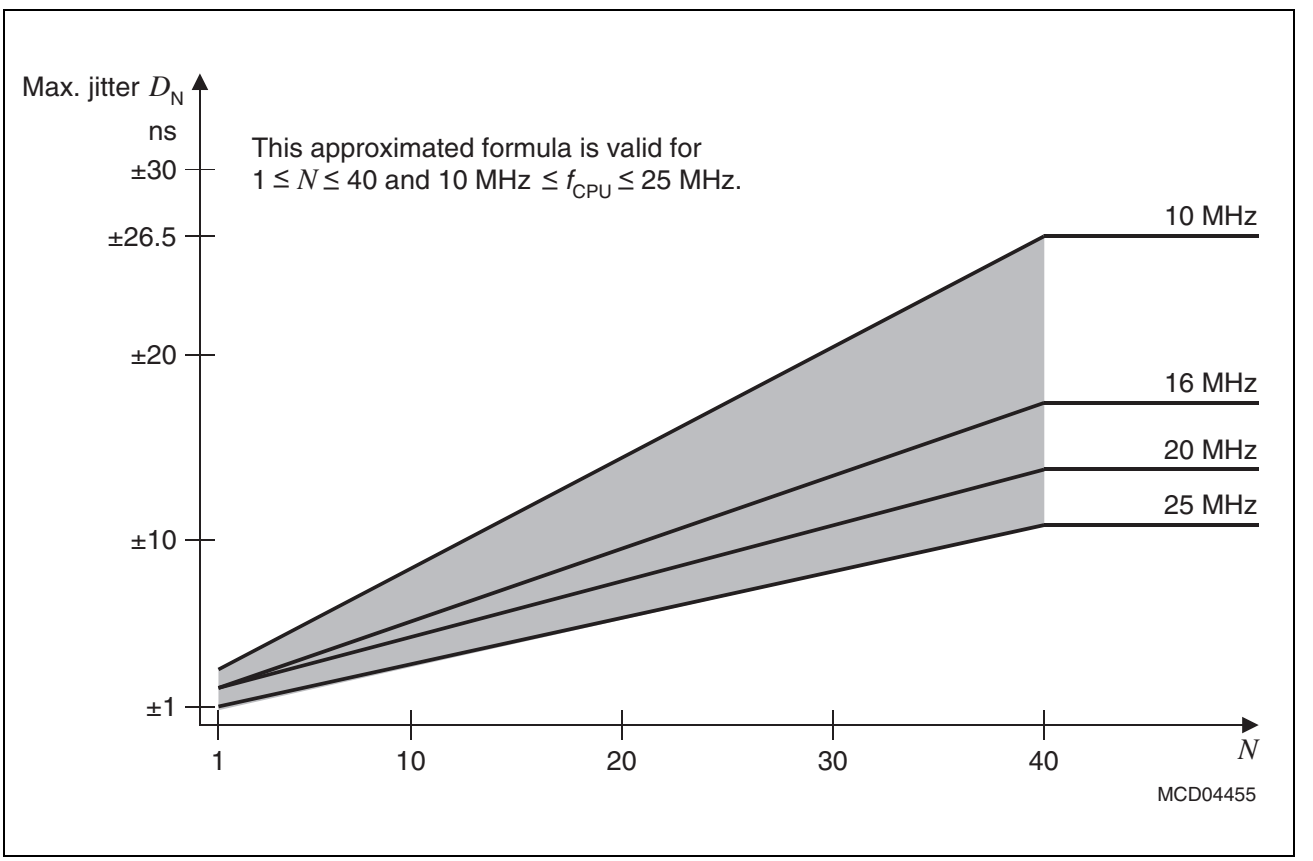

Figure 11 Approximated Maximum Accumulated PLL Jitter

Table 17 Multiplexed Bus (Reduced Supply Voltage Range) (cont'd)
(Operating Conditions apply)

ALE cycle time = 6 TCL + $2t_A + t_C + t_F$ (150 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			Min.	Max.	Min.	Max.	
Data valid to $\overline{WR}$	t_{22}	CC	24 + t_C	–	2TCL - 26 + t_C	–	ns
Data hold after $\overline{WR}$	t_{23}	CC	36 + t_F	–	2TCL - 14 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{25}	CC	36 + t_F	–	2TCL - 14 + t_F	–	ns
Address hold after $\overline{RD}$, $\overline{WR}$	t_{27}	CC	36 + t_F	–	2TCL - 14 + t_F	–	ns
ALE falling edge to $\overline{CS}$[1)]	t_{38}	CC	-8 - t_A	10 - t_A	-8 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In[1)]	t_{39}	SR	–	47 + t_C + $2t_A$	–	3TCL - 28 + t_C + $2t_A$	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$[1)]	t_{40}	CC	57 + t_F	–	3TCL - 18 + t_F	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{42}	CC	19 + t_A	–	TCL - 6 + t_A	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{43}	CC	-6 + t_A	–	-6 + t_A	–	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{44}	CC	–	0	–	0	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{45}	CC	–	25	–	TCL	ns
$\overline{RdCS}$ to Valid Data In (with RW delay)	t_{46}	SR	–	20 + t_C	–	2TCL - 30 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW delay)	t_{47}	SR	–	45 + t_C	–	3TCL - 30 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW delay)	t_{48}	CC	38 + t_C	–	2TCL - 12 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW delay)	t_{49}	CC	63 + t_C	–	3TCL - 12 + t_C	–	ns

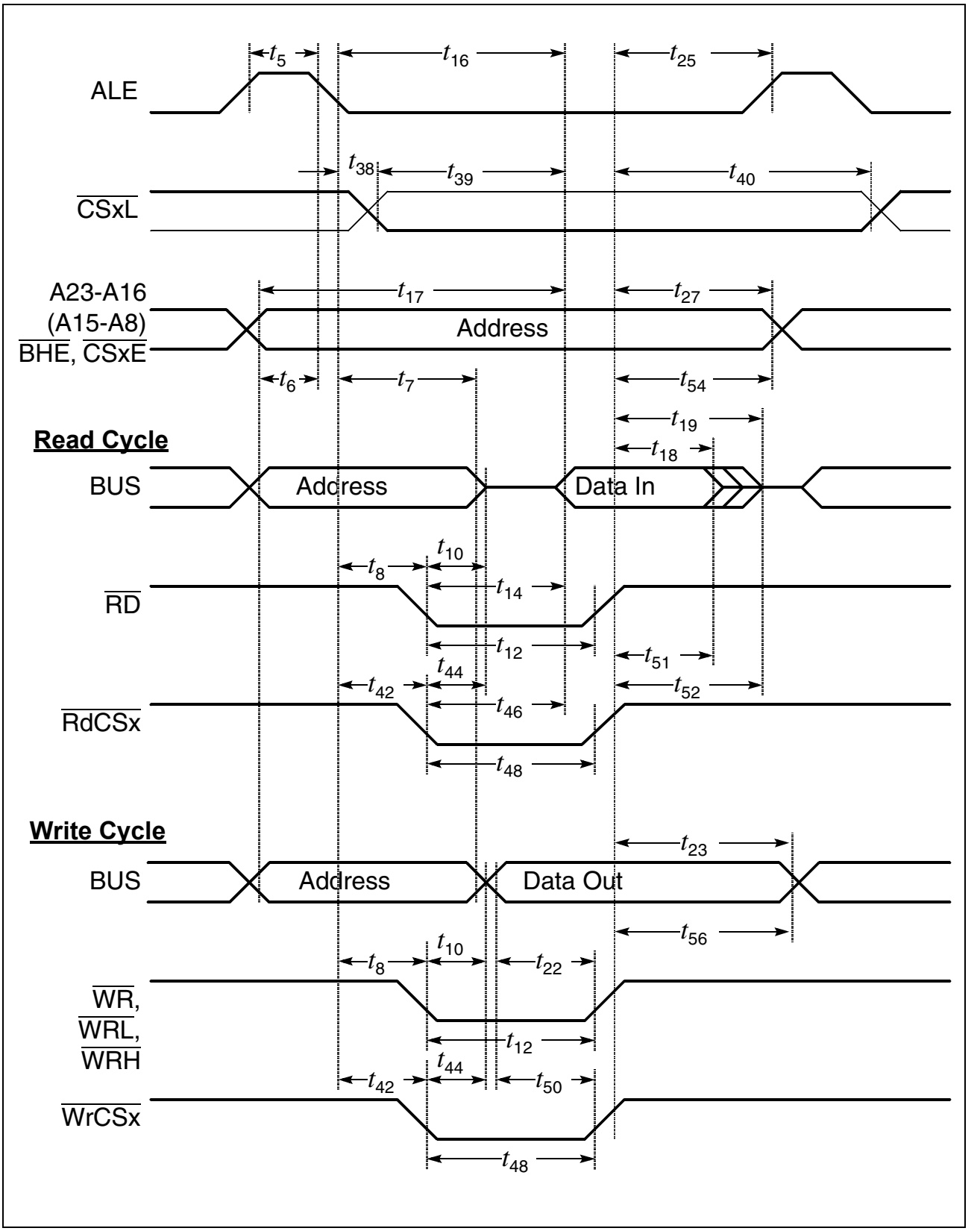

Figure 15 External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Normal ALE

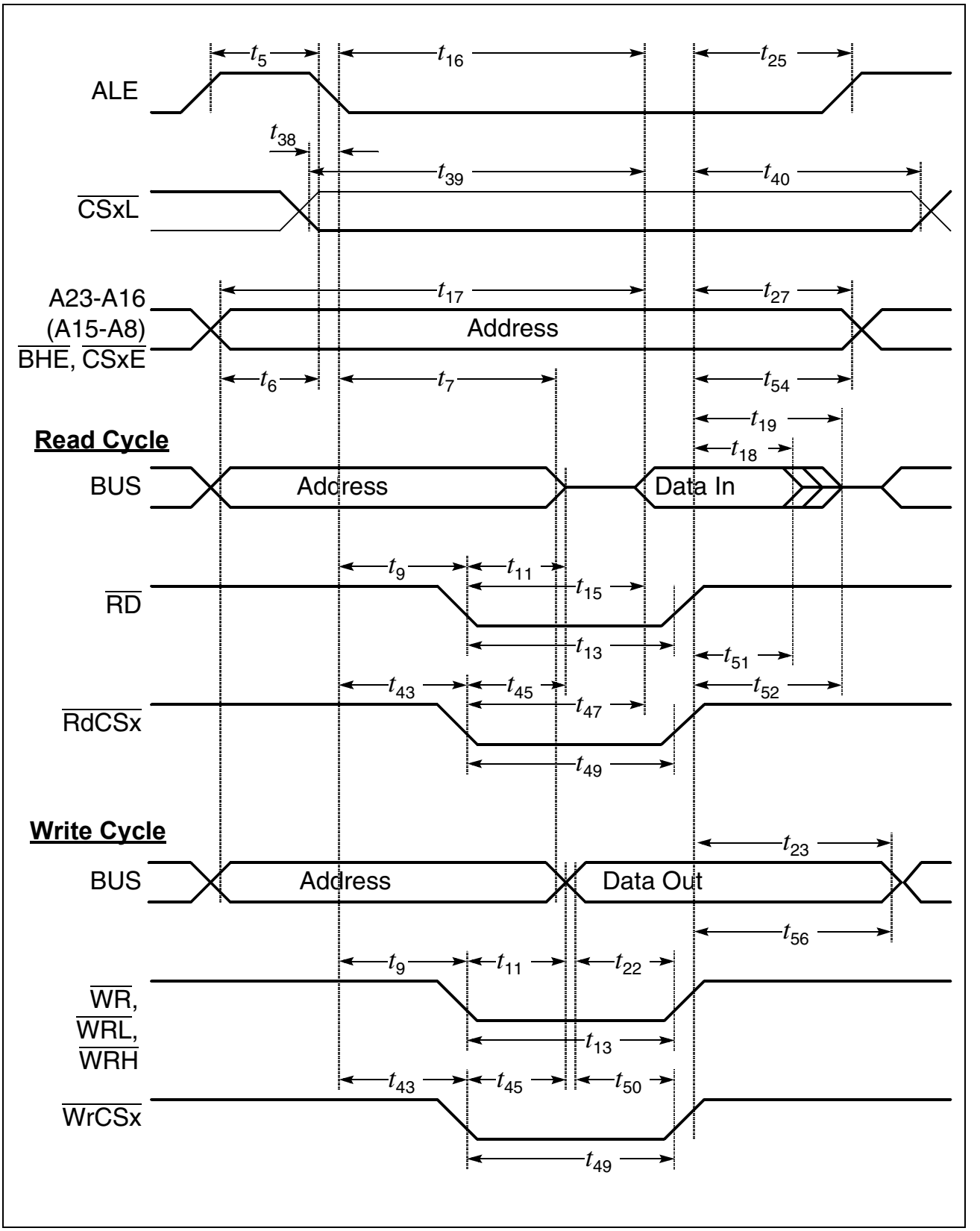

Figure 18 External Memory Cycle: Multiplexed Bus, No Read/Write Delay, Extended ALE

Table 19 Demultiplexed Bus (Reduced Supply Voltage Range)
(Operating Conditions apply)

ALE cycle time = 4 TCL + $2t_A + t_C + t_F$ (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			Min.	Max.	Min.	Max.	
ALE high time	t_5	CC	11 + t_A	–	TCL - 14 + t_A	–	ns
Address setup to ALE	t_6	CC	5 + t_A	–	TCL - 20 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	15 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	-10 + t_A	–	-10 + t_A	–	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	34 + t_C	–	2TCL - 16 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	59 + t_C	–	3TCL - 16 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	22 + t_C	–	2TCL - 28 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	47 + t_C	–	3TCL - 28 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	45 + t_A + t_C	–	3TCL - 30 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	57 + $2t_A$ + t_C	–	4TCL - 43 + $2t_A$ + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$ rising edge (with RW-delay[1)])	t_{20}	SR	–	36 + $2t_A$ + t_F[1)]	–	2TCL - 14 + $22t_A$ + t_F[1)]	ns
Data float after $\overline{RD}$ rising edge (no RW-delay[1)])	t_{21}	SR	–	15 + $2t_A$ + t_F[1)]	–	TCL - 10 + $22t_A$ + t_F[1)]	ns
Data valid to $\overline{WR}$	t_{22}	CC	24 + t_C	–	2TCL - 26 + t_C	–	ns

Table 19 Demultiplexed Bus (Reduced Supply Voltage Range) (cont'd)
(Operating Conditions apply)

ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			Min.	Max.	Min.	Max.	
Data float after $\overline{\text{RdCS}}$ (no RW-delay)[1]	t_{68}	SR	–	5 + t_F	–	TCL - 20 + $2t_A$ + t_F[1]	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{55}	CC	-16 + t_F	–	-16 + t_F	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{57}	CC	9 + t_F	–	TCL - 16 + t_F	–	ns

1) RW-delay and t_A refer to the next following bus cycle (including an access to an on-chip X-Peripheral).

2) Read data are latched with the same clock edge that triggers the address change and the rising $\overline{\text{RD}}$ edge. Therefore address changes before the end of $\overline{\text{RD}}$ have no impact on read cycles.

3) These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).

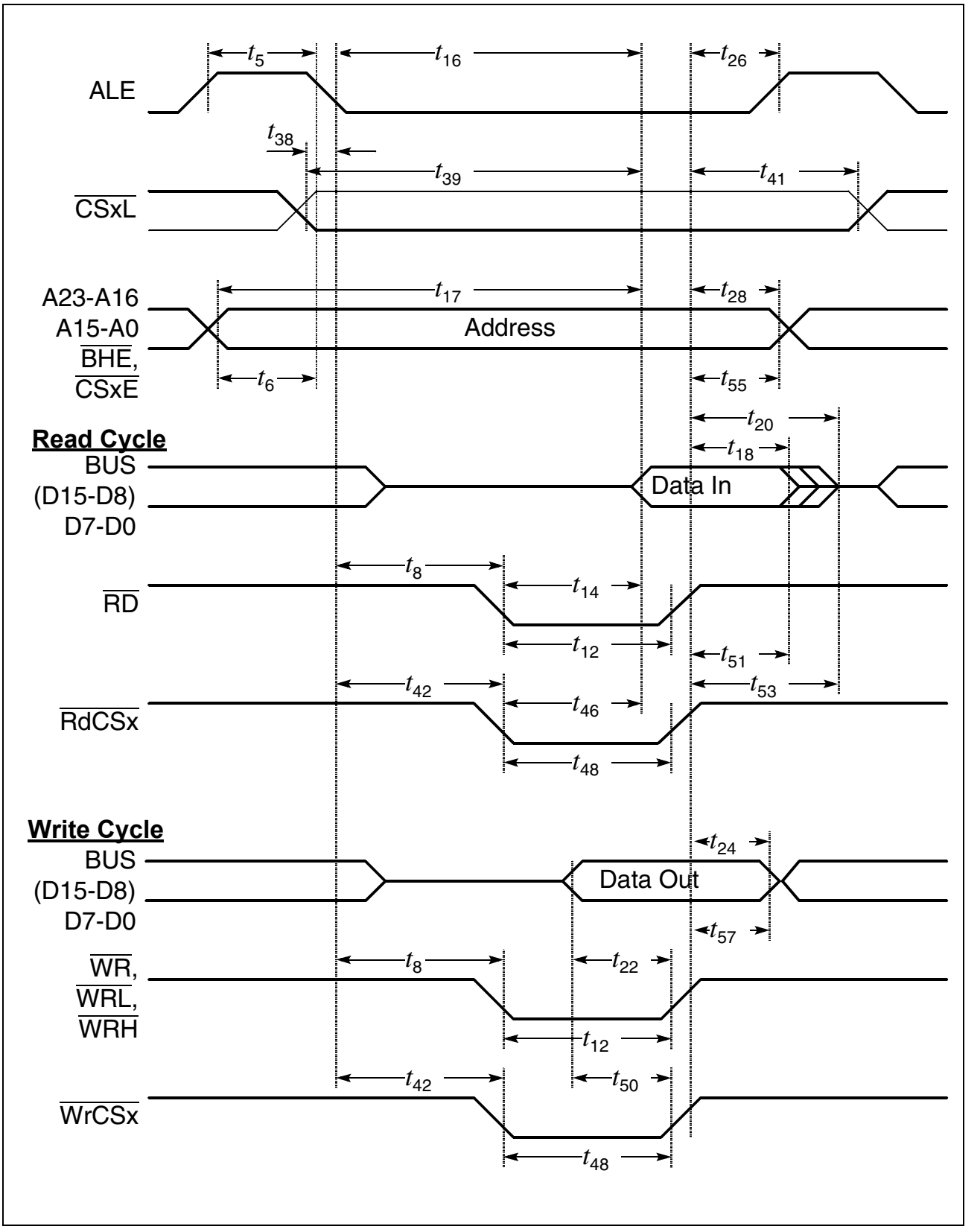

Figure 20 External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Extended ALE