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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z3
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5632mf1mlq60

  - Auxiliary Output port
    - 1 MCKO (message clock out) pin
    - 4 MDO (message data out) pins
    - 2 $\overline{\text{MSEO}}$ (message start/end out) pins
    - 1 $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port
    - 1 $\overline{\text{EVTI}}$ (event in) pin
- 17-pin Full Port interface in calibration package used on VertiCal boards
  - 3.3 V interface
  - Auxiliary Output port
    - 1 MCKO (message clock out) pin
    - 4 (reduced port mode) or 12 (full port mode) MDO (message data out) pins; 8 extra full port pins shared with calibration bus
    - 2 $\overline{\text{MSEO}}$ (message start/end out) pins
    - 1 $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port
    - 1 $\overline{\text{EVTI}}$ (event in) pin
- Host processor (e200) development support features
  - IEEE-ISTO 5001-2003 standard class 2 compliant
  - Program trace via branch trace messaging (BTM). Branch trace messaging displays program flow discontinuities (direct branches, indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus, static code may be traced.
  - Watchpoint trigger enable of program trace messaging
  - Data Value Breakpoints (JTAG feature of the e200z335 core): allows CPU to be halted when the CPU writes a specific value to a memory location
    - 4 data value breakpoints
    - CPU only
    - Detects ‘equal’ and ‘not equal’
    - Byte, half word, word (naturally aligned)

NOTE

This feature is imprecise due to CPU pipelining.

  - Subset of Power Architecture software debug facilities with OnCE block (Nexus class 1 features)
- eTPU development support features
  - IEEE-ISTO 5001-2003 standard class 1 compliant for the eTPU
  - Nexus based breakpoint configuration and single step support (JTAG feature of the eTPU)
- Run-time access to the on-chip memory map via the Nexus read/write access protocol. This feature supports accesses for run-time internal visibility, calibration variable acquisition, calibration constant tuning, and external rapid prototyping for powertrain automotive development systems.
- All features are independently configurable and controllable via the IEEE 1149.1 I/O port
- Power-on-reset status indication during reset via MDO[0] in disabled and reset modes

2.2.20.2 JTAG

The JTAGC (JTAG Controller) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001

3.5 208 MAPBGA ballmap (MPC5633M only)

Figure 6 shows the 208-pin MAPBGA ballmap for the MPC5633M (1024 KB flash memory) as viewed from above.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12-SDS	ALT_ MDO2	ALT_ MDO0	VRC33	VSS
B	VDD	VSS	AN38	AN21	AN0	AN4	REFBYPC	AN22	AN25	AN28	VDDA0	AN13-SDO	ALT_ MDO3	ALT_ MDO1	VSS	VDD
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14-SDI	AN15 FCK	VSS	ALT_ MSEO0	TCK
D	VRC33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH7	VSS	TMS	ALT_EVTO	NIC[1]
E	ETPUA30	ETPUA31	NC[2]	VDD									VDDE7	TDI	ALT_ EVTI	ALT_ MSEO1
F	ETPUA28	ETPUA29	ETPUA26	NC[2]									VDDEH6	TDO	ALT_MCKO	JCOMP
G	ETPUA24	ETPUA27	ETPUA25	ETPUA21			VSS	VSS	VSS	VSS			DSPI_B_ SOUT	DSPI_B_ PCS3	DSPI_B_ SIN	DSPI_B_ PCS0
H	ETPUA23	ETPUA22	ETPUA17	ETPUA18			VSS	VSS	VSS	VSS			NC[2]	DSPI_B_ PCS4	DSPI_B_ PCS2	DSPI_B_ PCS1
J	ETPUA20	ETPUA19	ETPUA14	ETPUA13			VSS	VSS	VSS	VSS			DSPI_B_ PCS5	SCI_A_TX	NC[2]	DSPI_B_ SCK
K	ETPUA16	ETPUA15	ETPUA7	VDDEH1			VSS	VSS	VSS	VSS			CAN_C_ TX	SCI_A_RX	RSTOUT	VDDREG
L	ETPUA12	ETPUA11	ETPUA6	ETPUA0									SCI_B_TX	CAN_C_ RX	WKPCFG	RESET
M	ETPUA10	ETPUA9	ETPUA1	ETPUA5									SCI_B_RX	PLLREF	BOOTCFG1	VSSPLL
N	ETPUA8	ETPUA4	ETPUA0	VSS	VDD	VRC33	EMIOS2	EMIOS10	VDDEH1/6[3]	EMIOS12	eTPUA19[4]	VRC33	VSS	VRCCTL	NIC[1]	EXTAL
P	ETPUA3	ETPUA2	VSS	VDD	NC[2]	VDDE7	NIC[1]	EMIOS8	eTPUA29[3]	eTPUA2[3]	eTPUA21[3]	CAN_A_ TX	VDD	VSS	NIC[1]	XTAL
R	NIC[1]	VSS	VDD	NC[2]	EMIOS4	NIC[1]	EMIOS9	EMIOS11	EMIOS14	eTPUA27[3]	EMIOS23	CAN_A_ RX	NC[2]	VDD	VSS	VDDPLL
T	VSS	VDD	NIC[1]	EMIOS0	NC[2]	GPIO219	eTPUA25[3]	NC[2]	NC[2]	eTPUA4[3]	eTPUA13[3]	NIC[1]	VDDE5	CLKOUT	VDD	VSS

1 Pins marked “NIC” have no internal connection.
2 Pins marked “NC” may be connected to internal circuitry. Connections to external circuits or other pins on this device can result in unpredictable system behavior or damage.
3 This ball may be changed to “NC” (no connection) in a future revision.
4 eTPU output only channel.

Figure 6. 208-pin MAPBGA ballmap (MPC5633M; top view)

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPBGA
CAL_ADDR[16][21] ALT_MDO[0][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	MDO / ALT_ADDR[12] / Low		—	17	A14
CAL_ADDR[17][21] ALT_MDO[1][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	ALT_MDO / CAL_ADDR[12] / Low		—	18	B14
CAL_ADDR[18][21] ALT_MDO[2][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	ALT_MDO / CAL_ADDR[12] / Low		—	19	A13
CAL_ADDR[19][21] ALT_MDO[3][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	ALT_MDO / CAL_ADDR[12] / Low		—	20	B13
CAL_ADDR[20:27] ALT_MDO[4:11]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] Fast	O / Low	ALT_MDO / CAL_ADDR[16] / Low		—	—	—
CAL_ADDR[28][21] ALT_$\overline{\text{MSEO}}$[0][12]	Calibration Address Bus Nexus Msg Start/End Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[17]	ALT_$\overline{\text{MSEO}}$[16] / CAL_ADDR[17]/ Low		—	118	C15
CAL_ADDR[29][21] ALT_$\overline{\text{MSEO}}$[1][12]	Calibration Address Bus Nexus Msg Start/End Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[17]	ALT_$\overline{\text{MSEO}}$[16] / CAL_ADDR[17]/ Low		—	117	E16
CAL_ADDR[30][21] ALT_$\overline{\text{EVTI}}$[12]	Calibration Address Bus Nexus Event In	PCR[345]	—	O I	VDDE12[13] VDDE7[14] Fast	—[18]	ALT_$\overline{\text{EVTI}}$ / CAL_ADDR[19]		—	116	E15
ALT_$\overline{\text{EVTO}}$	Nexus Event Out	PCR[344]	—	O	VDDE12[13] VDDE7[14] Fast	O / Low	ALT_$\overline{\text{EVTO}}$ / High		—	120	D15
ALT_MCKO	Nexus Msg Clock Out	PCR[344]	—	O	VDDE12[13] VDDE7[14] Fast	O / Low	ALT_MCKO / Enabled		—	14	F15
NEXUSCFG[11]	Nexus/Calibration bus selector	—	—	I	VDDE12 Fast	I / Down	NEXUSCFG / Down		—	—	—
CAL_$\overline{\text{CS}}$[0][11]	Calibration Chip Selects	PCR[336]	—	O	VDDE12 Fast	O / High	CAL_$\overline{\text{CS}}$ / High		—	—	—
CAL_$\overline{\text{CS}}$[2][11] CAL_ADDR[10]	Calibration Chip Selects Calibration Address Bus	PCR[338]	11 10	O O	VDDE12 Fast	O / High	CAL_$\overline{\text{CS}}$ / High		—	—	—

3.7 Signal details

Table 4 contains details on the multiplexed signals that appear in Table 2, “MPC563xM signal properties”.

Table 4. Signal details

Signal	Module or Function	Description
CLKOUT	Clock Generation	MPC5634M clock output for the external/calibration bus interface
EXTAL	Clock Generation	Input pin for an external crystal oscillator or an external clock source based on the value driven on the PLLREF pin at reset.
EXTCLK	Clock Generation	External clock input
PLLREF	Clock Generation	PLLREF is used to select whether the oscillator operates in xtal mode or external reference mode from reset. PLLREF=0 selects external reference mode.
XTAL	Clock Generation	Crystal oscillator input
SCK_B_LVDS– SCK_B_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission
SOUT_B_LVDS– SOUT_B_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission
SCK_C_LVDS– SCK_C_LVDS+	DSPI	LVDS pair used for DSPI_C TSB mode transmission
SOUT_C_LVDS– SOUT_C_LVDS+	DSPI	LVDS pair used for DSPI_C TSB mode transmission
PCS_B[0] PCS_C[0]	DSPI_B – DSPI_C	Peripheral chip select when device is in master mode—slave select when used in slave mode
PCS_B[1:5] PCS_C[1:5]	DSPI_B – DSPI_C	Peripheral chip select when device is in master mode—not used in slave mode
SCK_B SCK_C	DSPI_B – DSPI_C	DSPI clock—output when device is in master mode; input when in slave mode
SIN_B SIN_C	DSPI_B – DSPI_C	DSPI data in
SOUT_B SOUT_C	DSPI_B – DSPI_C	DSPI data out
CAL_ADDR[12:30]	Calibration Bus	The CAL_ADDR[12:30] signals specify the physical address of the bus transaction.
CAL_$\overline{\text{CS}}$[0:3]	Calibration Bus	$\overline{\text{CS}}$x is asserted by the master to indicate that this transaction is targeted for a particular memory bank on the Primary external bus.
CAL_DATA[0:15]	Calibration Bus	The CAL_DATA[0:15] signals contain the data to be transferred for the current transaction.
CAL_$\overline{\text{OE}}$	Calibration Bus	$\overline{\text{OE}}$ is used to indicate when an external memory is permitted to drive back read data. External memories must have their data output buffers off when $\overline{\text{OE}}$ is negated. $\overline{\text{OE}}$ is only asserted for chip-select accesses.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 3}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)
$R_{\theta JC}$ = junction-to-case thermal resistance ($^oC/W$)
$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 4}$$

where:

T_T = thermocouple temperature on top of the package (^oC)
Ψ_{JT} = thermal characterization parameter ($^oC/W$)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134
USA
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the web at http://www.jedec.org.

- C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
- G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications”, Electronic Packaging and Production, pp. 53-58, March 1998.

Table 22. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
V_{IL_LS}	CC	C	Multi-voltage pad I/O input low voltage in low-swing mode[10,11,12,13]	Hysteresis enabled	V_{SS}–0.3	—	0.8	V
		P		Hysteresis disabled	V_{SS}–0.3	—	1.1	
V_{IL_HS}	CC	C	Multi-voltage pad I/O input low voltage in high-swing mode	Hysteresis enabled	V_{SS}–0.3	—	0.35 V_{DDEH}	V
		P		Hysteresis disabled	V_{SS}–0.3	—	0.4 V_{DDEH}	
V_{IH_S}	CC	C	Slow/medium pad I/O input high voltage	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH}+0.3	V
		P		hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH}+0.3	
V_{IH_F}	CC	C	Fast pad I/O input high voltage	Hysteresis enabled	0.65 V_{DDE}	—	V_{DDE}+0.3	V
		P		hysteresis disabled	0.55 V_{DDE}	—	V_{DDE}+0.3	
V_{IH_LS}	CC	C	Multi-voltage pad I/O input high voltage in low-swing mode[10,11,12,13,14]	Hysteresis enabled	2.5	—	V_{DDEH}+0.3	V
		P		Hysteresis disabled	2.2	—	V_{DDEH}+0.3	
V_{IH_HS}	CC	C	Multi-voltage pad I/O input high voltage in high-swing mode[15]	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH}+0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH}+0.3	
V_{OL_S}	CC	P	Slow/medium multi-voltage pad I/O output low voltage[18,16]	—	—	—	0.2*V_{DDEH}	V
V_{OL_F}	CC	P	Fast pad I/O output low voltage[17,18]	—	—	—	0.2*V_{DDE}	V
V_{OL_LS}	CC	P	Multi-voltage pad I/O output low voltage in low-swing mode[10,11,12,13,17]	I_{OL} = 2 mA	—	—	0.6	V
V_{OL_HS}	CC	P	Multi-voltage pad I/O output low voltage in high-swing mode[17]	—	—	—	0.2 V_{DDEH}	V
V_{OH_S}	CC	P	Slow/medium pad I/O output high voltage[18,16]	—	0.8 V_{DDEH}	—	—	V
V_{OH_F}	CC	P	Fast pad I/O output high voltage[17,18]	—	0.8 V_{DDE}	—	—	V

Table 22. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
V_{OH_LS}	CC	P	Multi-voltage pad I/O output high voltage in low-swing mode[10,11,12,13,17]	I_{OH_LS} = 0.5 mA Min V_{DDEH} = 4.75 V	2.1	—	3.7	V
V_{OH_HS}	CC	P	Multi-voltage pad I/O output high voltage in high-swing mode[17]	—	0.8 V_{DDEH}	—	—	V
V_{HYS_S}	CC	C	Slow/medium/multi-voltage I/O input hysteresis	—	0.1 * V_{DDEH}	—	—	V
V_{HYS_F}	CC	C	Fast I/O input hysteresis	—	0.1 * V_{DDE}	—	—	V
V_{HYS_LS}	CC	C	Low-Swing-Mode Multi-Voltage I/O Input Hysteresis	hysteresis enabled	0.25	—	—	V
I_{DD}+I_{DDPLL}[19]	CC	P	Operating current 1.2 V supplies	V_{DD} = 1.32 V, 80 MHz	—	—	195	mA
	CC	P		V_{DD} = 1.32 V, 60 MHz	—	—	135	
	CC	P		V_{DD} = 1.32 V, 40 MHz	—	—	98	
I_{DDSTBY}	CC	T	Operating current 1 V supplies	T_J = 25 °C	—	—	80	µA
	CC	T		T_J = 55 °C	—	—	100	µA
$I_{DDSTBY150}$	CC	P	Operating current	T_J=150 °C	—	—	700	µA
I_{DDSLOW} I_{DDSTOP}	CC	P	V_{DD} low-power mode operating current @ 1.32 V	Slow mode[20]	—	—	50	mA
		C		Stop mode[21]	—	—	50	
I_{DD33}	CC	T	Operating current 3.3 V supplies @ 80 MHz	V_{RC33}[4,22]	—	—	70	mA
I_{DDA} I_{REF} I_{DDREG}	CC	P	Operating current 5.0 V supplies @ 80 MHz	V_{DDA}	—	—	30	mA
		P		Analog reference supply current	—	—	1.0	
		C		V_{DDREG}	—	—	70	

[8] V_{FLASH} is only available in the calibration package.

[9] Regulator is functional, with derated performance, with supply voltage down to 4.0 V.

[10] Multi-voltage pads (type pad_multv_hv) must be supplied with a power supply between 4.75 V and 5.25 V.

[11] The slew rate (SRC) setting must be 0b11 when in low-swing mode.

[12] While in low-swing mode there are no restrictions in transitioning to high-swing mode.

[13] Pin in low-swing mode can accept a 5 V input.

[14] Values are pending characterization.

[15] Pin in low-swing mode can accept a 5 V input.

[16] Characterization based capability:

IOH_S = {6, 11.6} mA and IOL_S = {9.2, 17.7} mA for {slow, medium} I/O with VDDEH=4.5 V;
IOH_S = {2.8, 5.4} mA and IOL_S = {4.2, 8.1} mA for {slow, medium} I/O with VDDEH=3.0 V

[17] Characterization based capability:

IOH_F = {12, 20, 30, 40} mA and IOL_F = {24, 40, 50, 65} mA for {00, 01,10, 11} drive mode with VDDE=3.0 V;
IOH_F = {7, 13, 18, 25} mA and IOL_F = {18, 30, 35, 50} mA for {00, 01, 10, 11} drive mode with VDDE=2.25 V;
IOH_F = {3, 7, 10, 15} mA and IOL_F = {12, 20, 27, 35} mA for {00, 01, 10, 11} drive mode with VDDE=1.62 V

[18] All VOL/VOH values 100% tested with ± 2 mA load.

[19] Run mode as follows:

System clock = 40/60/80 MHz + FM 2%
Code executed from flash memory
ADC0 at 16 MHz with DMA enabled
ADC1 at 8 MHz
eMIOS pads toggle in PWM mode with a rate between 100 kHz and 500 kHz
eTPU pads toggle in PWM mode with a rate between 10 kHz and 500 kHz
CAN configured for a bit rate of 500 kHz
DSPI configured in master mode with a bit rate of 2 MHz
eSCI transmission configured with a bit rate of 100 kHz

[20] Bypass mode, system clock at 1 MHz (using system clock divider), PLL shut down, CPU running simple executive code, 4 x ADC conversion every 10 ms, 2 × PWM channels at 1 kHz, all other modules stopped.

[21] Bypass mode, system clock at 1 MHz (using system clock divider), CPU stopped, PIT running, all other modules stopped.

[22] When using the internal regulator only, a bypass capacitor should be connected to this pin. External circuits should not be powered by the internal regulator. The internal regulator can be used as a reference for an external debugger.

[23] Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. See Table 23 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.

[24] Absolute value of current, measured at V_{IL} and V_{IH}.

[25] Weak pull up/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to pad types: fast (pad_fc).

[26] Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 ^{o}C, in the ambient temperature range of 50 to 125 ^{o}C. Applies to pad types: pad_a and pad_ae.

[27] Applies to CLKOUT, external bus pins, and Nexus pins.

[28] Applies to the FCK, SDI, SDO, and $\overline{SDS}$ pins.

[29] This programmable option applies only to eQADC differential input channels and is used for biasing and sensor diagnostics.

[30] When the pull-up and pull-down of the same nominal 200 KΩ or 100 KΩ value are both enabled, assuming no interference from external devices, the resulting pad voltage will be 0.5*V_{DDE} ± 2.5%

Table 25. V_{RC33} pad average DC current[1]

Pad Type	Symbol		C	Period (ns)	Load[2] (pF)	V_{RC33} (V)	V_{DDE} (V)	Drive Select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Fast	I_{DRV_FC}	CC	D	10	50	3.6	3.6	11	2.35	6.12
		CC	D	10	30	3.6	3.6	10	1.75	4.3
		CC	D	10	20	3.6	3.6	01	1.41	3.43
		CC	D	10	10	3.6	3.6	00	1.06	2.9
		CC	D	10	50	3.6	1.98	11	1.75	4.56
		CC	D	10	30	3.6	1.98	10	1.32	3.44
		CC	D	10	20	3.6	1.98	01	1.14	2.95
		CC	D	10	10	3.6	1.98	00	0.95	2.62

1 These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

2 All loads are lumped.

4.9.2 LVDS pad specifications

LVDS pads are implemented to support the MSC (Microsecond Channel) protocol which is an enhanced feature of the DSPI module. The LVDS pads are compliant with LVDS specifications and support data rates up to 50 MHz.

Table 26. DSPI LVDS pad specification [1, 2]

#	Characteristic	Symbol	C		Condition	Min. Value	Typ. Value	Max. Value	Unit
Data Rate									
4	Data Frequency	$F_{LVDSCLK}$	CC	D			50		MHz
Driver Specs									
5	Differential output voltage	V_{OD}[3]	CC	P	SRC=0b00 or 0b11	150		430	mV
			CC	P	SRC=0b01	90		340	
			CC	P	SRC=0b10	155		480	
6	Common mode voltage (LVDS), V_{OS}	V_{OS}[3]	CC	P		0.8	1.2	1.6	V
7	Rise/Fall time	T_R/T_F	CC	D			2		ns
8	Propagation delay (Low to High)	T_{PLH}	CC	D			4		ns
9	Propagation delay (High to Low)	T_{PHL}	CC	D			4		ns
10	Delay (H/L), sync Mode	t_{PDSYNC}	CC	D			4		ns
11	Delay, Z to Normal (High/Low)	T_{DZ}	CC	D			500		ns

[4] Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

[5] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA} + 0.5$ V and $V_{NEGCLAMP} = – 0.3$ V, then use the larger of the calculated values.

[6] Condition applies to two adjacent pins at injection limits.

[7] Performance expected with production silicon.

[8] All channels have same 10 kΩ < Rs < 100 kΩ; Channel under test has Rs=10 kΩ; I_{INJ}=I_{INJMAX},I_{INJMIN}.

[9] TUE is tested by averaging 10 samples.

[10] TUE is tested by averaging three samples.

[11] These values can be significantly improved by using three samples of averaging. Input frequency of 1 kHz was used as the reference for the Signal to Noise Ratio.

[12] Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed by as indicated.

[13] At $V_{RH} – V_{RL} = 5.12$ V, one LSB = 1.25 mV.

[14] Guaranteed 10-bit monotonicity.

[15] Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

4.13 Platform flash controller electrical characteristics

Table 30. APC, RWSC, WWSC settings vs. frequency of operation[1]

Target Max Frequency (MHz)	APC[2]	RWSC[2]	WWSC
21[3]	000	000	01
41[3]	001	001	01
62[3]	010	010	01
82[3]	011	011	01
All	111	111	111

1 Illegal combinations exist, all entries must be taken from the same row

2 APC must be equal to RWSC

3 Maximum Frequency includes FM modulation

4.14 Flash memory electrical characteristics

Table 31. Program and erase specifications

Symbol		Parameter	Min Value	Typical Value[1]	Initial Max[2]	Max[3]	Unit
$T_{dwprogram}$	P	Double Word (64 bits) Program Time[4]	—	22	50	500	µs
$T_{16kpperase}$	P	16 KB Block Pre-program and Erase Time	—	300	500	5000	ms
$T_{32kpperase}$	P	32 KB Block Pre-program and Erase Time	—	400	600	5000	ms
$T_{64kpperase}$	P	64 KB Block Pre-program and Erase Time	—	600	900	5000	ms
$T_{128kpperase}$	P	128 KB Block Pre-program and Erase Time	—	800	1300	7500	ms

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program & erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

Table 32. Flash module life

Symbol		Parameter	Conditions	Value		Unit
				Min	Typ	
P/E	C	Number of program/erase cycles per block for 16 Kbyte blocks over the operating temperature range (T_J)	—	100,000	—	cycles
P/E	C	Number of program/erase cycles per block for 32 and 64 Kbyte blocks over operating temperature range (T_J)	—	10,000	100,000	cycles
P/E	C	Number of program/erase cycles per block for 128 Kbyte blocks over the operating temperature range (T_J)	—	1,000	100,000	cycles
Retention	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0 – 1,000 P/E cycles	20	—	years
			Blocks with 10,000 P/E cycles	10	—	years
			Blocks with 100,000 P/E cycles	5	—	years

[1] Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

4.15 AC specifications

4.15.1 Pad AC specifications

Table 33. Pad AC specifications (5.0 V)[1,2]

Name		C	Output Delay (ns)[3,4] Low-to-High / High-to-Low		Rise/Fall Edge ( )[4,5]		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium[6,7,8]	CC	D	4.6/3.7	12/12	2.2/2.2	7/7	50	11[9]
	CC	D	13/10	32/32	9/9	22/22	200	
	N/A							10[10]
	CC	D	12/13	28/34	5.6/6	15/15	50	01
	CC	D	23/23	52/59	11/14	31/31	200	
	CC	D	69/71	152/165	34/35	74/74	50	00
	CC	D	95/90	205/220	44/51	96/96	200	
Slow[8,11]	CC	D	7.3/5.7	19/18	4.4/4.3	14/14	50	11[9]
	CC	D	24/19	58/58	17/15	42/42	200	
	N/A							10[10]
	CC	D	26/27	61/69	13/13	34/34	50	01
	CC	D	49/45	115/115	27/23	61/61	200	
	CC	D	137/142	320/330	72/74	164/164	50	00
	CC	D	182/172	420/420	90/85	200/200	200	
MultiV[12] (High Swing Mode)	CC	D	4.1/3.6	10.3/8.9	3.28/2.98	8/8	50	11[9]
	CC	D	10.4/10.2	24.2/23.6	12.7/11.54	29/29	200	
	N/A							10[10]
	CC	D	8.38/6.11	16/12.9	5.48/4.81	11/11	50	01
	CC	D	15.9/13.6	31/28.5	14.6/13.1	31/31	200	
	CC	D	61.7/10.4	92.2/24.3	42.0/12.2	63/63	50	00
	CC	D	85.5/37.3	132.6/ 78.9	57.7/46.4	85/85	200	
MultiV (Low Swing Mode)	CC	D	2.31/2.34	7.62/6.33	1.26/1.67	7/7	30	11[9]
Fast[13]	N/A							
pad_i_hv[14]	CC	D	0.5/0.5	1.9/1.9	0.3/0.3	1.5/1.5	0.5	N/A
pull_hv	CC	D	NA	6000	—	5000/5000	50	N/A

1 These are worst case values that are estimated from simulation and not tested. Values in the table are simulated at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDE} = 1.62 V to 1.98 V, V_{DDEH} = 4.5 V to 5.25 V, $T_A = T_L$ to T_H.

2 TBD: To Be Defined.

Table 37. Nexus debug port timing[1] (continued)

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
9	t_{TCYC}	CC	D	TCK Cycle Time	4[6,7]	—	t_{CYC}
9a	t_{TCYC}	CC	D	Absolute Minimum TCK Cycle Time	100[8]	—	ns
10	t_{TDC}	CC	D	TCK Duty Cycle	40	60	%
11	t_{NTDIS}	CC	D	TDI Data Setup Time	5	—	ns
12	t_{NTDIH}	CC	D	TDI Data Hold Time	25	—	ns
13	t_{NTMSS}	CC	D	TMS Data Setup Time	5	—	ns
14	t_{NTMSH}	CC	D	TMS Data Hold Time	25	—	ns
15	t_{JOV}	CC	D	TCK Low to TDO Data Valid	10	20	ns

1 All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.25 V with multi-voltage pads programmed to Low-Swing mode, T_A = TL to TH, and CL = 30 pF with DSC = 0b10.

2 Achieving the absolute minimum MCKO cycle time may require setting the MCKO divider to more than its minimum setting (NPC_PCR[MCKO_DIV] depending on the actual system frequency being used.

3 This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum MCKO period specification.

4 This may require setting the MCKO divider to more than its minimum setting (NPC_PCR[MCKO_DIV]) depending on the actual system frequency being used.

5 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

6 Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

7 This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.

8 This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

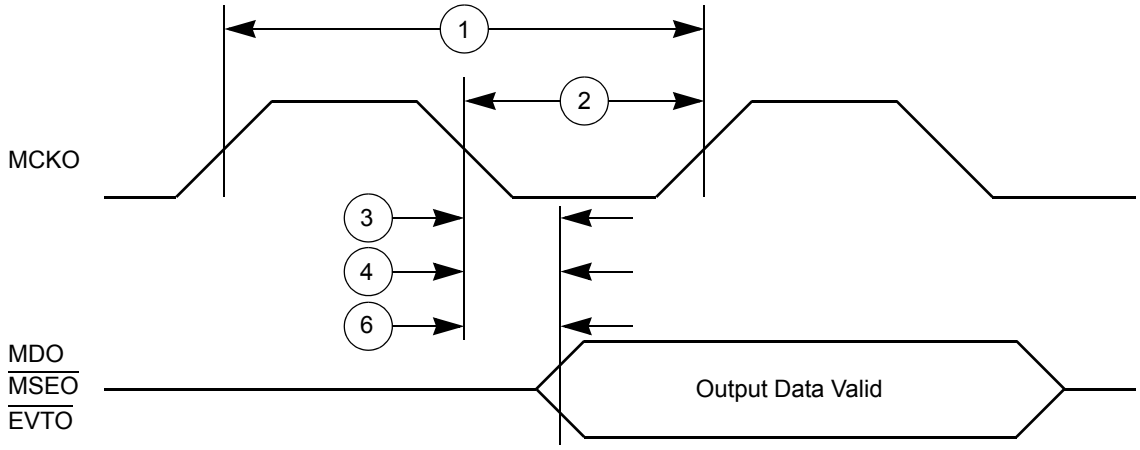

Figure 13. Nexus output timing

5 Packages

5.1 Package mechanical data

5.1.1 144 LQFP

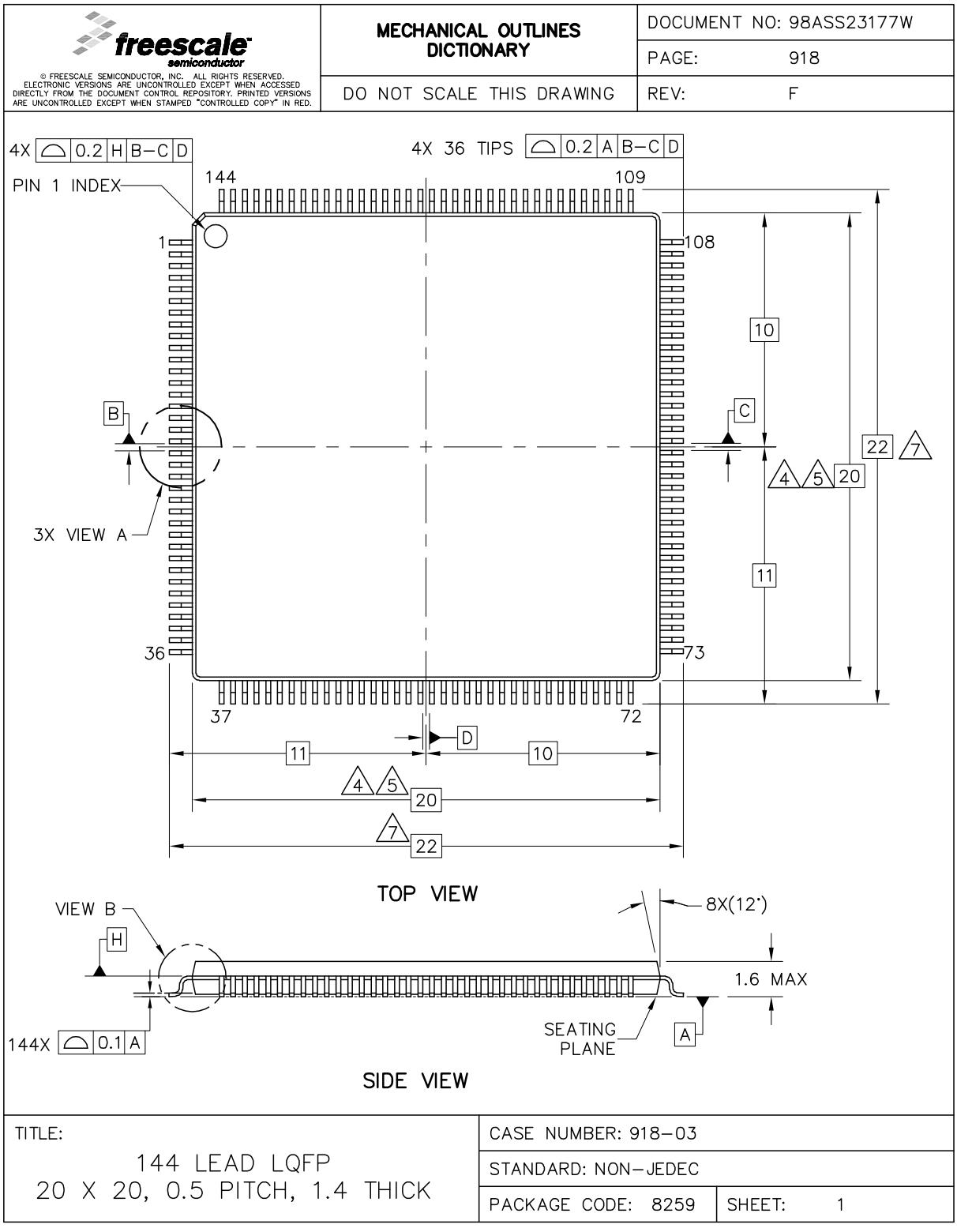

Figure 30. 144 LQFP package mechanical drawing (part 1)

5.1.2 176 LQFP

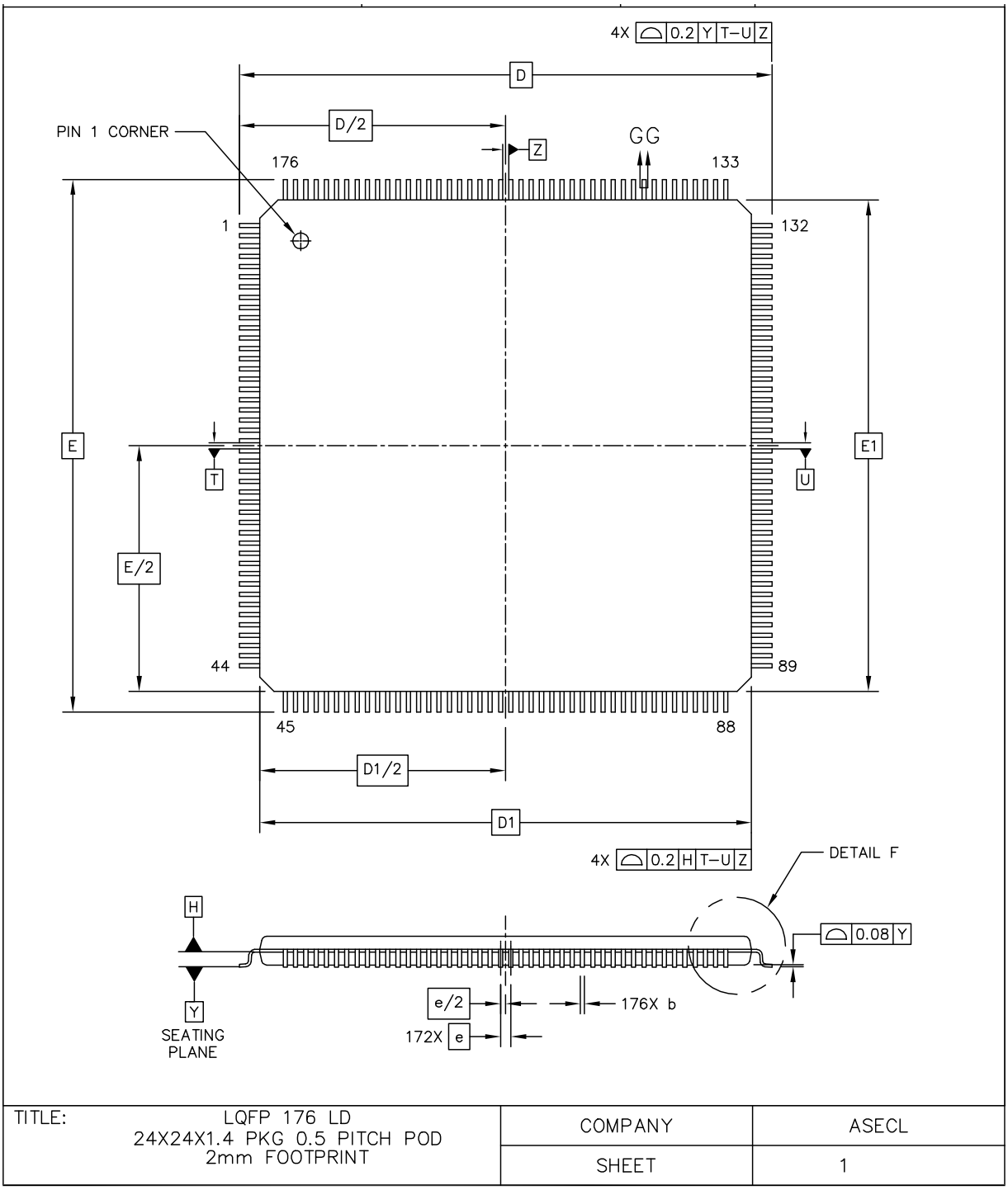

Figure 33. 176 LQFP package mechanical drawing (part 1)

6 Ordering information

Table 42 shows the orderable part numbers for the MPC5634M series.

Table 42. Orderable part number summary

Part Number	Flash/SRAM (Kbytes)	Package	Speed (MHz)
SPC5632MF2MLQ60	768 / 48	144 LQFP Pb-free	60
SPC5632MF2MLQ40	768 / 48	144 LQFP Pb-free	40
SPC5633MF2MMG80	1024 / 64	208 MAPBGA Pb-free	80
SPC5633MF2MLU80	1024 / 64	176 LQFP Pb-free	80
SPC5633MF2MLQ80	1024 / 64	144 LQFP Pb-free	80
SPC5633MF2MMG60	1024 / 64	208 MAPBGA Pb-free	60
SPC5633MF2MLU60	1024 / 64	176 LQFP Pb-free	60
SPC5633MF2MLQ60	1024 / 64	144 LQFP Pb-free	60
SPC5633MF2MLQ40	1024 / 64	144 LQFP Pb-free	40
SPC5634MF2MMG80	1536 / 94	208 MAPBGA Pb-free	80
SPC5634MF2MLU80	1536 / 94	176 LQFP Pb-free	80
SPC5634MF2MLQ80	1536 / 94	144 LQFP Pb-free	80
SPC5634MF2MMG60	1536 / 94	208 MAPBGA Pb-free	60
SPC5634MF2MLU60	1536 / 94	176 LQFP Pb-free	60
SPC5634MF2MLQ60	1536 / 94	144 LQFP Pb-free	60
SPC563M60L3CPBY			
SPC563M60L3CPAY			

Table 43. Revision history (continued)

Revision	Date	Description of Changes
Rev. 5	04/2010	Updates to features list: • MMU is 16-entry (previously noted as 8-entry) • ECSM features include single-bit error correction reporting • eTPU2 is object code compatible with previous eTPU versions Updates to feature details: • Programming feature: eTPU2 channel flags can be tested Pinout/ballmap changes: 144 pin LQFP package: • Pin 46 is now VDDEH1B (was VDDEH4A) • Pin 61 is now VDDEH6A (was VDDEH4B) 176 pin LQFP package (1.5M devices) • Pin 55 is now VDDEH1B (was VDDEH4A) • Pin 74 is now VDDEH6A (was VDDEH4B) 176 pin LQFP package (1.5M devices) • Pin 55 is now VDDEH1B (was VDDEH4A) • Pin 74 is now VDDEH6A (was VDDEH4B) 208 ball BGA package (all devices) Ball N9 changed to VDDEH1/6 (was VDDEH6). In a future revision of the device this may be changed to NC (no connect). Changes to calibration ball names on devices with 1 MB flash memory: • CAL_MDO0 changed to ALT_MDO0 • CAL_MDO1 changed to ALT_MDO1 • CAL_MDO2 changed to ALT_MDO2 • CAL_MDO3 changed to ALT_MDO3 • CAL_MSEO0 changed to ALT_MSEO0 • CAL_MSEO1 changed to ALT_MSEO1 • CAL_EVTI changed to ALT_EVTI • CAL_EVTO changed to ALT_EVTO • CAL_MCKO changed to ALT_MCKO Power/ground segment changes: • The following pins are on VDDE7 I/O segment only on the 208-ball BGA package: ALT_MDO[0:3], ALT_MSEO[0:1], ALT_EVTI, ALT_EVTO, ALT_MCKO. • Power segments VDDEH4, VDDEH4A and VDDEH4B have been removed. CLKOUT power segment is VDDE5 (was VDDE12) Thermal characteristics for 176-pin LQFP updated (all parameter values)

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Document Number: MPC5634M
Rev. 9
05/2012