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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z3
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5632mf2mlq60

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- Advanced error detection, and optional parity generation and detection
- Word length programmable as 8, 9, 12 or 13 bits
- Separately enabled transmitter and receiver
- LIN support
- DMA support
- Interrupt request support
- Programmable clock source: system clock or oscillator clock
- Support Microsecond Channel (Timed Serial Bus - TSB) upstream Version 1.0

- Two FlexCAN
  - One with 32 message buffers; the second with 64 message buffers
  - Full implementation of the CAN protocol specification, Version 2.0B
  - Based on and including all existing features of the Freescale TouCAN module
  - Programmable acceptance filters
  - Short latency time for high priority transmit messages
  - Arbitration scheme according to message ID or message buffer number
  - Listen only mode capabilities
  - Programmable clock source: system clock or oscillator clock
  - Message buffers may be configured as mailboxes or as FIFO
- Nexus port controller (NPC)
  - Per IEEE-ISTO 5001-2003
  - Real time development support for Power Architecture core and eTPU engine through Nexus class 2/1
  - Read and write access (Nexus class 3 feature that is supported on this device)
    - Run-time access of entire memory map
    - Calibration
  - Support for data value breakpoints / watchpoints
    - Run-time access of entire memory map
    - Calibration

      Table constants calibrated using MMU and internal and external RAM

      Scalar constants calibrated using cache line locking
  - Configured via the IEEE 1149.1 (JTAG) port
- IEEE 1149.1 JTAG controller (JTAGC)
  - IEEE 1149.1-2001 Test Access Port (TAP) interface
  - 5-bit instruction register that supports IEEE 1149.1-2001 defined instructions
  - 5-bit instruction register that supports additional public instructions
  - Three test data registers: a bypass register, a boundary scan register, and a device identification register
  - Censorship disable register. By writing the 64-bit serial boot password to this register, Censorship may be disabled until the next reset
  - TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- On-chip Voltage Regulator for single 5 V supply operation
  - On-chip regulator 5 V to 3.3 V for internal supplies
  - On-chip regulator controller 5 V to 1.2 V (with external bypass transistor) for core logic
- Low-power modes
  - SLOW Mode. Allows device to be run at very low speed (approximately 1 MHz), with modules (including the PLL) selectively disabled in software
  - STOP Mode. System clock stopped to all modules including the CPU. Wake-up timer used to restart the system clock after a predetermined time

Branch Address adder to minimize delays during change of flow operations. Sequential prefetching is performed to ensure a supply of instructions into the execution pipeline. Branch target prefetching is performed to accelerate taken branches. Prefetched instructions are placed into an instruction buffer capable of holding six instructions.

Branches can also be decoded at the instruction buffer and branch target addresses calculated prior to the branch reaching the instruction decode stage, allowing the branch target to be prefetched early. When a branch is detected at the instruction buffer, a prediction may be made on whether the branch is taken or not. If the branch is predicted to be taken, a target fetch is initiated and its target instructions are placed in the instruction buffer following the branch instruction. Many branches take zero cycle to execute by using branch folding. Branches are folded out from the instruction execution pipe whenever possible. These include unconditional branches and conditional branches with condition codes that can be resolved early.

Conditional branches which are not taken and not folded execute in a single clock. Branches with successful target prefetching which are not folded have an effective execution time of one clock. All other taken branches have an execution time of two clocks. Memory load and store operations are provided for byte, halfword, and word (32-bit) data with automatic zero or sign extension of byte and halfword load data as well as optional byte reversal of data. These instructions can be pipelined to allow effective single cycle throughput. Load and store multiple word instructions allow low overhead context save and restore operations. The load/store unit contains a dedicated effective address adder to allow effective address generation to be optimized. Also, a load-to-use dependency does not incur any pipeline bubbles for most cases.

The Condition Register unit supports the condition register (CR) and condition register operations defined by the Power Architecture. The condition register consists of eight 4-bit fields that reflect the results of certain operations, such as move, integer and floating-point compare, arithmetic, and logical instructions, and provide a mechanism for testing and branching. Vectored and autovectored interrupts are supported by the CPU. Vectored interrupt support is provided to allow multiple interrupt sources to have unique interrupt handlers invoked with no software overhead.

The hardware floating-point unit utilizes the IEEE-754 single-precision floating-point format and supports single-precision floating-point operations in a pipelined fashion. The general purpose register file is used for source and destination operands, thus there is a unified storage model for single-precision floating-point data types of 32 bits and the normal integer type. Single-cycle floating-point add, subtract, multiply, compare, and conversion operations are provided. Divide instructions are multi-cycle and are not pipelined.

The Signal Processing Extension (SPE) Auxiliary Processing Unit (APU) provides hardware SIMD operations and supports a full complement of dual integer arithmetic operation including Multiply Accumulate (MAC) and dual integer multiply (MUL) in a pipelined fashion. The general purpose register file is enhanced such that all 32 of the GPRs are extended to 64 bits wide and are used for source and destination operands, thus there is a unified storage model for 32×32 MAC operations which generate greater than 32-bit results.

The majority of both scalar and vector operations (including MAC and MUL) are executed in a single clock cycle. Both scalar and vector divides take multiple clocks. The SPE APU also provides extended load and store operations to support the transfer of data to and from the extended 64-bit GPRs. This SPE APU is fully binary compatible with e200z6 SPE APU used in MPC5554 and MPC5553.

The CPU includes support for Variable Length Encoding (VLE) instruction enhancements. This enables the classic Power Architecture instruction set to be represented by a modified instruction set made up from a mixture of 16- and 32-bit instructions. This results in a significantly smaller code size footprint without noticeably affecting performance. The Power Architecture instruction set and VLE instruction set are available concurrently. Regions of the memory map are designated as PPC or VLE using an additional configuration bit in each of Table Look-aside Buffers (TLB) entries in the MMU.

The CPU core is enhanced by the addition of two additional interrupt sources; Non-Maskable Interrupt and Critical Interrupt. These two sources are routed directly from package pins, via edge detection logic in the SIU to the CPU, bypassing completely the Interrupt Controller. Once the edge detection logic is programmed, it cannot be disabled, except by reset. The non-maskable Interrupt is, as the name suggests, completely un-maskable and when asserted will always result in the immediate execution of the respective interrupt service routine. The non-maskable interrupt is not guaranteed to be recoverable. The Critical Interrupt is very similar to the non-maskable interrupt, but it can be masked by other exceptional interrupts in the CPU and is guaranteed to be recoverable (code execution may be resumed from where it stopped).

The CPU core has an additional ‘Wait for Interrupt’ instruction that is used in conjunction with low power STOP mode. When Low Power Stop mode is selected, this instruction is executed to allow the system clock to be stopped. An external interrupt source or the system wake-up timer is used to restart the system clock and allow the CPU to service the interrupt.

2.2.2 Crossbar

The XBAR multi-port crossbar switch supports simultaneous connections between three master ports and four slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows three concurrent transactions to occur from the master ports to any slave port; but each master must access a different slave. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters are treated with equal priority and are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access. The crossbar provides the following features:

- 3 master ports:
  - e200z335 core complex Instruction port
  - e200z335 core complex Load/Store port
  - eDMA
- 4 slave ports
  - FLASH
  - calibration bus
  - SRAM
  - Peripheral bridge A/B (eTPU2, eMIOS, SIU, DSPI, eSCI, FlexCAN, eQADC, BAM, decimation filter, PIT, STM and SWT)
- 32-bit internal address, 64-bit internal data paths

2.2.3 eDMA

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 32 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size. The eDMA module provides the following features:

- All data movement via dual-address transfers: read from source, write to destination
- Programmable source and destination addresses, transfer size, plus support for enhanced addressing modes
- Transfer control descriptor organized to support two-deep, nested transfer operations
- An inner data transfer loop defined by a “minor” byte transfer count
- An outer data transfer loop defined by a “major” iteration count
- Channel activation via one of three methods:
  - Explicit software initiation
  - Initiation via a channel-to-channel linking mechanism for continuous transfers
  - Peripheral-paced hardware requests (one per channel)
- Support for fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests
- 1 interrupt per channel, optionally asserted at completion of major iteration count
- Error termination interrupts are optionally enabled
- Support for scatter/gather DMA processing

- Each of the three modes may be run with a crystal oscillator or an external clock reference
- Programmable frequency modulation
  - Modulation enabled/disabled through software
  - Triangle wave modulation up to 100 kHz modulation frequency
  - Programmable modulation depth (0% to 2% modulation depth)
  - Programmable modulation frequency dependent on reference frequency
- Lock detect circuitry reports when the PLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Clock Quality Module
  - detects the quality of the crystal clock and cause interrupt request or system reset if error is detected
  - detects the quality of the PLL output clock. If an error is detected, causes a system reset or switches the system clock to the crystal clock and causes an interrupt request
- Programmable interrupt request or system reset on loss of lock

2.2.6 Calibration EBI

The Calibration EBI controls data transfer across the crossbar switch to/from memories or peripherals attached to the VertiCal connector in the calibration address space. The Calibration EBI is only available in the VertiCal Calibration System. The Calibration EBI includes a memory controller that generates interface signals to support a variety of external memories. The Calibration EBI memory controller supports legacy flash, SRAM, and asynchronous memories. In addition, the calibration EBI supports up to three regions via chip selects (two chip selects are multiplexed with two address bits), along with programmed region-specific attributes. The calibration EBI supports the following features:

- 22-bit address bus (two most significant signals multiplexed with two chip selects)
- 16-bit data bus
- Multiplexed mode with addresses and data signals present on the data lines

NOTE

The calibration EBI must be configured in multiplexed mode when the extended Nexus trace is used on the VertiCal Calibration System. This is because Nexus signals and address lines of the calibration bus share the same balls in the calibration package.

- Memory controller with support for various memory types:
  - Asynchronous/legacy flash and SRAM
  - Most standard memories used with the MPC5xx or MPC55xx family
- Bus monitor
  - User selectable
  - Programmable timeout period (with 8 external bus clock resolution)
- Configurable wait states (via chip selects)
- 3 chip-select (Cal_$\overline{CS}$[0], Cal_$\overline{CS}$[2:3]) signals (Multiplexed with 2 most significant address signals)
- 2 write/byte enable (WE[0:1]/BE[0:1]) signals
- Configurable bus speed modes
  - system frequency
  - 1/2 of system frequency
  - 1/4 of system frequency
- Optional automatic CLKOUT gating to save power and reduce EMI
- Compatible with MPC5xx external bus (with some limitations)
- Selectable drive strengths; 10 pF, 20 pF, 30 pF, 50 pF

standard. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE 1149.1-2001 standard and supports the following features:

- IEEE 1149.1-2001 Test Access Port (TAP) interface 4 pins (TDI, TMS, TCK, and TDO)
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD, HIGHZ, CLAMP
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC
  - ACCESS_AUX_TAP_ONCE
  - ACCESS_AUX_TAP_eTPU
  - ACCESS_CENSOR
- 3 test data registers to support JTAG Boundary Scan mode
  - Bypass register
  - Boundary scan register
  - Device identification register
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- Censorship Inhibit Register
  - 64-bit Censorship password register
  - If the external tool writes a 64-bit password that matches the Serial Boot password stored in the internal flash shadow row, Censorship is disabled until the next system reset.

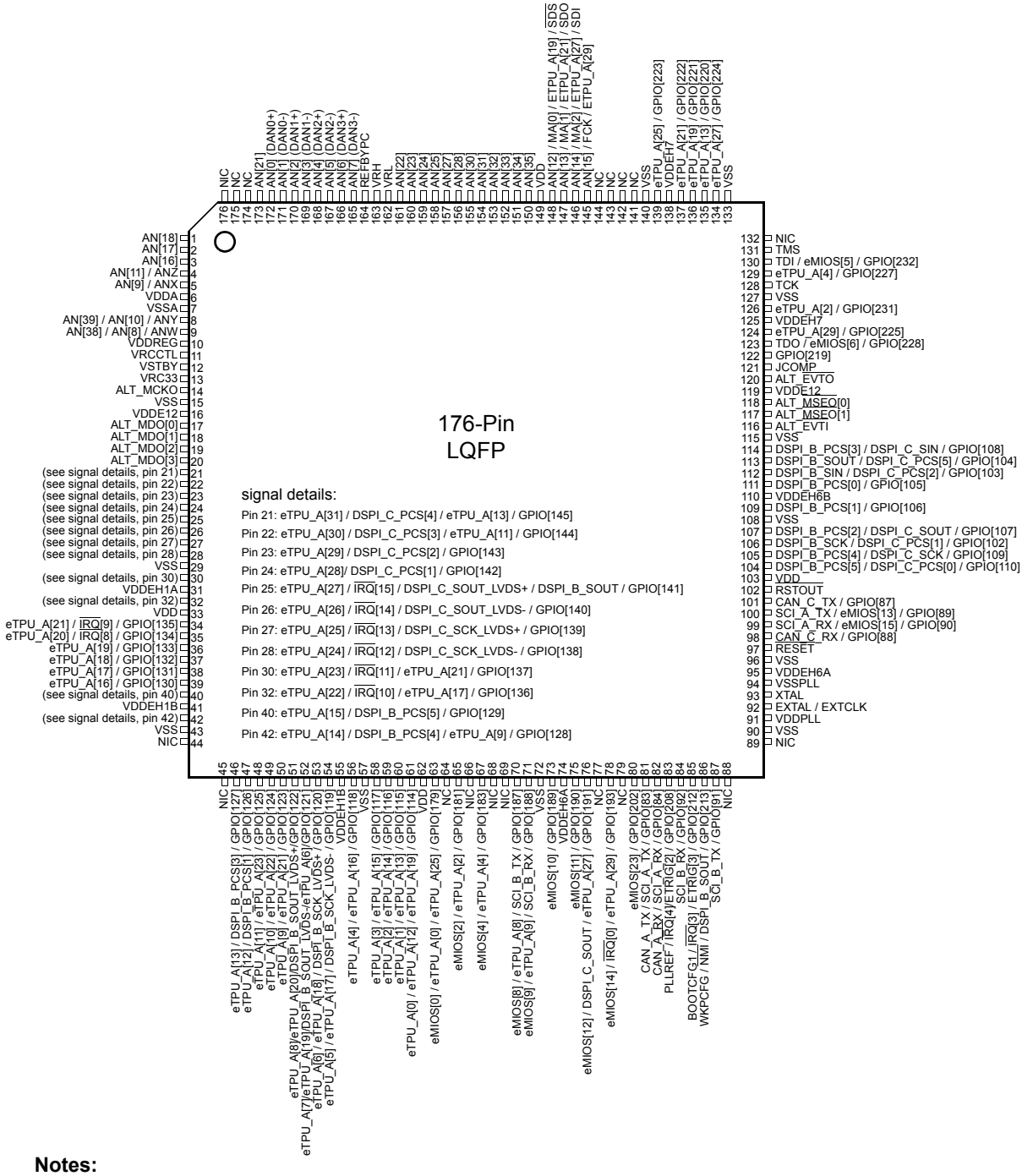
2.3 MPC5634M series architecture

2.3.1 Block diagram

Figure 1 shows a top-level block diagram of the MPC5634M series.

3.3 176 LQFP pinout (MPC5633M)

Figure 4 shows the pinout for the 176-pin LQFP for the MPC5633M (1024 KB flash memory).



Notes:

1. Pins marked “NIC” have no internal connection.
2. Pins marked “NC” are not functional pins but may be connected to internal circuitry. Connections to external circuits or other pins on this device can result in unpredictable system behavior or damage.

Figure 4. 176-pin LQFP pinout (MPC5633M; top view)

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPBGA
CAL_ADDR[16][21] ALT_MDO[0][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	MDO / ALT_ADDR[12] / Low		—	17	A14
CAL_ADDR[17][21] ALT_MDO[1][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	ALT_MDO / CAL_ADDR[12] / Low		—	18	B14
CAL_ADDR[18][21] ALT_MDO[2][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	ALT_MDO / CAL_ADDR[12] / Low		—	19	A13
CAL_ADDR[19][21] ALT_MDO[3][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	ALT_MDO / CAL_ADDR[12] / Low		—	20	B13
CAL_ADDR[20:27] ALT_MDO[4:11]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] Fast	O / Low	ALT_MDO / CAL_ADDR[16] / Low		—	—	—
CAL_ADDR[28][21] ALT_$\overline{\text{MSEO}}$[0][12]	Calibration Address Bus Nexus Msg Start/End Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[17]	ALT_$\overline{\text{MSEO}}$[16] / CAL_ADDR[17]/ Low		—	118	C15
CAL_ADDR[29][21] ALT_$\overline{\text{MSEO}}$[1][12]	Calibration Address Bus Nexus Msg Start/End Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[17]	ALT_$\overline{\text{MSEO}}$[16] / CAL_ADDR[17]/ Low		—	117	E16
CAL_ADDR[30][21] ALT_$\overline{\text{EVTI}}$[12]	Calibration Address Bus Nexus Event In	PCR[345]	—	O I	VDDE12[13] VDDE7[14] Fast	—[18]	ALT_$\overline{\text{EVTI}}$ / CAL_ADDR[19]		—	116	E15
ALT_$\overline{\text{EVTO}}$	Nexus Event Out	PCR[344]	—	O	VDDE12[13] VDDE7[14] Fast	O / Low	ALT_$\overline{\text{EVTO}}$ / High		—	120	D15
ALT_MCKO	Nexus Msg Clock Out	PCR[344]	—	O	VDDE12[13] VDDE7[14] Fast	O / Low	ALT_MCKO / Enabled		—	14	F15
NEXUSCFG[11]	Nexus/Calibration bus selector	—	—	I	VDDE12 Fast	I / Down	NEXUSCFG / Down		—	—	—
CAL_$\overline{\text{CS}}$[0][11]	Calibration Chip Selects	PCR[336]	—	O	VDDE12 Fast	O / High	CAL_$\overline{\text{CS}}$ / High		—	—	—
CAL_$\overline{\text{CS}}$[2][11] CAL_ADDR[10]	Calibration Chip Selects Calibration Address Bus	PCR[338]	11 10	O O	VDDE12 Fast	O / High	CAL_$\overline{\text{CS}}$ / High		—	—	—

[9] The GPIO functions on GPIO[206] and GPIO[207] can be selected as trigger functions in the SIU for the ADC by making the proper selections in the SIU_ETISR and SIU_ISEL3 registers in the SIU.

[10] Some signals in this section are available only on calibration package.

[11] These pins are only available in the 496 CSP/MAPBGA calibration/development package.

[12] On the calibration package, the Nexus function on this pin is enabled when the NEXUSCFG pin is high and Nexus is configured to full port mode. On the 176-pin and 208-pin packages, the Nexus function on this pin is enabled permanently. Do not connect the Nexus MDO or MSEO pins directly to a power supply or ground.

[13] In the calibration package, the I/O segment containing this pin is called VDDE12.

[14] 208-ball BGA package only

[15] When configured as Nexus (208-pin package or calibration package with NEXUSCFG=1), and JCOMP is asserted during reset, MDO[0] is driven high until the crystal oscillator becomes stable, at which time it is then negated.

[16] The function of this pin is Nexus when NEXUSCFG is high.

[17] High when the pin is configured to Nexus, low otherwise.

[18] O/Low for the calibration with NEXUSCFG=0; I/Up otherwise.

[19] ALT_ADDR/Low for the calibration package with NEXUSCFG=0; $\overline{\text{EVTI}}$/Up otherwise.

[20] In 176-pin and 208-pin packages, the Nexus function is disabled and the pin/ball has the secondary function

[21] This signal is not available in the 176-pin and 208-pin packages.

[22] The primary function is not selected via the PA field when the pin is a Nexus signal. Instead, it is activated by the Nexus controller.

[23] TDI and TDO are required for JTAG operation.

[24] The primary function is not selected via the PA field when the pin is a JTAG signal. Instead, it is activated by the JTAG controller.

[25] The function and state of the CAN_A and eSCI_A pins after execution of the BAM program is determined by the BOOTCFG1 pin.

[26] Connect an external 10K pull-up resistor to the SCI_A_RX pin to ensure that the pin is driven high during CAN serial boot.

[27] For pins AN[0:7], during and just after POR negates, internal pull resistors can be enabled, resulting in as much as 4 mA of current draw. The pull resistors are disabled when the system clock propagates through the device.

[28] ETPUA[24:29] are input and output. The input muxing is controlled by SIU_ISEL8 register.

[29] eTPU_A[25] is an output only function.

[30] Only the output channels of eTPU[8:9] are connected to pins.

[31] The function after reset of the XTAL pin is determined by the value of the signal on the PLLCFG[1] pin. When bypass mode is chosen XTAL has no function and should be grounded.

[32] The function after reset of the EXTAL_EXTCLK pin is determined by the value of the signal on the PLLCFG[1] pin. If the EXTCLK function is chosen, the valid operating voltage for the pin is 1.62 V to 3.6 V. If the EXTAL function is chosen, the valid operating voltage is 3.3 V.

[33] VSSPLL and VSSREG are connected to the same pin.

[34] This pin is shared by two pads: VDDA_AN, using pad_vdde_hv, and VDDA_DIG, using pad_vdde_int_hv.

[35] This pin is shared by two pads: VSSA_AN, using pad_vsse_hv, and VSSA_DIG, using pad_vsse_int_hv.

[36] VDDEH1A, VDDEH1B, and VDDEH1AB are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[37] LVDS pins will not work at 3.3 V.

[38] The VDDEH6 segment may be powered from 3.0 V to 5.0 V for mux address or SSI functions, but must meet the VDDA specifications of 4.5 V to 5.25 V for analog input function.

[39] VDDEH6A and VDDEH6B are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[40] If using JTAG or Nexus, the I/O segment that contains the JTAG and Nexus pins must be powered by a 5 V supply. The 3.3 V Nexus/JTAG signals are derived from the 5 volt power supply.

[41] In the calibration package this signal is named VDDE12.

Table 3. Pad types

Pad Type	Name	Supply Voltage
Slow	pad_ssr_hv	3.0 V – 5.25 V
Medium	pad_msr_hv	3.0 V – 5.25 V
Fast	pad_fc	3.0 V – 3.6 V
MultiV	pad_multv_hv	3.0 V – 5.25 V (high swing mode) 4.5 V – 5.25 V (low swing mode)
Analog	pad_ae_hv	0.0 – 5.25 V
LVDS	pad_lo_lv	—

Table 7. Absolute maximum ratings[1] (continued)

Symbol		Parameter	Conditions	Value		Unit
				min	max	
V_{DDA}	SR	Analog supply voltage[4]	Reference to V_{SSA}	– 0.3	5.5	V
V_{DDE}	SR	I/O supply voltage[6]		– 0.3	3.6	V
V_{DDEH}	SR	I/O supply voltage[4]		– 0.3	5.5	V
V_{IN}	SR	DC input voltage[7]	V_{DDEH} powered I/O pads	–1.0[8]	V_{DDEH} + 0.3 V[9]	V
			V_{DDE} powered I/O pads	–1.0[10]	V_{DDE} + 0.3 V[10]	
			V_{DDA} powered I/O pads	–1.0	V_{DDA} + 0.3 V	
V_{DDREG}	SR	Voltage regulator supply voltage[6]		– 0.3	5.5	V
V_{RH}	SR	Analog reference high voltage	Reference to VRL	– 0.3	5.5	V
$V_{SS} – V_{SSA}$	SR	V_{SS} differential voltage		– 0.1	0.1	V
$V_{RH} – V_{RL}$	SR	V_{REF} differential voltage[6]		– 0.3	5.5	V
$V_{RL} – V_{SSA}$	SR	VRL to V_{SSA} differential voltage		– 0.3	0.3	V
$V_{SSPLL} – V_{SS}$	SR	V_{SSPLL} to V_{SS} differential voltage		– 0.1	0.1	V
I_{MAXD}	SR	Maximum DC digital input current[11]	Per pin, applies to all digital pins	– 3	3	mA
I_{MAXA}	SR	Maximum DC analog input current[12]	Per pin, applies to all analog pins	—	5	mA
T_J	SR	Maximum operating temperature range[13] – die junction temperature		– 40.0	150.0	°C
T_{STG}	SR	Storage temperature range		– 55.0	150.0	°C
T_{SDR}	SR	Maximum solder temperature[14]		—	260.0	°C
MSL	SR	Moisture sensitivity level[15]		—	3	—

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Allowed 2 V for 10 hours cumulative time, remaining time at 1.2 V +10%.

3 The V_{FLASH} supply is connected to V_{DDEH1}.

4 Allowed 6.8 V for 10 hours cumulative time, remaining time at 5 V +10%.

5 The pin named as V_{RC33} is internally connected to the pads V_{FLASH} and V_{RC33} in the 144 LQFP package. These limits apply when the internal regulator is disabled and V_{RC33} power is supplied externally.

6 All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}, or V_{DDEH}.

7 AC signal overshoot and undershoot of up to 2.0 V of the input voltages is permitted for an accumulative duration of 60 hours over the complete lifetime of the device (injection current not limited for this duration).

4.6 Power Management Control (PMC) and Power On Reset (POR) electrical specifications

Table 13. PMC Operating conditions and external regulators supply voltage

ID	Name		C	Parameter	Min	Typ	Max	Unit
1	Jtemp	SR	—	Junction temperature	–40	27	150	°C
2	Vddreg	SR	—	PMC 5 V supply voltage VDDREG	4.75[1]	5	5.25	V
3	Vdd	SR	—	Core supply voltage 1.2 V VDD when external regulator is used without disabling the internal regulator (PMC unit turned on, LVI monitor active)[2]	1.26[3]	1.3	1.32	V
3a	—	SR	—	Core supply voltage 1.2 V VDD when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	1.14	1.2	1.32	V
4	Ivdd	SR	—	Voltage regulator core supply maximum DC output current[4]	400	—	—	mA
5	Vdd33	SR	—	Regulated 3.3 V supply voltage when external regulator is used without disabling the internal regulator (PMC unit turned-on, internal 3.3V regulator enabled, LVI monitor active)[5]	3.3	3.45	3.6	V
5a	—	SR	—	Regulated 3.3 V supply voltage when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	3	3.3	3.6	V
6	—	SR	—	Voltage regulator 3.3 V supply maximum required DC output current	80	—	—	mA

1 During start up operation the minimum required voltage to come out of reset state is 4.6 V.

2 An internal regulator controller can be used to regulate core supply.

3 The minimum supply required for the part to exit reset and enter in normal run mode is 1.28 V.

4 The onchip regulator can support a minimum of 400 ma although the worst case core current is 180 ma.

5 An internal regulator can be used to regulate 3.3 V supply.

Table 14. PMC electrical characteristics

ID	Name		C	Parameter	Min	Typ	Max	Unit	Notes
1	Vbg	CC	C	Nominal bandgap voltage reference	—	1.219	—	V	
1a	—	CC	P	Untrimmed bandgap reference voltage	Vbg–7%	Vbg	Vbg+6%	V	
1b	—	CC	P	Trimmed bandgap reference voltage (5 V, 27 °C)[1]	Vbg–10mV	Vbg	Vbg+10mV	V	
1c	—	CC	C	Bandgap reference temperature variation	—	100	—	ppm /°C	

Table 14. PMC electrical characteristics (continued)

ID	Name		C	Parameter	Min	Typ	Max	Unit	Notes
5b	—	CC	P	Nominal 3.3 V supply internal regulator DC output voltage variation after power-on reset	Vdd33 – 7.5%	Vdd33	Vdd33 + 7%	V	With internal load up to Idd3p3
5c	—	CC	D	Voltage regulator 3.3 V output impedance at maximum DC load	—	—	2	Ω	
5d	Idd3p3	CC	P	Voltage regulator 3.3 V maximum DC output current	80	—	—	mA	
5e	Vdd33 ILim[6]	CC	C	Voltage regulator 3.3 V DC current limit	—	130	—	mA	
6	Lvi3p3	CC	C	Nominal LVI for rising 3.3 V supply[5]	—	3.090	—	V	The Lvi3p3 specs are also valid for the Vddeh LVI
6a	—	CC	C	Variation of LVI for rising 3.3 V supply at power-on reset[5]	Lvi3p3–6%	Lvi3p3	Lvi3p3+6%	V	See note [7]
6b	—	CC	C	Variation of LVI for rising 3.3 V supply after power-on reset[5]	Lvi3p3–3%	Lvi3p3	Lvi3p3+3%	V	See note 7
6c	—	CC	C	Trimming step LVI 3.3 V[5]	—	20	—	mV	
6d	Lvi3p3_h	CC	C	LVI 3.3 V hysteresis[5]	—	60	—	mV	
7	Por3.3V_r	CC	C	Nominal POR for rising 3.3 V supply	—	2.07	—	V	The 3.3V POR specs are also valid for the Vddeh POR
7a	—	CC	C	Variation of POR for rising 3.3 V supply	Por3.3V_r–35%	Por3.3V_r	Por3.3V_r+35%	V	
7b	Por3.3V_f	CC	C	Nominal POR for falling 3.3 V supply	—	1.95	—	V	
7c	—	CC	C	Variation of POR for falling 3.3 V supply	Por3.3V_f–35%	Por3.3V_f	Por3.3V_f+35%	V	
8	Lvi5p0	CC	C	Nominal LVI for rising 5 V VDDREG supply[5]	—	4.290	—	V	
8a	—	CC	C	Variation of LVI for rising 5 V VDDREG supply at power-on reset[5]	Lvi5p0–6%	Lvi5p0	Lvi5p0+6%	V	
8b	—	CC	C	Variation of LVI for rising 5 V VDDREG supply power-on reset[5]	Lvi5p0–3%	Lvi5p0	Lvi5p0+3%	V	
8c	—	CC	C	Trimming step LVI 5 V[5]	—	20	—	mV	

4.6.1 Regulator example

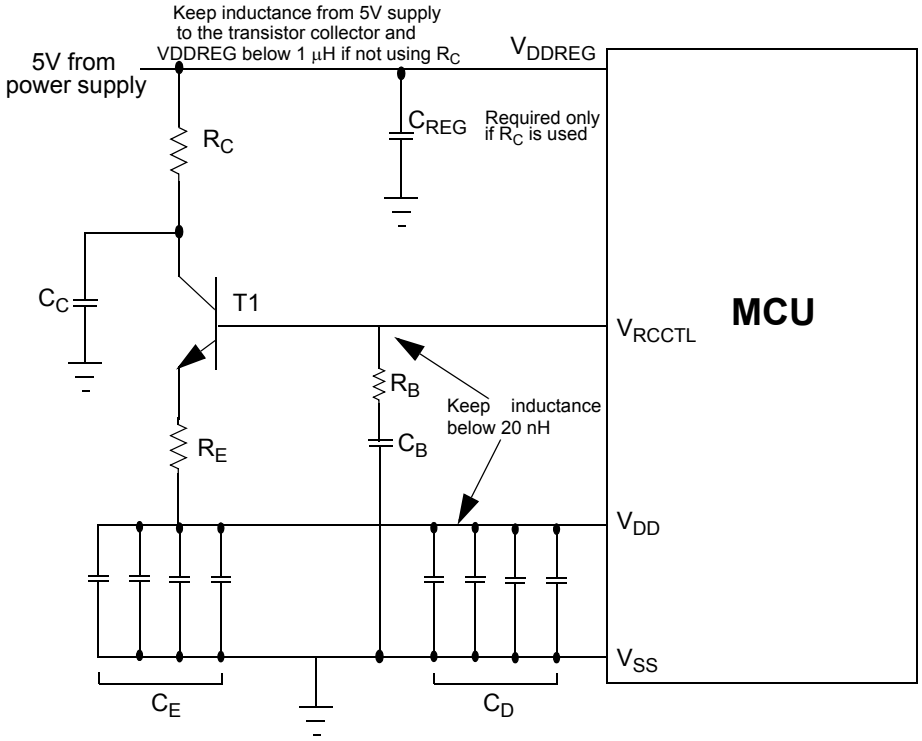


Figure 7. Core voltage regulator controller external components preferred configuration

There are three options for the bypassing and compensation networks for the 1.2V regulator controller. The component values in the following table are the same for all PMC network requirements.

Table 15. Required external PMC component values

Component	Symbol	Minimum	Typical	Maximum	Units	Comment
Pass Transistor	T1					NJD2873 or BCP68
VDDREG capacitor	C_{REG}		10		µF	X7R, -50%/+35%
Pass transistor Collector bypass capacitor	C_C			13.3	µF	X7R, -50%/+35%
Collector resistor[1]	R_C	1.1	—	5.6	Ω	

[1] The collector resistor may not be required. It depends on the allowable power dissipation of the pass transistor (T1).

Table 16, Table 17 and Table 18 show the required component values for the three different options.

Table 16. Network 1 component values

Component	Symbol	Minimum	Typical	Maximum	Units	Comment
Transistor emitter bypass capacitance	C_E	4 x 2.35	4 x 4.7	4 x 6.35	µF	X7R, -50%/+35%
		1 x 5	1 x 10	1 x 13.5	µF	X7R, -50%/+35%
	R_{ESR}	5		50	mΩ	Equivalent ESR of C_E capacitors
MCU decoupling capacitor	C_D	4 x 50	4 x 100	4 x 135	nF	X7R, -50%/+35%
Base "snubber" capacitor	C_B	1.1	2.2	2.97	µF	X7R, -50%/+35%
Base "snubber" resistor	R_B	6.12	6.8	7.48	Ω	±10%
Emitter resistor	R_E	0	0	0	Ω	Not required (short)

Table 17. Network 2 component values

Component	Symbol	Minimum	Typical	Maximum	Units	Comment
Transistor emitter bypass capacitance	C_E	3 x 2.35	3 x 4.7	3 x 6.35	µF	X7R, -50%/+35%
		1 x 5	1 x 10	1 x 13.5	µF	X7R, -50%/+35%
	R_{ESR}	5		50	mΩ	Equivalent ESR of C_E capacitors
MCU decoupling capacitor	C_D	4 x 50	4 x 100	4 x 135	nF	X7R, -50%/+35%
Base "snubber" capacitor	C_B	1.1	2.2	2.97	µF	X7R, -50%/+35%
Base "snubber" resistor	R_B	9	10	11	Ω	±10%
Emitter resistor	R_E	0.252	0.280	0.308	Ω	Not required (short)

The following component configuration is acceptable when using the BCP68 transistor, however, is not recommended for new designs. Either option 1 or option 2 should be used for new designs. This option should not be used with the NJD2873 transistor.

Table 18. Network 3 component values

Component	Symbol	Minimum	Typical	Maximum	Units	Comment
Transistor emitter bypass capacitance	C_E	4 x 3.4	4 x 6.8	4 x 9.18	µF	X7R, -50%/+35%
	R_{ESR}	5		50	mΩ	Equivalent ESR of C_E capacitors
MCU decoupling capacitor	C_D	4 x 110	4 x 220	4 x 297	nF	X7R, -50%/+35%
Base "snubber" capacitor	C_B	1.1	2.2	2.97	µF	X7R, -50%/+35%
Base "snubber" resistor	R_B	13.5	15	16.5	Ω	±10%
Emitter resistor	R_E	0	0	0	Ω	Not required (short)

4.9 I/O Pad current specifications

NOTE

MPC5634M devices use two sets of I/O pads (5 V and 3.3 V). See Table 2 and Table 3 in Section 3.6, "Signal summary, for the pad type associated with each signal.

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 23 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 23.

Table 23. I/O pad average I_{DDE} specifications[1]

Pad Type	Symbol		C	Period (ns)	Load[2] (pF)	V_{DDE} (V)	Drive/Slew Rate Select	I_{DDE} Avg (mA)[3]	I_{DDE} RMS (mA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	37	50	5.25	11	9	—
		CC	D	130	50	5.25	01	2.5	—
		CC	D	650	50	5.25	00	0.5	—
		CC	D	840	200	5.25	00	1.5	—
Medium	$I_{DRV\_MSR\_HV}$	CC	D	24	50	5.25	11	14	—
		CC	D	62	50	5.25	01	5.3	—
		CC	D	317	50	5.25	00	1.1	—
		CC	D	425	200	5.25	00	3	—
Fast	I_{DRV_FC}	CC	D	10	50	3.6	11	22.7	68.3
		CC	D	10	30	3.6	10	12.1	41.1
		CC	D	10	20	3.6	01	8.3	27.7
		CC	D	10	10	3.6	00	4.44	14.3
		CC	D	10	50	1.98	11	12.5	31
		CC	D	10	30	1.98	10	7.3	18.6
		CC	D	10	20	1.98	01	5.42	12.6
		CC	D	10	10	1.98	00	2.84	6.4
MultiV (High Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	15	50	5.25	11	21.2[4]	—
		CC	D	30	50	5.25	10	—[5]	—
		CC	D	50	50	5.25	01	6.2[4]	—
		CC	D	300	50	5.25	00	1.1[4]	—
		CC	D	300	200	5.25	00	4.0[4]	—
MultiV (Low Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	15	30	5.25	11	20.2[6]	—
		CC	D	30	30	5.25	11	NA	—

1 Numbers from simulations at best case process, 150 °C.

2 All loads are lumped.

3 Average current is for pad configured as output only.

[4] Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

[5] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA} + 0.5$ V and $V_{NEGCLAMP} = – 0.3$ V, then use the larger of the calculated values.

[6] Condition applies to two adjacent pins at injection limits.

[7] Performance expected with production silicon.

[8] All channels have same 10 kΩ < Rs < 100 kΩ; Channel under test has Rs=10 kΩ; I_{INJ}=I_{INJMAX},I_{INJMIN}.

[9] TUE is tested by averaging 10 samples.

[10] TUE is tested by averaging three samples.

[11] These values can be significantly improved by using three samples of averaging. Input frequency of 1 kHz was used as the reference for the Signal to Noise Ratio.

[12] Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed by as indicated.

[13] At $V_{RH} – V_{RL} = 5.12$ V, one LSB = 1.25 mV.

[14] Guaranteed 10-bit monotonicity.

[15] Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

Table 32. Flash module life

Symbol		Parameter	Conditions	Value		Unit
				Min	Typ	
P/E	C	Number of program/erase cycles per block for 16 Kbyte blocks over the operating temperature range (T_J)	—	100,000	—	cycles
P/E	C	Number of program/erase cycles per block for 32 and 64 Kbyte blocks over operating temperature range (T_J)	—	10,000	100,000	cycles
P/E	C	Number of program/erase cycles per block for 128 Kbyte blocks over the operating temperature range (T_J)	—	1,000	100,000	cycles
Retention	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0 – 1,000 P/E cycles	20	—	years
			Blocks with 10,000 P/E cycles	10	—	years
			Blocks with 100,000 P/E cycles	5	—	years

[1] Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

Table 37. Nexus debug port timing[1] (continued)

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
9	t_{TCYC}	CC	D	TCK Cycle Time	4[6,7]	—	t_{CYC}
9a	t_{TCYC}	CC	D	Absolute Minimum TCK Cycle Time	100[8]	—	ns
10	t_{TDC}	CC	D	TCK Duty Cycle	40	60	%
11	t_{NTDIS}	CC	D	TDI Data Setup Time	5	—	ns
12	t_{NTDIH}	CC	D	TDI Data Hold Time	25	—	ns
13	t_{NTMSS}	CC	D	TMS Data Setup Time	5	—	ns
14	t_{NTMSH}	CC	D	TMS Data Hold Time	25	—	ns
15	t_{JOV}	CC	D	TCK Low to TDO Data Valid	10	20	ns

1 All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.25 V with multi-voltage pads programmed to Low-Swing mode, T_A = TL to TH, and CL = 30 pF with DSC = 0b10.

2 Achieving the absolute minimum MCKO cycle time may require setting the MCKO divider to more than its minimum setting (NPC_PCR[MCKO_DIV] depending on the actual system frequency being used.

3 This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum MCKO period specification.

4 This may require setting the MCKO divider to more than its minimum setting (NPC_PCR[MCKO_DIV]) depending on the actual system frequency being used.

5 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

6 Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

7 This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.

8 This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

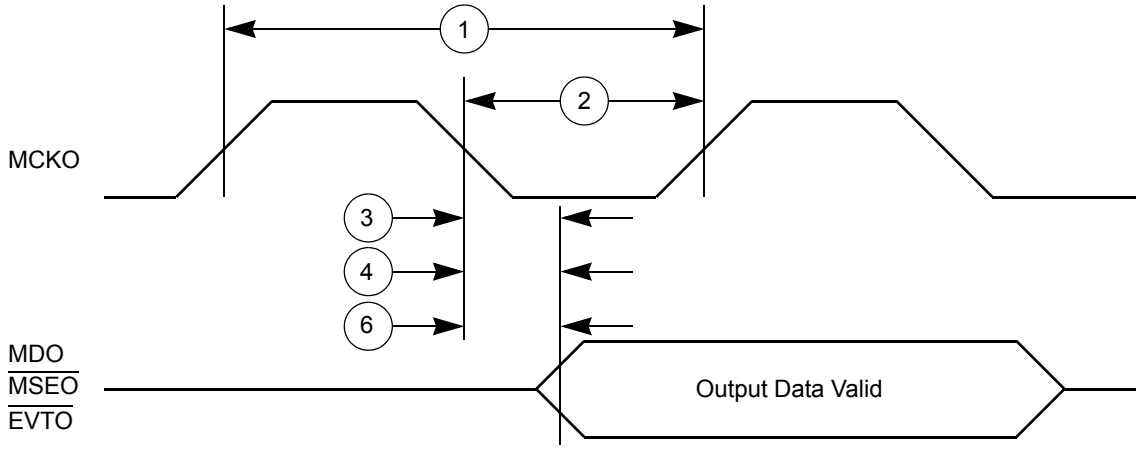


Figure 13. Nexus output timing

4.16.6 eQADC SSI timing

Table 41. eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V)[1]

CLOAD = 25pF on all outputs. Pad drive strength set to maximum.								
#	Symbol		C	Rating	Min	Typ	Max	Unit
1	f_{FCK}	CC	D	FCK Frequency [2, 3]	1/17 f_{SYS_CLK}		1/2 f_{SYS_CLK}	Hertz
1	t_{FCK}	CC	D	FCK Period (t_{FCK} = 1/ f_{FCK})	2 t_{SYS_CLK}		17t_{SYS_CLK}	seconds
2	t_{FCKHT}	CC	D	Clock (FCK) High Time	t_{SYS_CLK} − 6.5		$_{9*}$ t_{SYS_CLK} + 6.5	ns
3	t_{FCKLT}	CC	D	Clock (FCK) Low Time	t_{SYS_CLK} − 6.5		$_{8*}$ t_{SYS_CLK} + 6.5	ns
4	t_{SDS_LL}	CC	D	SDS Lead/Lag Time	–7.5		+7.5	ns
5	t_{SDO_LL}	CC	D	SDO Lead/Lag Time	–7.5		+7.5	ns
6	t_{DVFE}	CC	D	Data Valid from FCK Falling Edge (t_{FCKLT}+t_{SDO_LL})	1			ns
7	t_{EQ_SU}	CC	D	eQADC Data Setup Time (Inputs)	22			ns
8	t_{EQ_HO}	CC	D	eQADC Data Hold Time (Inputs)	1			ns

1 SS timing specified at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.25 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b00.

2 Maximum operating frequency is highly dependent on track delays, master pad delays, and slave pad delays.

3 FCK duty is not 50% when it is generated through the division of the system clock by an odd number.

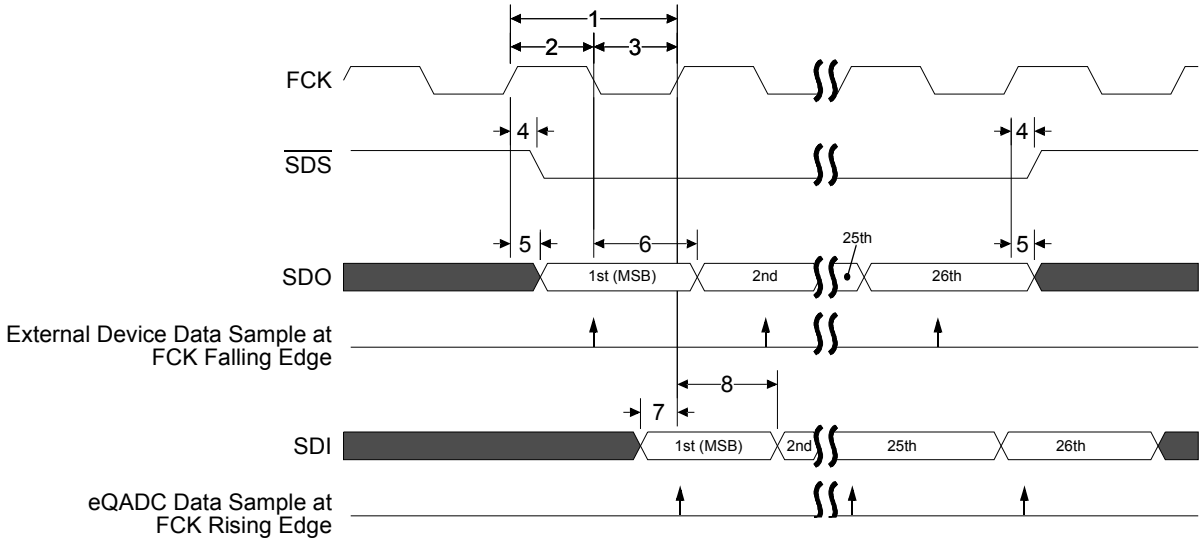


Figure 29. eQADC SSI timing