Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5633mf1mlq40

The CPU core has an additional ‘Wait for Interrupt’ instruction that is used in conjunction with low power STOP mode. When Low Power Stop mode is selected, this instruction is executed to allow the system clock to be stopped. An external interrupt source or the system wake-up timer is used to restart the system clock and allow the CPU to service the interrupt.

2.2.2 Crossbar

The XBAR multi-port crossbar switch supports simultaneous connections between three master ports and four slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows three concurrent transactions to occur from the master ports to any slave port; but each master must access a different slave. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters are treated with equal priority and are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access. The crossbar provides the following features:

- 3 master ports:
  - e200z335 core complex Instruction port
  - e200z335 core complex Load/Store port
  - eDMA
- 4 slave ports
  - FLASH
  - calibration bus
  - SRAM
  - Peripheral bridge A/B (eTPU2, eMIOS, SIU, DSPI, eSCI, FlexCAN, eQADC, BAM, decimation filter, PIT, STM and SWT)
- 32-bit internal address, 64-bit internal data paths

2.2.3 eDMA

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 32 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size. The eDMA module provides the following features:

- All data movement via dual-address transfers: read from source, write to destination
- Programmable source and destination addresses, transfer size, plus support for enhanced addressing modes
- Transfer control descriptor organized to support two-deep, nested transfer operations
- An inner data transfer loop defined by a “minor” byte transfer count
- An outer data transfer loop defined by a “major” iteration count
- Channel activation via one of three methods:
  - Explicit software initiation
  - Initiation via a channel-to-channel linking mechanism for continuous transfers
  - Peripheral-paced hardware requests (one per channel)
- Support for fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests
- 1 interrupt per channel, optionally asserted at completion of major iteration count
- Error termination interrupts are optionally enabled
- Support for scatter/gather DMA processing

intervention. Consequently, for each timer event, the host CPU setup and service times are minimized or eliminated. A powerful timer subsystem is formed by combining the eTPU2 with its own instruction and data RAM. High-level assembler/compiler and documentation allows customers to develop their own functions on the eTPU2.

The eTPU2 includes these distinctive features:

- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.
- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.
- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.
- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.
- 32 channels, each channel is associated with one input and one output signal
  - Enhanced input digital filters on the input pins for improved noise immunity.
  - Identical, orthogonal channels: each channel can perform any time function. Each time function can be assigned to more than one channel at a given time, so each signal can have any functionality.
  - Each channel has an event mechanism which supports single and double action functionality in various combinations. It includes two 24-bit capture registers, two 24-bit match registers, 24-bit greater-equal and equal-only comparators
  - Input and output signal states visible from the host
- 2 independent 24-bit time bases for channel synchronization:
  - First time base clocked by system clock with programmable prescale division from 2 to 512 (in steps of 2), or by output of second time base prescaler
  - Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
  - Both time bases can be exported to the eMIOS timer module
  - Both time bases visible from the host
- Event-triggered microengine:
  - Fixed-length instruction execution in two-system-clock microcycle
  - 14 KB of code memory (SCM)
  - 3 KB of parameter (data) RAM (SPRAM)
  - Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations

  - Queue_0 can bypass all prioritization, buffering and abort current conversions to start a Queue_0 conversion a deterministic time after the queue trigger
  - Streaming mode operation of Queue_0 to execute some commands several times
  - Supports software and hardware trigger modes to arm a particular Queue
  - Generates interrupt when command coherency is not achieved
- External hardware triggers
  - Supports rising edge, falling edge, high level and low level triggers
  - Supports configurable digital filter
- Supports four external 8-to-1 muxes which can expand the input channels to 56 channels total

2.2.15 DSPI

The deserial serial peripheral interface (DSPI) block provides a synchronous serial interface for communication between the MPC5634M MCU and external devices. The DSPI supports pin count reduction through serialization and deserialization of eTPU and eMIOS channels and memory-mapped registers. The channels and register content are transmitted using a SPI-like protocol. This SPI-like protocol is completely configurable for baud rate, polarity and phase, frame length, chip select assertion, etc. Each bit in the frame may be configured to serialize either eTPU channels, eMIOS channels or GPIO signals. The DSPI can be configured to serialize data to an external device that supports the Microsecond Channel protocol. There are two identical DSPI blocks on the MPC5634M MCU. The DSPI output pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) according to the Microsecond Channel specification.

The DSPIs have three configurations:

- Serial peripheral interface (SPI) configuration where the DSPI operates as an up to 16-bit SPI with support for queues
- Enhanced deserial serial interface (DSI) configuration where DSPI serializes up to 32 bits with three possible sources per bit
  - eTPU, eMIOS, new virtual GPIO registers as possible bit source
  - Programmable inter-frame gap in continuous mode
  - Bit source selection allows microsecond channel downstream with command or data frames up to 32 bits
  - Microsecond channel dual receiver mode
- Combined serial interface (CSI) configuration where the DSPI operates in both SPI and DSI configurations interleaving DSI frames with SPI frames, giving priority to SPI frames

For queued operations, the SPI queues reside in system memory external to the DSPI. Data transfers between the memory and the DSPI FIFOs are accomplished through the use of the eDMA controller or through host software.

The DSPI supports these SPI features:

- Full-duplex, synchronous transfers
- Selectable LVDS Pads working at 40 MHz for SOUT and SCK pins
- Master and Slave Mode
- Buffered transmit operation using the TX FIFO with parameterized depth of 4 entries
- Buffered receive operation using the RX FIFO with parameterized depth of 4 entries
- TX and RX FIFOs can be disabled individually for low-latency updates to SPI queues
- Visibility into the TX and RX FIFOs for ease of debugging
- FIFO Bypass Mode for low-latency updates to SPI queues
- Programmable transfer attributes on a per-frame basis:
  - Parameterized number of transfer attribute registers (from two to eight)
  - Serial clock with programmable polarity and phase
  - Various programmable delays:
    - PCS to SCK delay

  - SCK to PCS delay
  - Delay between frames
  - Programmable serial frame size of 4 to 16 bits, expandable with software control
  - Continuously held chip select capability
- 6 Peripheral Chip Selects, expandable to 64 with external demultiplexer
- Deglitching support for up to 32 Peripheral Chip Selects with external demultiplexer
- DMA support for adding entries to TX FIFO and removing entries from RX FIFO:
  - TX FIFO is not full (TFFF)
  - RX FIFO is not empty (RFDF)
- 6 Interrupt conditions:
  - End of queue reached (EOQF)
  - TX FIFO is not full (TFFF)
  - Transfer of current frame complete (TCF)
  - Attempt to transmit with an empty Transmit FIFO (TFUF)
  - RX FIFO is not empty (RFDF)
  - FIFO Underrun (slave only and SPI mode, the slave is asked to transfer data when the TxFIFO is empty)
  - FIFO Overrun (serial frame received while RX FIFO is full)
- Modified transfer formats for communication with slower peripheral devices
- Continuous Serial Communications Clock (SCK)
- Power savings via support for Stop Mode
- Enhanced DSI logic to implement a 32-bit Timed Serial Bus (TSB) configuration, supporting the Microsecond Channel downstream frame format

The DSPIs also support these features unique to the DSI and CSI configurations:

- 2 sources of the serialized data:
  - eTPU_A and eMIOS output channels
  - Memory-mapped register in the DSPI
- Destinations for the deserialized data:
  - eTPU_A and eMIOS input channels
  - SIU External Interrupt Request inputs
  - Memory-mapped register in the DSPI
- Deserialized data is provided as Parallel Output signals and as bits in a memory-mapped register
- Transfer initiation conditions:
  - Continuous
  - Edge sensitive hardware trigger
  - Change in data
- Pin serialization/deserialization with interleaved SPI frames for control and diagnostics
- Continuous serial communications clock
- Support for parallel and serial chaining of up to four DSPI blocks

2.2.16 eSCI

The enhanced serial communications interface (eSCI) allows asynchronous serial communications with peripheral devices and other MCUs. It includes special support to interface to Local Interconnect Network (LIN) slave devices. The eSCI block provides the following features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format

3.5 208 MAPBGA ballmap (MPC5633M only)

Figure 6 shows the 208-pin MAPBGA ballmap for the MPC5633M (1024 KB flash memory) as viewed from above.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12-SDS	ALT_ MDO2	ALT_ MDO0	VRC33	VSS
B	VDD	VSS	AN38	AN21	AN0	AN4	REFBYPC	AN22	AN25	AN28	VDDA0	AN13-SDO	ALT_ MDO3	ALT_ MDO1	VSS	VDD
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14-SDI	AN15 FCK	VSS	ALT_ MSEO0	TCK
D	VRC33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH7	VSS	TMS	ALT_EVTO	NIC[1]
E	ETPUA30	ETPUA31	NC[2]	VDD									VDDE7	TDI	ALT_ EVTI	ALT_ MSEO1
F	ETPUA28	ETPUA29	ETPUA26	NC[2]									VDDEH6	TDO	ALT_MCKO	JCOMP
G	ETPUA24	ETPUA27	ETPUA25	ETPUA21			VSS	VSS	VSS	VSS			DSPI_B_ SOUT	DSPI_B_ PCS3	DSPI_B_ SIN	DSPI_B_ PCS0
H	ETPUA23	ETPUA22	ETPUA17	ETPUA18			VSS	VSS	VSS	VSS			NC[2]	DSPI_B_ PCS4	DSPI_B_ PCS2	DSPI_B_ PCS1
J	ETPUA20	ETPUA19	ETPUA14	ETPUA13			VSS	VSS	VSS	VSS			DSPI_B_ PCS5	SCI_A_TX	NC[2]	DSPI_B_ SCK
K	ETPUA16	ETPUA15	ETPUA7	VDDEH1			VSS	VSS	VSS	VSS			CAN_C_ TX	SCI_A_RX	RSTOUT	VDDREG
L	ETPUA12	ETPUA11	ETPUA6	ETPUA0									SCI_B_TX	CAN_C_ RX	WKPCFG	RESET
M	ETPUA10	ETPUA9	ETPUA1	ETPUA5									SCI_B_RX	PLLREF	BOOTCFG1	VSSPLL
N	ETPUA8	ETPUA4	ETPUA0	VSS	VDD	VRC33	EMIOS2	EMIOS10	VDDEH1/6[3]	EMIOS12	eTPUA19[4]	VRC33	VSS	VRCCTL	NIC[1]	EXTAL
P	ETPUA3	ETPUA2	VSS	VDD	NC[2]	VDDE7	NIC[1]	EMIOS8	eTPUA29[3]	eTPUA2[3]	eTPUA21[3]	CAN_A_ TX	VDD	VSS	NIC[1]	XTAL
R	NIC[1]	VSS	VDD	NC[2]	EMIOS4	NIC[1]	EMIOS9	EMIOS11	EMIOS14	eTPUA27[3]	EMIOS23	CAN_A_ RX	NC[2]	VDD	VSS	VDDPLL
T	VSS	VDD	NIC[1]	EMIOS0	NC[2]	GPIO219	eTPUA25[3]	NC[2]	NC[2]	eTPUA4[3]	eTPUA13[3]	NIC[1]	VDDE5	CLKOUT	VDD	VSS

1 Pins marked “NIC” have no internal connection.
2 Pins marked “NC” may be connected to internal circuitry. Connections to external circuits or other pins on this device can result in unpredictable system behavior or damage.
3 This ball may be changed to “NC” (no connection) in a future revision.
4 eTPU output only channel.

Figure 6. 208-pin MAPBGA ballmap (MPC5633M; top view)

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPBGA
CAL_ADDR[16][21] ALT_MDO[0][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	MDO / ALT_ADDR[12] / Low		—	17	A14
CAL_ADDR[17][21] ALT_MDO[1][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	ALT_MDO / CAL_ADDR[12] / Low		—	18	B14
CAL_ADDR[18][21] ALT_MDO[2][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	ALT_MDO / CAL_ADDR[12] / Low		—	19	A13
CAL_ADDR[19][21] ALT_MDO[3][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	ALT_MDO / CAL_ADDR[12] / Low		—	20	B13
CAL_ADDR[20:27] ALT_MDO[4:11]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] Fast	O / Low	ALT_MDO / CAL_ADDR[16] / Low		—	—	—
CAL_ADDR[28][21] ALT_$\overline{\text{MSEO}}$[0][12]	Calibration Address Bus Nexus Msg Start/End Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[17]	ALT_$\overline{\text{MSEO}}$[16] / CAL_ADDR[17]/ Low		—	118	C15
CAL_ADDR[29][21] ALT_$\overline{\text{MSEO}}$[1][12]	Calibration Address Bus Nexus Msg Start/End Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[17]	ALT_$\overline{\text{MSEO}}$[16] / CAL_ADDR[17]/ Low		—	117	E16
CAL_ADDR[30][21] ALT_$\overline{\text{EVTI}}$[12]	Calibration Address Bus Nexus Event In	PCR[345]	—	O I	VDDE12[13] VDDE7[14] Fast	—[18]	ALT_$\overline{\text{EVTI}}$ / CAL_ADDR[19]		—	116	E15
ALT_$\overline{\text{EVTO}}$	Nexus Event Out	PCR[344]	—	O	VDDE12[13] VDDE7[14] Fast	O / Low	ALT_$\overline{\text{EVTO}}$ / High		—	120	D15
ALT_MCKO	Nexus Msg Clock Out	PCR[344]	—	O	VDDE12[13] VDDE7[14] Fast	O / Low	ALT_MCKO / Enabled		—	14	F15
NEXUSCFG[11]	Nexus/Calibration bus selector	—	—	I	VDDE12 Fast	I / Down	NEXUSCFG / Down		—	—	—
CAL_$\overline{\text{CS}}$[0][11]	Calibration Chip Selects	PCR[336]	—	O	VDDE12 Fast	O / High	CAL_$\overline{\text{CS}}$ / High		—	—	—
CAL_$\overline{\text{CS}}$[2][11] CAL_ADDR[10]	Calibration Chip Selects Calibration Address Bus	PCR[338]	11 10	O O	VDDE12 Fast	O / High	CAL_$\overline{\text{CS}}$ / High		—	—	—

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPB GA
CAL_$\overline{CS}$[3][11] CAL_ADDR[11]	Calibration Chip Selects Calibration Address Bus	PCR[339]	11 10	O O	VDDE12 Fast	O / High	CAL_$\overline{CS}$ / High		—	—	—
CAL_DATA[0:9][11]	Calibration Data Bus	PCR[341]		I/O	VDDE12 Fast	– / Up	– / Up		—	—	—
CAL_DATA[10:15][11]	Calibration Data Bus	PCR[341]		I/O	VDDE12 Fast	– / Up	– / Up		—	—	—
CAL_$\overline{OE}$[11]	Calibration Output Enable	PCR[342]	—	O	VDDE12 Fast	O / High	CAL_$\overline{OE}$ / High		—	—	—
CAL_RD_$\overline{WR}$[11]	Calibration Read/Write	PCR[342]	—	O	VDDE12 Fast	O / High	CAL_RD_$\overline{WR}$ /High		—	—	—
CAL_$\overline{TS}$_ALE[11]	Calibration Transfer Start Address Latch Enable	PCR[343]	TS=0b1 ALE=0b0	O O	VDDE12 Fast	O / High	CAL_$\overline{TS}$ / High		—	—	—
CAL_$\overline{WE}$_BE[0:1][11]	Calibration Write Enable Byte Enable	PCR[342]	—	O	VDDE12 Fast	O / High	CAL_$\overline{WE}$ / High		—	—	—
NEXUS[20]											
$\overline{EVTI}$[21] eTPU_A[2] GPIO[231]	Nexus Event In eTPU A Ch. GPIO	PCR[231]	01 10 00	I O I/O	VDDEH7 Multi-V	– / –	– / –		103	126	P10
$\overline{EVTO}$ [21] eTPU_A[4] GPIO[227]	Nexus Event Out eTPU A Ch. GPIO	PCR[227]	01[22] 10 00	O O I/O	VDDEH7 Multi-V	I / Up	I / Up		106	129	T10
MCKO[21] GPIO[219]	Nexus Msg Clock Out GPIO	PCR[219]	N/A[22] 00	O I/O	VDDEH7 Multi-V	– / –	– / –		99	122	T6
MDO[0][21] eTPU_A[13] GPIO[220]	Nexus Msg Data Out eTPU A Ch. GPIO	PCR[220]	01 10 00	O O I/O	VDDEH7 Multi-V	– / –	– / –		110	135	T11
MDO[1][21] eTPU_A[19] GPIO[221]	Nexus Msg Data Out eTPU A Ch. GPIO	PCR[221]	01[22] 10 00	O O I/O	VDDEH7 Multi-V	– / –	– / –		111	136	N11
MDO[2][21] eTPU_A[21] GPIO[222]	Nexus Msg Data Out eTPU A Ch. GPIO	PCR[222]	01[22] 10 00	O O I/O	VDDEH7 Multi-V	– / –	– / –		112	137	P11

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPBGA
DSPI_B_PCS[5] DSPI_C_PCS[0] GPIO[110]	DSPI_B Periph Chip Select DSPI_C Periph Chip Select GPIO	PCR[110]	01 10 00	O O I/O	VDDEH6b Medium	– / Up	– / Up		87	104	J13
eQADC											
AN[0][27] DAN0+	Single Ended Analog Input Positive Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[0] / –		143	172	B5
AN[1][27] DAN0-	Single Ended Analog Input Negative Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[1] / –		142	171	A6
AN[2][27] DAN1+	Single Ended Analog Input Positive Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[2] / –		141	170	D6
AN[3][27] DAN1-	Single Ended Analog Input Negative Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[3] / –		140	169	C7
AN[4][27] DAN2+	Single Ended Analog Input Positive Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[4] / –		139	168	B6
AN[5][27] DAN2-	Single Ended Analog Input Negative Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[5] / –		138	167	A7
AN[6][27] DAN3+	Single Ended Analog Input Positive Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[6] / –		137	166	D7
AN[7][27] DAN3-	Single Ended Analog Input Negative Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[7] / –		136	165	C8
AN[8]	See AN[38]-AN[8]-ANW										
AN[9] ANX	Single Ended Analog Input External Multiplexed Analog Input	—	—	I I	VDDA	I / –	AN[9] / –		5	5	A2
AN[10]	See AN[39]-AN[10]-ANY										
AN[11] ANZ	Single Ended Analog Input External Multiplexed Analog Input	—	—	I I	VDDA	I / –	AN[11] / –		4	4	A3
AN[12] MA[0] ETPU_A[19] $\overline{SDS}$	Single Ended Analog Input Mux Address ETPU_A Ch. eQADC Serial Data Strobe	PCR[215]	011 010 100 000	I O O O	VDDEH7	I / –	AN[12] / –		119	148	A12

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPBGA
AN[38]-AN[8]-ANW	Single Ended Analog Input Multiplexed Analog Input	—	—	I	VDDA	I / –	AN[38] / –		9	9	B3
AN[39]-AN[10]-ANY	Single Ended Analog Input Multiplexed Analog Input	—	—	I	VDDA	I / –	AN[39] / –		8	8	D2
VRH	Voltage Reference High	—	—	I	VDDA	– / –	VRH		134	163	A8
VRL	Voltage Reference Low	—	—	I	VSSA0	– / –	VRL		133	162	A9
REFBYPC	Bypass Capacitor Input	—	—	I	VRL	– / –	REFBYPC		135	164	B7
eTPU2											
eTPU_A[0] eTPU_A[12] eTPU_A[19] GPIO[114]	eTPU_A Ch. eTPU_A Ch. eTPU_A Ch. GPIO	PCR[114]	011 010 100 000	I/O O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		52	61	L4, N3
eTPU_A[1] eTPU_A[13] GPIO[115]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[115]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		51	60	M3
eTPU_A[2] eTPU_A[14] GPIO[116]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[116]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		50	59	P2
eTPU_A[3] eTPU_A[15] GPIO[117]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[117]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		49	58	P1
eTPU_A[4] eTPU_A[16] GPIO[118]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[118]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		47	56	N2
eTPU_A[5] eTPU_A[17] DSPI_B_SCK_LVDS- GPIO[119]	eTPU_A Ch. eTPU_A Ch. DSPI_B CLOCK LVDS- GPIO	PCR[119]	001 010 100 000	I/O O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		45	54	M4
eTPU_A[6] eTPU_A[18] DSPI_B_SCK_LVDS+ GPIO[120]	eTPU_A Ch. eTPU_A Ch. DSPI_B Clock LVDS+ GPIO	PCR[120]	001 010 100 000	I/O O O I/O	VDDEH1b Medium	– / WKPCFG	– / WKPCFG		44	53	L3

- B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

4.4 Electromagnetic Interference (EMI) characteristics

Table 11. EMI testing specifications[1]

Symbol	Parameter	Conditions	f_{OSC}/f_{BUS}	Frequency	Level (Typ)	Unit
Radiated Emissions	V_{EME}	Device Configuration, test conditions and EM testing per standard IEC61967-2; Supply Voltage = 5.0V DC, Ambient Temperature = 25°C, Worst-case Orientation	Oscillator Frequency = 8 MHz; System Bus Frequency = 80 MHz; No PLL Frequency Modulation	150 kHz – 50 MHz	26	dBμV
				50–150 MHz	24	
				150–500 MHz	24	
				500–1000 MHz	21	
				IEC Level	K	—
			Oscillator Frequency = 8 MHz; System Bus Frequency = 80 MHz; 1% PLL Frequency Modulation	150 kHz – 50 MHz	20	dBμV
				50–150 MHz	19	
				150–500 MHz	14	
				500–1000 MHz	7	
				IEC Level	L	—

1 IEC Classification Level: L = 24dBuV; K = 30dBuV.

4.5 Electromagnetic static discharge (ESD) characteristics

Table 12. ESD ratings[1,2]

Symbol		Parameter	Conditions	Value	Unit
—	SR	ESD for Human Body Model (HBM)	—	2000	V
R1	SR	HBM circuit description	—	1500	Ω
C	SR		—	100	pF
—	SR	ESD for field induced charge Model (FCDM)	All pins	500	V
			Corner pins	750	
—	SR	Number of pulses per pin	Positive pulses (HBM)	1	—
			Negative pulses (HBM)	1	—
—	SR	Number of pulses	—	1	—

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature.”

4.6.2 Recommended power transistors

The following NPN transistors are recommended for use with the on-chip voltage regulator controller: ON Semiconductor™ BCP68T1 or NJD2873 as well as Philips Semiconductor™ BCP68. The collector of the external transistor is preferably connected to the same voltage supply source as the output stage of the regulator.

Table 19. Recommended operating characteristics

Symbol	Parameter	Value	Unit
h_{FE} (β)	DC current gain (Beta)	60 – 550	—
P_D	Absolute minimum power dissipation	>1.0 (1.5 preferred)	W
I_{CMaxDC}	Minimum peak collector current	1.0	A
VCE_{SAT}	Collector-to-emitter saturation voltage	200–600[1]	mV
V_{BE}	Base-to-emitter voltage	0.4–1.0	V

[1] Adjust resistor at bipolar transistor collector for 3.3 V/5.0 V to avoid VCE < VCE_{SAT}

4.7 Power up/down sequencing

There is no power sequencing required among power sources during power up and power down, in order to operate within specification but use of the following sequence is strongly recommended when the internal regulator is bypassed:

5 V → 3.3 V and 1.2 V

This is also the normal sequence when the internal regulator is enabled.

Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies according to table Table 20 for all pins with fast pads and Table 21 for all pins with medium, slow and multi-voltage pads.[1]

Table 20. Power sequence pin states for fast pads

V_{DDE}	V_{RC33}	V_{DD}	Fast (pad_fc)
LOW	X	X	LOW
V_{DDE}	LOW	X	HIGH
V_{DDE}	V_{RC33}	LOW	HIGH IMPEDANCE
V_{DDE}	V_{RC33}	V_{DD}	FUNCTIONAL

Table 21. Power sequence pin states for medium, slow and multi-voltage pads

V_{DDEH}	V_{DD}	Medium (pad_msr_hv) Slow (pad_ssr_hv) Multi-voltage (pad_multv_hv)
LOW	X	LOW
V_{DDEH}	LOW	HIGH IMPEDANCE
V_{DDEH}	V_{DD}	FUNCTIONAL

1.If an external 3.3V external regulator is used to supply current to the 1.2V pass transistor and this supply also supplies current for the other 3.3V supplies, then the 5V supply must always be greater than or equal to the external 3.3V supply.

Table 22. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
V_{OH_LS}	CC	P	Multi-voltage pad I/O output high voltage in low-swing mode[10,11,12,13,17]	I_{OH_LS} = 0.5 mA Min V_{DDEH} = 4.75 V	2.1	—	3.7	V
V_{OH_HS}	CC	P	Multi-voltage pad I/O output high voltage in high-swing mode[17]	—	0.8 V_{DDEH}	—	—	V
V_{HYS_S}	CC	C	Slow/medium/multi-voltage I/O input hysteresis	—	0.1 * V_{DDEH}	—	—	V
V_{HYS_F}	CC	C	Fast I/O input hysteresis	—	0.1 * V_{DDE}	—	—	V
V_{HYS_LS}	CC	C	Low-Swing-Mode Multi-Voltage I/O Input Hysteresis	hysteresis enabled	0.25	—	—	V
I_{DD}+I_{DDPLL}[19]	CC	P	Operating current 1.2 V supplies	V_{DD} = 1.32 V, 80 MHz	—	—	195	mA
	CC	P		V_{DD} = 1.32 V, 60 MHz	—	—	135	
	CC	P		V_{DD} = 1.32 V, 40 MHz	—	—	98	
I_{DDSTBY}	CC	T	Operating current 1 V supplies	T_J = 25 °C	—	—	80	µA
	CC	T		T_J = 55 °C	—	—	100	µA
$I_{DDSTBY150}$	CC	P	Operating current	T_J=150 °C	—	—	700	µA
I_{DDSLOW} I_{DDSTOP}	CC	P	V_{DD} low-power mode operating current @ 1.32 V	Slow mode[20]	—	—	50	mA
		C		Stop mode[21]	—	—	50	
I_{DD33}	CC	T	Operating current 3.3 V supplies @ 80 MHz	V_{RC33}[4,22]	—	—	70	mA
I_{DDA} I_{REF} I_{DDREG}	CC	P	Operating current 5.0 V supplies @ 80 MHz	V_{DDA}	—	—	30	mA
		P		Analog reference supply current	—	—	1.0	
		C		V_{DDREG}	—	—	70	

Table 27. PLLMRFM electrical specifications[1]

(V_{DDPLL} =1.14 V to 1.32 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					min	max	
V_{ILEXT}	CC	T	EXTAL input low voltage	Crystal Mode[14], 0.65≤Vxtal≤1.25V[15]	—	Vxtal – 0.4	V
		T		External Reference[14, 16]	0	V_{RC33}/2 – 0.4	
—	CC	T	XTAL load capacitance[12]	4 MHz	5	30	pF
				8 MHz	5	26	
				12 MHz	5	23	
				16 MHz	5	19	
				20 MHz	5	16	
t_{lpll}	CC	P	PLL lock time [12, 17]	—	—	200	µs
t_{dc}	CC	T	Duty cycle of reference	—	40	60	%
f_{LCK}	CC	T	Frequency LOCK range	—	–6	6	% f_{sys}
f_{UL}	CC	T	Frequency un-LOCK range	—	–18	18	% f_{sys}
f_{CS} f_{DS}	CC	D	Modulation Depth	Center spread	±0.25	±4.0	%f_{sys}
		D		Down Spread	–0.5	–8.0	
f_{MOD}	CC	D	Modulation frequency[18]	—	—	100	kHz

1 All values given are initial design targets and subject to change.

2 Considering operation with PLL not bypassed.

3 f_{VCO} is calculated as follows:

— In Legacy Mode f_{VCO} = ($f_{crystal}$ / (PREDIV + 1)) * (4 * (MFD + 4))

— In Enhanced Mode fvco = ($f_{crystal}$ / (EPREDIV + 1)) * (EMFD + 4)

4 All internal registers retain data at 0 Hz.

5 “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.

6 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.

7 f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.

8 This value is determined by the crystal manufacturer and board design.

9 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.

10 Proper PC board layout procedures must be followed to achieve specifications.

11 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).

12 This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits. For a 20 MHz crystal the maximum load should be 17 pF.

13 Proper PC board layout procedures must be followed to achieve specifications.

14 This parameter is guaranteed by design rather than 100% tested.

Table 29. eQADC conversion specifications (operating) (continued)

Symbol		C	Parameter		Value		Unit
					min	max	
TUE8	CC	C	Total unadjusted error (TUE) at 8 MHz[9]		–4	4	Counts
TUE16	CC	C	Total unadjusted error at 16 MHz[10]		–8	8	Counts
SNR	CC	T	Signal to Noise Ratio[11]		55.2		dB
THD	CC	T	Total Harmonic Distorsion		70.0		dB
SFDR	CC	T	Spurious Free Dynamic Range		65.0		dB
SINAD	CC	T	Signal to Noise and Distorsion		55.0		dB
ENOB	CC	T	Effective Number of Bits		8.8		Counts
GAINVGA1	CC	–	Variable gain amplifier accuracy (gain=1)[12]				
	CC	C	INL	8 MHz ADC	–4	4	Counts[13]
	CC	C		16 MHz ADC	–8	8	Counts
	CC	C	DNL	8 MHz ADC	–3[14]	3[14]	Counts
	CC	C		16 MHz ADC	–3[14]	3[14]	Counts
GAINVGA2	CC	–	Variable gain amplifier accuracy (gain=2)[12]				
	CC	D	INL	8 MHz ADC	–5	5	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–3	3	Counts
	CC	D		16 MHz ADC	–3	3	Counts
GAINVGA4	CC	–	Variable gain amplifier accuracy (gain=4)[12]				
	CC	D	INL	8 MHz ADC	–7	7	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–4	4	Counts
	CC	D		16 MHz ADC	–4	4	Counts
$DIFF_{max}$	CC	C	Maximum differential voltage (DANx+ - DANx-) or (DANx- - DANx+)	PREGAIN set to 1X setting	–	(VRH - VRL)/2	V
$DIFF_{max2}$	CC	C		PREGAIN set to 2X setting	–	(VRH - VRL)/4	V
$DIFF_{max4}$	CC	C		PREGAIN set to 4X setting	–	(VRH - VRL)/8	V
$DIFF_{cmv}$	CC	C	Differential input Common mode voltage (DANx- + DANx+)/2[15]		(VRH - VRL)/2 - 5%	(VRH - VRL)/2 + 5%	V

1 Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions.Delay from power up to full accuracy = 8 ms.

2 At $V_{RH} – V_{RL}$ = 5.12 V, one count = 1.25 mV. Without using pregain.

3 Below disruptive current conditions, the channel being stressed has conversion values of 0x3FF for analog inputs greater then V_{RH} and 0x0 for values less then V_{RL}. Other channels are not affected by non-disruptive conditions.

Table 32. Flash module life

Symbol		Parameter	Conditions	Value		Unit
				Min	Typ	
P/E	C	Number of program/erase cycles per block for 16 Kbyte blocks over the operating temperature range (T_J)	—	100,000	—	cycles
P/E	C	Number of program/erase cycles per block for 32 and 64 Kbyte blocks over operating temperature range (T_J)	—	10,000	100,000	cycles
P/E	C	Number of program/erase cycles per block for 128 Kbyte blocks over the operating temperature range (T_J)	—	1,000	100,000	cycles
Retention	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0 – 1,000 P/E cycles	20	—	years
			Blocks with 10,000 P/E cycles	10	—	years
			Blocks with 100,000 P/E cycles	5	—	years

[1] Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

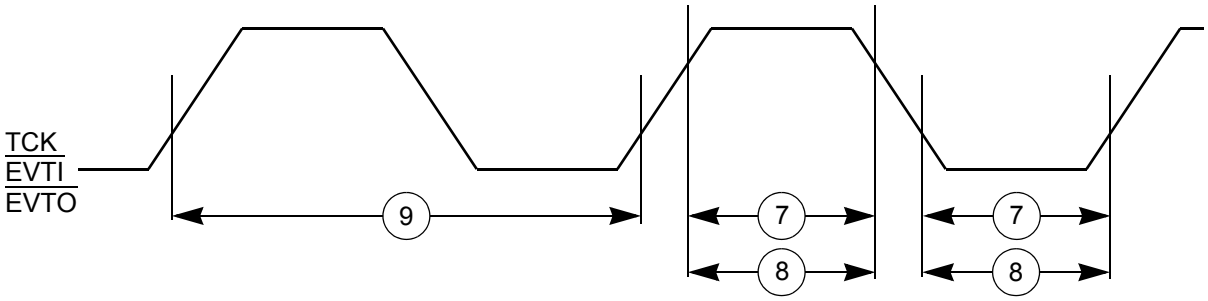


Figure 14. Nexus event trigger and test clock timings

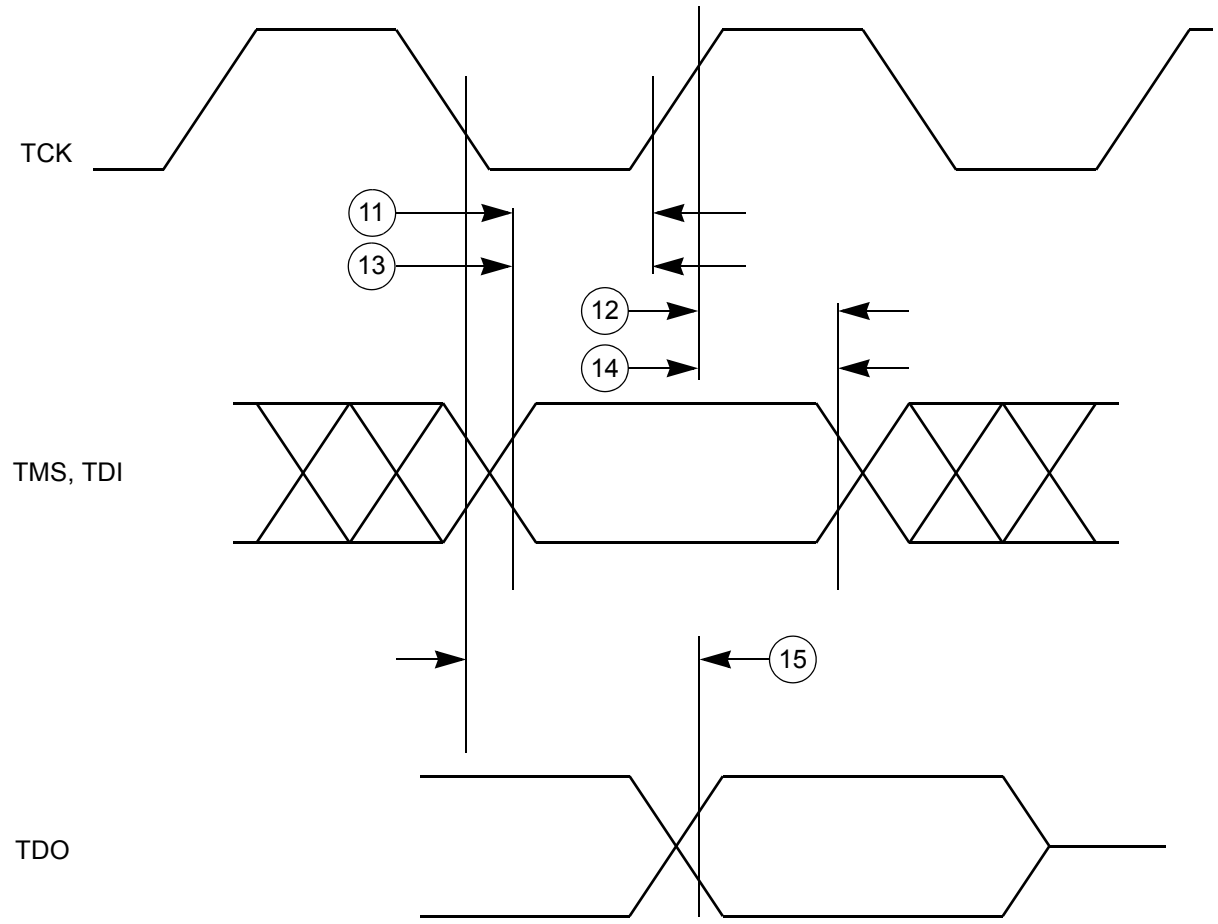
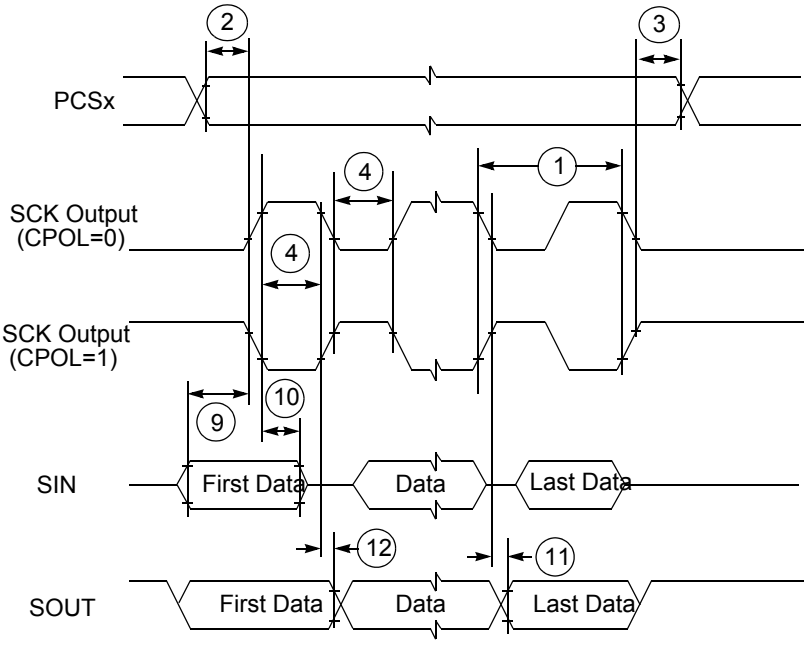
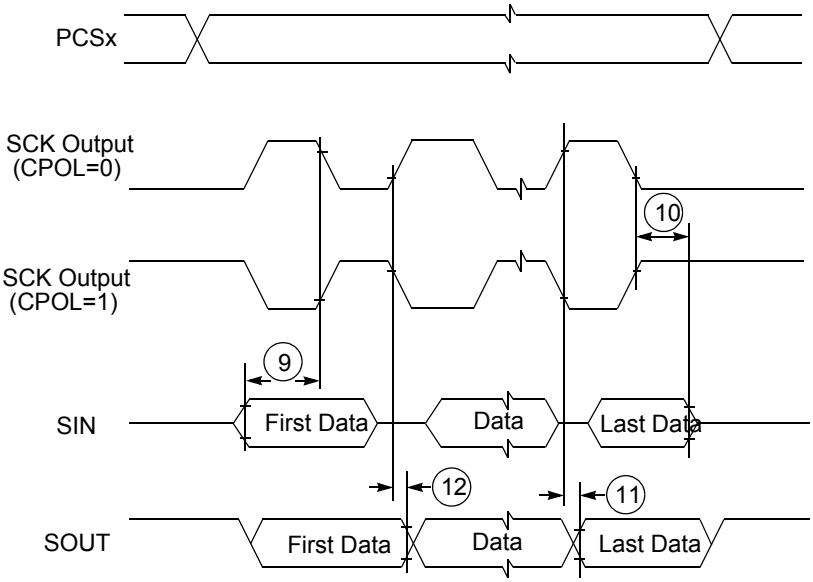


Figure 15. Nexus TDI, TMS, TDO timing



These numbers reference Table 40.

Figure 20. DSPI classic SPI timing – master, CPHA = 0



These numbers reference Table 40.

Figure 21. DSPI classic SPI timing – master, CPHA = 1

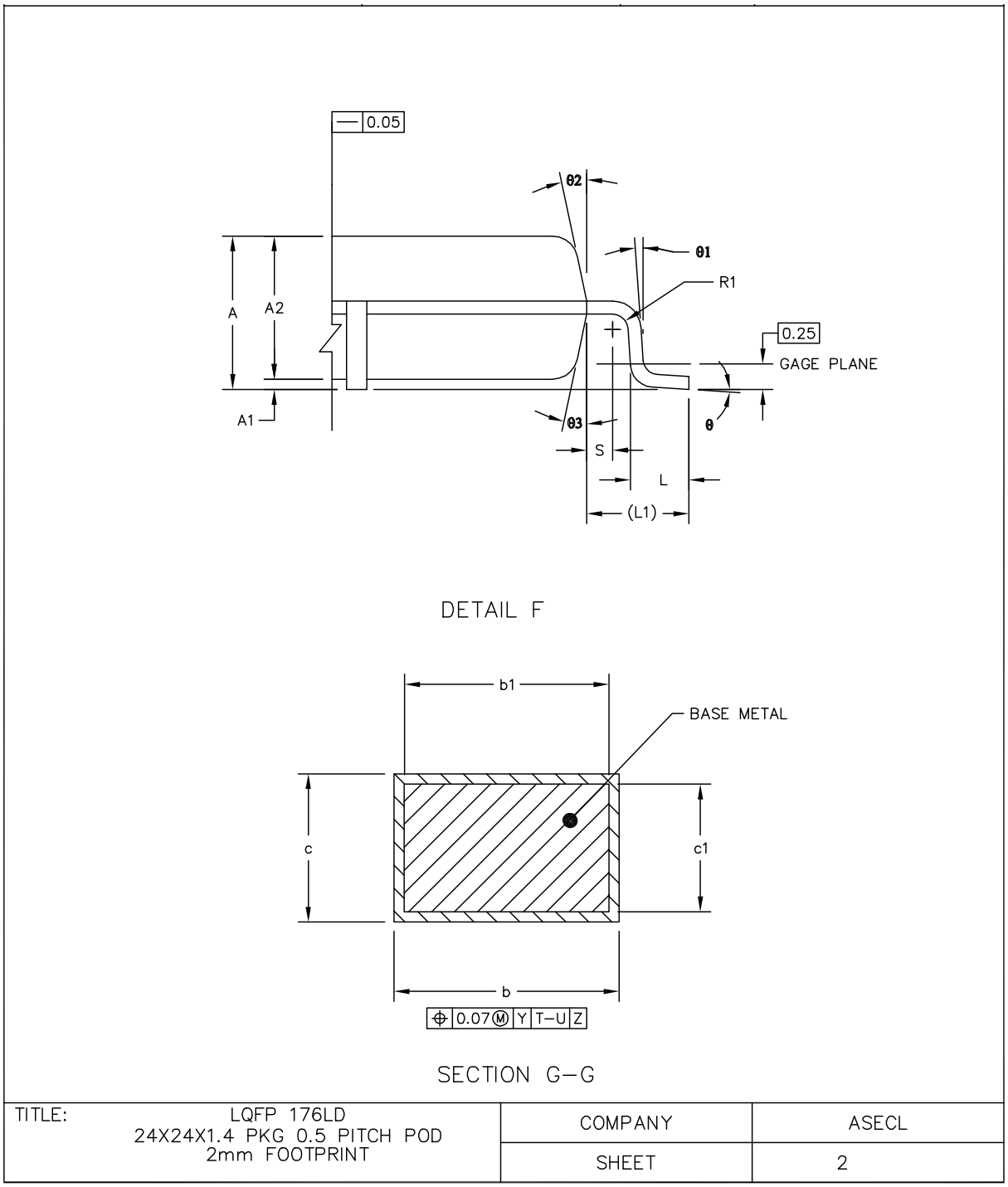
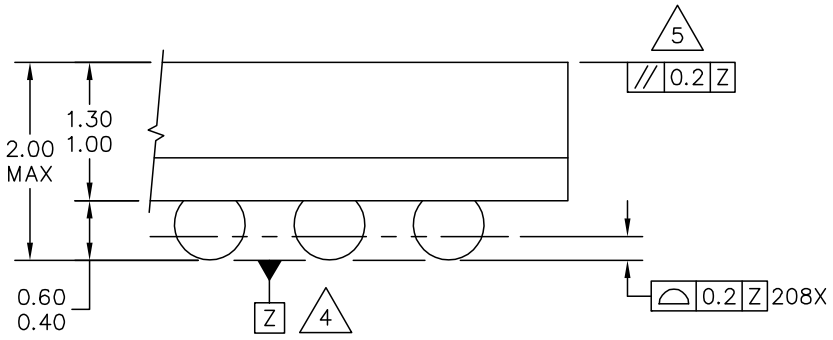


Figure 34. 176 LQFP package mechanical drawing (part 2)

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ARS23882W
		PAGE: 1159A
	DO NOT SCALE THIS DRAWING	REV: D



DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH	CASE NUMBER: 1159A–01	
	STANDARD: JEDEC MO–151 AAF–1	
	PACKAGE CODE: 5253	SHEET: 2 OF 3

Figure 37. 208 MAPBGA package mechanical drawing (part 2)

Table 43. Revision history (continued)

Revision	Date	Description of Changes
Rev 9	05/2012	In Section 4.6.1, “Regulator example • Updated ,Figure 7 “Core voltage regulator controller external components preferred configuration” to show R_C, R_B, R_E, C_C, C_B, C_E, C_D and C_{REG}. • Added Table 15 “Required external PMC component values”, Table 16 “Network 1 component values”, Table 17 “Network 2 component values” and Table 18 “Network 3 component values”. Updated Table 1: Number of eMIOS channels changed from ‘8’ to ‘16’ for MPC5632M. In Section 4.2, “Maximum ratings, Table 7 • V_{FLASH} maximum value changed from 3.6V to 5.5V and changed table note3 to: “The V_{FLASH} supply is connected to V_{DDEH}” • Removed table note 4, “Allowed 5.3 V for 10 hours cumulative time, remaining time at 3.3 V +10%” In Section 4.12, “eQADC electrical characteristics: • Added note. • In Table 29, additional five parameters added (SNR, THD, SFDR, SINAD and ENOB) and added footnotes # 9,10 and 11.