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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z3
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5633mf1mlu60

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— Four pairs of differential analog input channels
— Full duplex synchronous serial interface to an external device
  – Has a free-running clock for use by the external device
  – Supports a 26-bit message length
  – Transmits a null message when there are no triggered CFIFOs with commands bound for external CBuffers, or when there are triggered CFIFOs with commands bound for external CBuffers but the external CBuffers are full
— Parallel Side Interface to communicate with an on-chip companion module
— Zero jitter triggering for queue 0. (Queue 0 trigger causes current conversion to be aborted and the queued conversions in the CBUFFER to be bypassed. Delay from Trigger to start of conversion is 13 system clocks + 1 ADC clock.)
— eQADC Result Streaming. Generation of a continuous stream of ADC conversion results from a single eQADC command word. Controlled by two different trigger signals; one to define the rate at which results are generated and the other to define the beginning and ending of the stream. Used to digitize waveforms during specific time/angle windows, e.g., engine knock sensor sampling.
— Angular Decimation. The ability of the eQADC to sample an analog waveform in the time domain, perform Finite Impulse Response (FIR) or Infinite Impulse Response (IIR) filtering also in the time domain, but to down sample the results in the angle domain. Resulting in a time domain filtered result at a given engine angle.
— Priority Based CFIFOs
  – Supports six CFIFOs with fixed priority. The lower the CFIFO number, the higher its priority. When commands of distinct CFIFOs are bound for the same CBuffer, the higher priority CFIFO is always served first.
  – Supports software and several hardware trigger modes to arm a particular CFIFO
  – Generates interrupt when command coherency is not achieved
— External Hardware Triggers
  – Supports rising edge, falling edge, high level and low level triggers
  – Supports configurable digital filter
— Supports four external 8-to-1 muxes which can expand the input channel number from 34[1] to 59

- Two deserial serial peripheral interface modules (DSPI)
  — SPI
    – Full duplex communication ports with interrupt and DMA request support
    – Supports all functional modes from QSPI subblock of QSMCM (MPC5xx family)
    – Support for queues in RAM
    – 6 chip selects, expandable to 64 with external demultiplexers
    – Programmable frame size, baud rate, clock delay and clock phase on a per frame basis
    – Modified SPI mode for interfacing to peripherals with longer setup time requirements
    – LVDS option for output clock and data to allow higher speed communication
  — Deserial serial interface (DSI)
    – Pin reduction by hardware serialization and deserialization of eTPU, eMIOS channels and GPIO
    – 32 bits per DSPI module
    – Triggered transfer control and change in data transfer control (for reduced EMI)
    – Compatible with Microsecond Channel Version 1.0 downstream
- Two enhanced serial communication interface (eSCI) modules
  — UART mode provides NRZ format and half or full duplex interface
  — eSCI bit rate up to 1 Mbps

1. 176-pin and 208-pin packages have 34 input channels; 144-pin package has 32.
1. 176-pin and 208-ball packages.

Branch Address adder to minimize delays during change of flow operations. Sequential prefetching is performed to ensure a supply of instructions into the execution pipeline. Branch target prefetching is performed to accelerate taken branches. Prefetched instructions are placed into an instruction buffer capable of holding six instructions.

Branches can also be decoded at the instruction buffer and branch target addresses calculated prior to the branch reaching the instruction decode stage, allowing the branch target to be prefetched early. When a branch is detected at the instruction buffer, a prediction may be made on whether the branch is taken or not. If the branch is predicted to be taken, a target fetch is initiated and its target instructions are placed in the instruction buffer following the branch instruction. Many branches take zero cycle to execute by using branch folding. Branches are folded out from the instruction execution pipe whenever possible. These include unconditional branches and conditional branches with condition codes that can be resolved early.

Conditional branches which are not taken and not folded execute in a single clock. Branches with successful target prefetching which are not folded have an effective execution time of one clock. All other taken branches have an execution time of two clocks. Memory load and store operations are provided for byte, halfword, and word (32-bit) data with automatic zero or sign extension of byte and halfword load data as well as optional byte reversal of data. These instructions can be pipelined to allow effective single cycle throughput. Load and store multiple word instructions allow low overhead context save and restore operations. The load/store unit contains a dedicated effective address adder to allow effective address generation to be optimized. Also, a load-to-use dependency does not incur any pipeline bubbles for most cases.

The Condition Register unit supports the condition register (CR) and condition register operations defined by the Power Architecture. The condition register consists of eight 4-bit fields that reflect the results of certain operations, such as move, integer and floating-point compare, arithmetic, and logical instructions, and provide a mechanism for testing and branching. Vectored and autovectored interrupts are supported by the CPU. Vectored interrupt support is provided to allow multiple interrupt sources to have unique interrupt handlers invoked with no software overhead.

The hardware floating-point unit utilizes the IEEE-754 single-precision floating-point format and supports single-precision floating-point operations in a pipelined fashion. The general purpose register file is used for source and destination operands, thus there is a unified storage model for single-precision floating-point data types of 32 bits and the normal integer type. Single-cycle floating-point add, subtract, multiply, compare, and conversion operations are provided. Divide instructions are multi-cycle and are not pipelined.

The Signal Processing Extension (SPE) Auxiliary Processing Unit (APU) provides hardware SIMD operations and supports a full complement of dual integer arithmetic operation including Multiply Accumulate (MAC) and dual integer multiply (MUL) in a pipelined fashion. The general purpose register file is enhanced such that all 32 of the GPRs are extended to 64 bits wide and are used for source and destination operands, thus there is a unified storage model for 32×32 MAC operations which generate greater than 32-bit results.

The majority of both scalar and vector operations (including MAC and MUL) are executed in a single clock cycle. Both scalar and vector divides take multiple clocks. The SPE APU also provides extended load and store operations to support the transfer of data to and from the extended 64-bit GPRs. This SPE APU is fully binary compatible with e200z6 SPE APU used in MPC5554 and MPC5553.

The CPU includes support for Variable Length Encoding (VLE) instruction enhancements. This enables the classic Power Architecture instruction set to be represented by a modified instruction set made up from a mixture of 16- and 32-bit instructions. This results in a significantly smaller code size footprint without noticeably affecting performance. The Power Architecture instruction set and VLE instruction set are available concurrently. Regions of the memory map are designated as PPC or VLE using an additional configuration bit in each of Table Look-aside Buffers (TLB) entries in the MMU.

The CPU core is enhanced by the addition of two additional interrupt sources; Non-Maskable Interrupt and Critical Interrupt. These two sources are routed directly from package pins, via edge detection logic in the SIU to the CPU, bypassing completely the Interrupt Controller. Once the edge detection logic is programmed, it cannot be disabled, except by reset. The non-maskable Interrupt is, as the name suggests, completely un-maskable and when asserted will always result in the immediate execution of the respective interrupt service routine. The non-maskable interrupt is not guaranteed to be recoverable. The Critical Interrupt is very similar to the non-maskable interrupt, but it can be masked by other exceptional interrupts in the CPU and is guaranteed to be recoverable (code execution may be resumed from where it stopped).

  - Auxiliary Output port
    - 1 MCKO (message clock out) pin
    - 4 MDO (message data out) pins
    - 2 $\overline{\text{MSEO}}$ (message start/end out) pins
    - 1 $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port
    - 1 $\overline{\text{EVTI}}$ (event in) pin
- 17-pin Full Port interface in calibration package used on VertiCal boards
  - 3.3 V interface
  - Auxiliary Output port
    - 1 MCKO (message clock out) pin
    - 4 (reduced port mode) or 12 (full port mode) MDO (message data out) pins; 8 extra full port pins shared with calibration bus
    - 2 $\overline{\text{MSEO}}$ (message start/end out) pins
    - 1 $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port
    - 1 $\overline{\text{EVTI}}$ (event in) pin
- Host processor (e200) development support features
  - IEEE-ISTO 5001-2003 standard class 2 compliant
  - Program trace via branch trace messaging (BTM). Branch trace messaging displays program flow discontinuities (direct branches, indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus, static code may be traced.
  - Watchpoint trigger enable of program trace messaging
  - Data Value Breakpoints (JTAG feature of the e200z335 core): allows CPU to be halted when the CPU writes a specific value to a memory location
    - 4 data value breakpoints
    - CPU only
    - Detects ‘equal’ and ‘not equal’
    - Byte, half word, word (naturally aligned)

NOTE

This feature is imprecise due to CPU pipelining.

  - Subset of Power Architecture software debug facilities with OnCE block (Nexus class 1 features)
- eTPU development support features
  - IEEE-ISTO 5001-2003 standard class 1 compliant for the eTPU
  - Nexus based breakpoint configuration and single step support (JTAG feature of the eTPU)
- Run-time access to the on-chip memory map via the Nexus read/write access protocol. This feature supports accesses for run-time internal visibility, calibration variable acquisition, calibration constant tuning, and external rapid prototyping for powertrain automotive development systems.
- All features are independently configurable and controllable via the IEEE 1149.1 I/O port
- Power-on-reset status indication during reset via MDO[0] in disabled and reset modes

2.2.20.2 JTAG

The JTAGC (JTAG Controller) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPBGA
AN[38]-AN[8]-ANW	Single Ended Analog Input Multiplexed Analog Input	—	—	I	VDDA	I / –	AN[38] / –		9	9	B3
AN[39]-AN[10]-ANY	Single Ended Analog Input Multiplexed Analog Input	—	—	I	VDDA	I / –	AN[39] / –		8	8	D2
VRH	Voltage Reference High	—	—	I	VDDA	– / –	VRH		134	163	A8
VRL	Voltage Reference Low	—	—	I	VSSA0	– / –	VRL		133	162	A9
REFBYPC	Bypass Capacitor Input	—	—	I	VRL	– / –	REFBYPC		135	164	B7
eTPU2											
eTPU_A[0] eTPU_A[12] eTPU_A[19] GPIO[114]	eTPU_A Ch. eTPU_A Ch. eTPU_A Ch. GPIO	PCR[114]	011 010 100 000	I/O O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		52	61	L4, N3
eTPU_A[1] eTPU_A[13] GPIO[115]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[115]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		51	60	M3
eTPU_A[2] eTPU_A[14] GPIO[116]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[116]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		50	59	P2
eTPU_A[3] eTPU_A[15] GPIO[117]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[117]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		49	58	P1
eTPU_A[4] eTPU_A[16] GPIO[118]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[118]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		47	56	N2
eTPU_A[5] eTPU_A[17] DSPI_B_SCK_LVDS- GPIO[119]	eTPU_A Ch. eTPU_A Ch. DSPI_B CLOCK LVDS- GPIO	PCR[119]	001 010 100 000	I/O O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		45	54	M4
eTPU_A[6] eTPU_A[18] DSPI_B_SCK_LVDS+ GPIO[120]	eTPU_A Ch. eTPU_A Ch. DSPI_B Clock LVDS+ GPIO	PCR[120]	001 010 100 000	I/O O O I/O	VDDEH1b Medium	– / WKPCFG	– / WKPCFG		44	53	L3

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPBGA
VSTBY	Power Supply for Standby RAM	—	—	I	VSTBY	I / –	—		12	12	C1
VRC33	3.3V Voltage Regulator Bypass Capacitor	—	—	O	VRC33	O / –	—		13	13	A15, D1, N6, N12
VRCCTL	Voltage Regulator Control Output	—	—	O	NA	O / –	—		11	11	N14
VDDA[34]	Analog Power Input for eQADC	—	—	I	VDDA (5.0 V)	I / –	—		6	6	—
VDDA0	Analog Power Input for eQADC	—	—	I	VDDA	I / –	—		—	—	B11
VSSA0	Analog Ground Input for eQADC	—	—	I	VSSA	I / –	—		—	—	A11
VDDA1	Analog Power Input for eQADC	—	—	I	VDDA	I / –	—		—	—	A4
VSSA1	Analog Ground Input for eQADC	—	—	I	VSSA	I / –	—		—	—	A5
VSSA[35]	Analog Ground Input for eQADC	—	—	I	VSSA	I / –	—		7	7	—
VDDREG	Voltage Regulator Supply	—	—	I	VDDREG (5.0 V)	I / –	—		10	10	K16
VDD	Internal Logic Supply Input	—	—	I	VDD (1.2 V)	I / –	—		26, 53, 86, 120	33, 62, 103, 149	B1, B16, C2, D3, E4, N5, P4, P13, R3, R14, T2, T15

Table 4. Signal details (continued)

Signal	Module or Function	Description
CAL_RD_$\overline{WR}$	Calibration Bus	RD_$\overline{WR}$ indicates whether the current transaction is a read access or a write access.
CAL_$\overline{TS}$_ALE	Calibration Bus	The Transfer Start signal ($\overline{TS}$) is asserted by the MPC5634M to indicate the start of a transfer. The Address Latch Enable (ALE) signal is used to demultiplex the address from the data bus.
CAL_$\overline{EVTO}$	Calibration Bus	Nexus Event Out
CAL_MCKO	Calibration Bus	Nexus Message Clock Out
NEXUSCFG	Nexus/Calibration Bus	Nexus/Calibration Bus selector
eMIOS[0:23]	eMIOS	eMIOS I/O channels
AN[0:39]	eQADC	Single-ended analog inputs for analog-to-digital converter
FCK	eQADC	eQADC free running clock for eQADC SSI.
MA[0:2]	eQADC	These three control bits are output to enable the selection for an external Analog Mux for expansion channels.
REFBYPC	eQADC	Bypass capacitor input
SDI	eQADC	Serial data in
SDO	eQADC	Serial data out
SDS	eQADC	Serial data select
VRH	eQADC	Voltage reference high input
VRL	eQADC	Voltage reference low input
SCI_A_RX SCI_B_RX	eSCI_A – eSCI_B	eSCI receive
SCI_A_TX SCI_B_TX	eSCI_A – eSCI_B	eSCI transmit
ETPU_A[0:31]	eTPU	eTPU I/O channel
CAN_A_TX CAN_C_TX	FlexCan_A – FlexCAN_C	FlexCAN transmit
CAN_A_RX CAN_C_RX	FlexCAN_A – FlexCAN_C	FlexCAN receive
JCOMP	JTAG	Enables the JTAG TAP controller.
TCK	JTAG	Clock input for the on-chip test and debug logic.
TDI	JTAG	Serial test instruction and data input for the on-chip test and debug logic.
TDO	JTAG	Serial test data output for the on-chip test logic.
TMS	JTAG	Controls test mode operations for the on-chip test and debug logic.

[8] Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met.

[9] Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.

[10] Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.

[11] Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

[12] Total injection current for all analog input pins must not exceed 15 mA.

[13] Lifetime operation at these specification limits is not guaranteed.

[14] Solder profile per CDF-AEC-Q100.

[15] Moisture sensitivity per JEDEC test method A112.

4.3 Thermal characteristics

Table 8. Thermal characteristics for 144-pin LQFP

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[1]	Single layer board – 1s	43	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board – 2s2p	35	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Ambient (@200 ft/min)[2]	Single layer board –1s	34	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Ambient (@200 ft/min)[2]	Four layer board – 2s2p	29	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board[2]		22	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-Case (Top)[3]		8	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection[4]		2	°C/W

[1] Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

[2] Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

[3] Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

[4] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.6 Power Management Control (PMC) and Power On Reset (POR) electrical specifications

Table 13. PMC Operating conditions and external regulators supply voltage

ID	Name		C	Parameter	Min	Typ	Max	Unit
1	Jtemp	SR	—	Junction temperature	–40	27	150	°C
2	Vddreg	SR	—	PMC 5 V supply voltage VDDREG	4.75[1]	5	5.25	V
3	Vdd	SR	—	Core supply voltage 1.2 V VDD when external regulator is used without disabling the internal regulator (PMC unit turned on, LVI monitor active)[2]	1.26[3]	1.3	1.32	V
3a	—	SR	—	Core supply voltage 1.2 V VDD when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	1.14	1.2	1.32	V
4	Ivdd	SR	—	Voltage regulator core supply maximum DC output current[4]	400	—	—	mA
5	Vdd33	SR	—	Regulated 3.3 V supply voltage when external regulator is used without disabling the internal regulator (PMC unit turned-on, internal 3.3V regulator enabled, LVI monitor active)[5]	3.3	3.45	3.6	V
5a	—	SR	—	Regulated 3.3 V supply voltage when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	3	3.3	3.6	V
6	—	SR	—	Voltage regulator 3.3 V supply maximum required DC output current	80	—	—	mA

1 During start up operation the minimum required voltage to come out of reset state is 4.6 V.

2 An internal regulator controller can be used to regulate core supply.

3 The minimum supply required for the part to exit reset and enter in normal run mode is 1.28 V.

4 The onchip regulator can support a minimum of 400 ma although the worst case core current is 180 ma.

5 An internal regulator can be used to regulate 3.3 V supply.

Table 14. PMC electrical characteristics

ID	Name		C	Parameter	Min	Typ	Max	Unit	Notes
1	Vbg	CC	C	Nominal bandgap voltage reference	—	1.219	—	V	
1a	—	CC	P	Untrimmed bandgap reference voltage	Vbg–7%	Vbg	Vbg+6%	V	
1b	—	CC	P	Trimmed bandgap reference voltage (5 V, 27 °C)[1]	Vbg–10mV	Vbg	Vbg+10mV	V	
1c	—	CC	C	Bandgap reference temperature variation	—	100	—	ppm /°C	

4.6.1 Regulator example

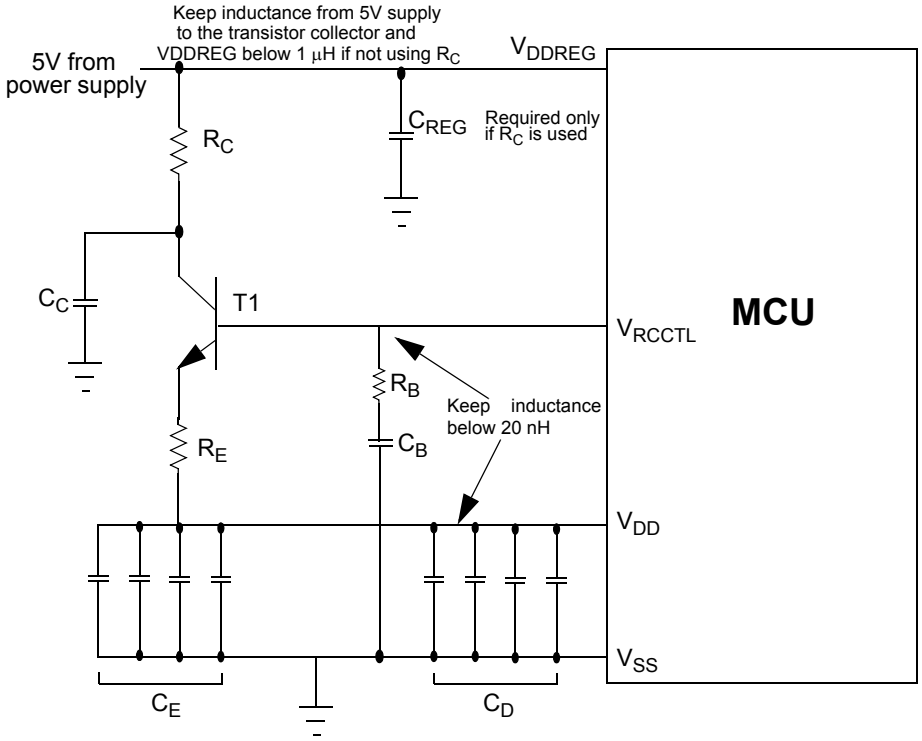


Figure 7. Core voltage regulator controller external components preferred configuration

There are three options for the bypassing and compensation networks for the 1.2V regulator controller. The component values in the following table are the same for all PMC network requirements.

Table 15. Required external PMC component values

Component	Symbol	Minimum	Typical	Maximum	Units	Comment
Pass Transistor	T1					NJD2873 or BCP68
VDDREG capacitor	C_{REG}		10		µF	X7R, -50%/+35%
Pass transistor Collector bypass capacitor	C_C			13.3	µF	X7R, -50%/+35%
Collector resistor[1]	R_C	1.1	—	5.6	Ω	

[1] The collector resistor may not be required. It depends on the allowable power dissipation of the pass transistor (T1).

Table 16, Table 17 and Table 18 show the required component values for the three different options.

4.8 DC electrical specifications

Table 22. DC electrical specifications[1]

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
V_{DD}	SR	—	Core supply voltage	—	1.14	—	1.32	V
V_{DDE}	SR	—	I/O supply voltage	—	1.62	—	3.6[3]	V
V_{DDEH}	SR	—	I/O supply voltage	—	3.0	—	5.25	V
V_{RC33}	SR	—	3.3 V external voltage[4]	—	3.0	—	3.6	V
V_{DDA}	SR	—	Analog supply voltage	—	4.75[5]	—	5.25	V
V_{INDC}	SR	—	Analog input voltage[6]	—	V_{SSA} – 0.3	—	V_{DDA}+0.3	V
$V_{SS} – V_{SSA}$	SR	—	V_{SS} differential voltage	—	–100	—	100	mV
V_{RL}	SR	—	Analog reference low voltage	—	V_{SSA}	—	V_{SSA}+0.1	V
$V_{RL} – V_{SSA}$	SR	—	V_{RL} differential voltage	—	–100	—	100	mV
V_{RH}	SR	—	Analog reference high voltage	—	V_{DDA} – 0.1	—	V_{DDA}	V
$V_{RH} – V_{RL}$	SR	—	V_{REF} differential voltage	—	4.75	—	5.25	V
V_{DDF}	SR	—	Flash operating voltage [7]	—	1.14	—	1.32	V
V_{FLASH}[8]	SR	—	Flash read voltage	—	4.75	—	5.25	V
V_{STBY}	SR	—	SRAM standby voltage	Unregulated mode	0.95	—	1.2	V
				Regulated mode	2.0	—	5.5	
V_{DDREG}	SR	—	Voltage regulator supply voltage[9]	—	4.75	—	5.25	V
V_{DDPLL}	SR	—	Clock synthesizer operating voltage	—	1.14	—	1.32	V
$V_{SSPLL} – V_{SS}$	SR	—	V_{SSPLL} to V_{SS} differential voltage	—	–100	—	100	mV
V_{IL_S}	CC	C	Slow/medium pad I/O input low voltage	Hysteresis enabled	V_{SS}–0.3	—	0.35*V_{DDEH}	V
		P		hysteresis disabled	V_{SS}–0.3	—	0.40*V_{DDEH}	
V_{IL_F}	CC	C	Fast pad I/O input low voltage	Hysteresis enabled	V_{SS}–0.3	—	0.35*V_{DDE}	V
		P		hysteresis disabled	V_{SS}–0.3	—	0.40*V_{DDE}	

Table 22. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
C_L	CC	D	Load capacitance (fast I/O)[27]	DSC(PCR[8:9]) = 0b00	—	—	10	pF
		D		DSC(PCR[8:9]) = 0b01	—	—	20	
		D		DSC(PCR[8:9]) = 0b10	—	—	30	
		D		DSC(PCR[8:9]) = 0b11	—	—	50	
C_{IN}	CC	D	Input capacitance (digital pins)	—	—	—	7	pF
C_{IN_A}	CC	D	Input capacitance (analog pins)	—	—	—	10	pF
C_{IN_M}	CC	D	Input capacitance (digital and analog pins[28])	—	—	—	12	pF
$R_{PUPD200K}$	CC	P	Weak Pull-Up/Down Resistance[29,30] 200 kΩ Option	—	130	—	280	kΩ
$R_{PUPDMATCH}$	CC	C	200KΩ Option		–2.5		2.5	%
$R_{PUPD100K}$	CC	P	Weak Pull-Up/Down Resistance[29,30] 100 kΩ Option	—	65	—	140	kΩ
$R_{PUPDMATCH}$	CC	C	100KΩ Option		–2.5		2.5	%
R_{PUPD5K}	CC	D	Weak Pull-Up/Down Resistance[29] 5 kΩ Option	5 V ± 5% supply	1.4	—	7.5	kΩ
T_A (T_L to T_H)	SR	—	Operating temperature range - ambient (packaged)	—	–40.0	—	125.0	°C
—	SR	—	Slew rate on power supply pins	—	—	—	50	V/ms

1 These specifications are design targets and subject to change per device characterization.

2 TBD: To Be Defined.

3 V_{DDE} must be lower than V_{RC33}, otherwise there is additional leakage on pins supplied by V_{DDE}.

4 These specifications apply when V_{RC33} is supplied externally, after disabling the internal regulator (V_{DDREG} = 0).

5 ADC is functional with 4 V ≤ V_{DDA} ≤ 4.75 V but with derated accuracy. This means the ADC will continue to function at full speed with no bad behavior, but the accuracy will be degraded.

6 Internal structures hold the input voltage less than V_{DDA} + 1.0 V on all pads powered by V_{DDA} supplies, if the maximum injection current specification is met (3 mA for all pins) and V_{DDA} is within the operating voltage specifications.

7 The V_{DDF} supply is connected to V_{DD} in the package substrate. This specification applies to calibration package devices only.

4 Ratio from 5.5 V pad spec to 5.25 V data sheet.
5 Not specified.
6 Low swing mode is not a strong function of V_{DDE}.

4.9.1 I/O pad VRC33 current specifications

The power consumption of the VRC33 supply is dependent on the usage of the pins on all I/O segments. The power consumption is the sum of all output pin V_{RC33} currents for all I/O segments. The output pin V_{RC33} current can be calculated from Table 24 based on the voltage, frequency, and load on all medium, slow, and multv_hv pins. The output pin VRC33 current can be calculated from Table 25 based on the voltage, frequency, and load on all fast pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 24 and Table 25.

Table 24. I/O pad V_{RC33} average I_{DDE} specifications[1]

Pad Type	Symbol		C	Period (ns)	Load[2] (pF)	Slew Rate Select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	100	50	11	0.8	235.7
		CC	D	200	50	01	0.04	87.4
		CC	D	800	50	00	0.06	47.4
		CC	D	800	200	00	0.009	47
Medium	$I_{DRV\_MSR\_HV}$	CC	D	40	50	11	2.75	258
		CC	D	100	50	01	0.11	76.5
		CC	D	500	50	00	0.02	56.2
		CC	D	500	200	00	0.01	56.2
MultiV[3] (High Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	40	50	11	2.75	258
		CC	D	100	50	01	0.11	76.5
		CC	D	500	50	00	0.02	56.2
		CC	D	500	200	00	0.01	56.2
MultiV[4] (Low Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	40	30	11	2.75	258
		CC	D	100	30	11	0.11	76.5
		CC	D	500	30	11	0.02	56.2
		CC	D	500	30	11	0.01	56.2

1 These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.
2 All loads are lumped.
3 Average current is for pad configured as output only.
4 In low swing mode, multi-voltage pads (pad_multv_hv) must operate in highest slew rate setting.

Table 27. PLLMRFM electrical specifications[1]

(V_{DDPLL} =1.14 V to 1.32 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					min	max	
V_{ILEXT}	CC	T	EXTAL input low voltage	Crystal Mode[14], 0.65≤Vxtal≤1.25V[15]	—	Vxtal – 0.4	V
		T		External Reference[14, 16]	0	V_{RC33}/2 – 0.4	
—	CC	T	XTAL load capacitance[12]	4 MHz	5	30	pF
				8 MHz	5	26	
				12 MHz	5	23	
				16 MHz	5	19	
				20 MHz	5	16	
t_{lpll}	CC	P	PLL lock time [12, 17]	—	—	200	µs
t_{dc}	CC	T	Duty cycle of reference	—	40	60	%
f_{LCK}	CC	T	Frequency LOCK range	—	–6	6	% f_{sys}
f_{UL}	CC	T	Frequency un-LOCK range	—	–18	18	% f_{sys}
f_{CS} f_{DS}	CC	D	Modulation Depth	Center spread	±0.25	±4.0	%f_{sys}
		D		Down Spread	–0.5	–8.0	
f_{MOD}	CC	D	Modulation frequency[18]	—	—	100	kHz

1 All values given are initial design targets and subject to change.

2 Considering operation with PLL not bypassed.

3 f_{VCO} is calculated as follows:

— In Legacy Mode f_{VCO} = ($f_{crystal}$ / (PREDIV + 1)) * (4 * (MFD + 4))

— In Enhanced Mode fvco = ($f_{crystal}$ / (EPREDIV + 1)) * (EMFD + 4)

4 All internal registers retain data at 0 Hz.

5 “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.

6 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.

7 f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.

8 This value is determined by the crystal manufacturer and board design.

9 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.

10 Proper PC board layout procedures must be followed to achieve specifications.

11 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).

12 This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits. For a 20 MHz crystal the maximum load should be 17 pF.

13 Proper PC board layout procedures must be followed to achieve specifications.

14 This parameter is guaranteed by design rather than 100% tested.

Table 32. Flash module life

Symbol		Parameter	Conditions	Value		Unit
				Min	Typ	
P/E	C	Number of program/erase cycles per block for 16 Kbyte blocks over the operating temperature range (T_J)	—	100,000	—	cycles
P/E	C	Number of program/erase cycles per block for 32 and 64 Kbyte blocks over operating temperature range (T_J)	—	10,000	100,000	cycles
P/E	C	Number of program/erase cycles per block for 128 Kbyte blocks over the operating temperature range (T_J)	—	1,000	100,000	cycles
Retention	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0 – 1,000 P/E cycles	20	—	years
			Blocks with 10,000 P/E cycles	10	—	years
			Blocks with 100,000 P/E cycles	5	—	years

[1] Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

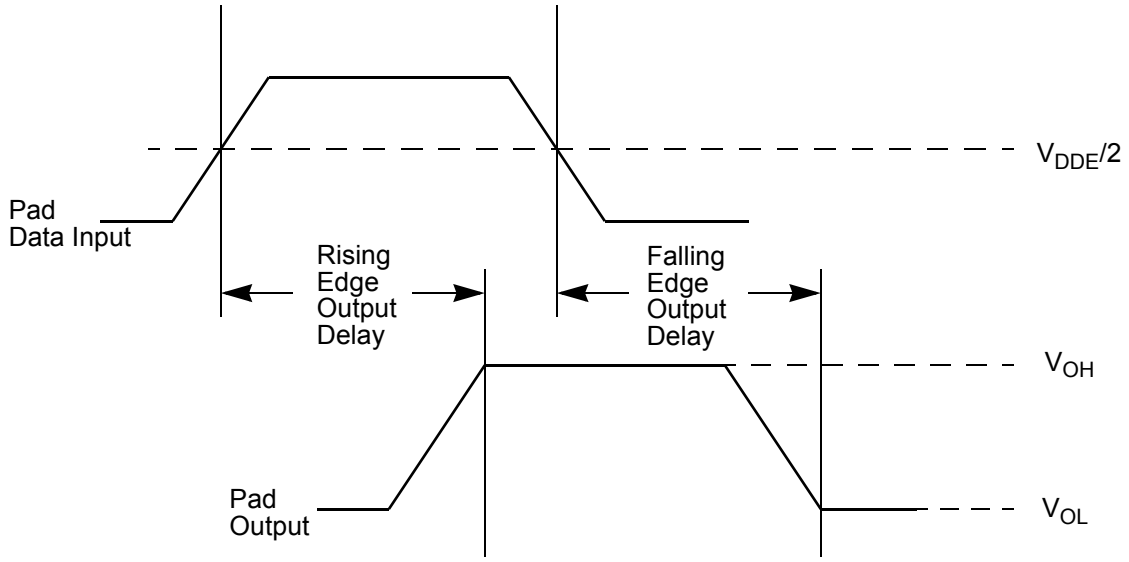


Figure 8. Pad output delay

4.16 AC timing

4.16.1 IEEE 1149.1 interface timing

Table 36. JTAG pin AC electrical characteristics[1]

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
1	t_{JCYC}	CC	D	TCK Cycle Time	100	—	ns
2	t_{JDC}	CC	D	TCK Clock Pulse Width	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK Rise and Fall Times (40% – 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI Data Hold Time	25	—	ns
6	t_{TDOV}	CC	D	TCK Low to TDO Data Valid	—	23	ns
7	t_{TDOI}	CC	D	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	CC	D	TCK Low to TDO High Impedance	—	20	ns
9	t_{JCMPPW}	CC	D	JCOMP Assertion Time	100	—	ns
10	t_{JCMPS}	CC	D	JCOMP Setup Time to TCK Low	40	—	ns
11	t_{BSDV}	CC	D	TCK Falling Edge to Output Valid	—	50	ns

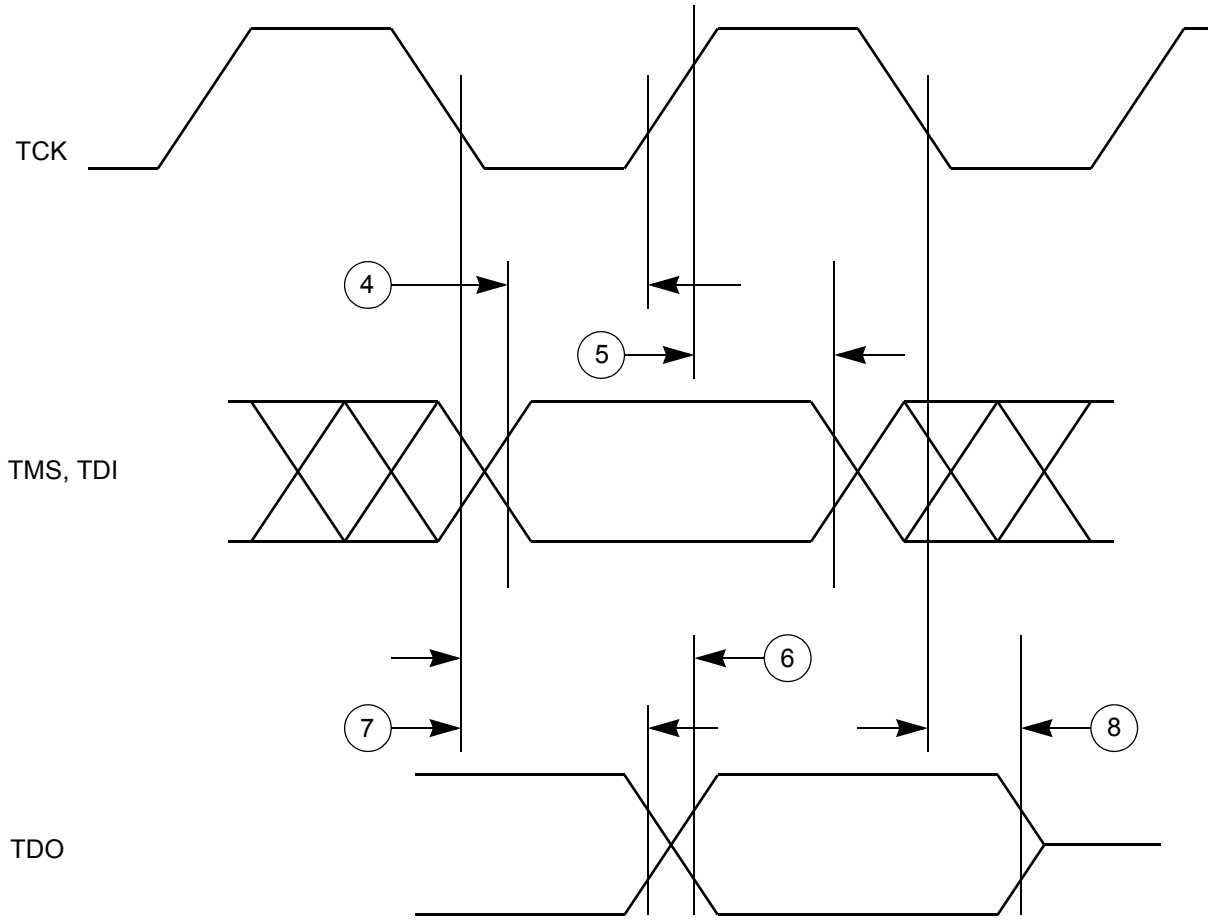


Figure 10. JTAG test access port timing

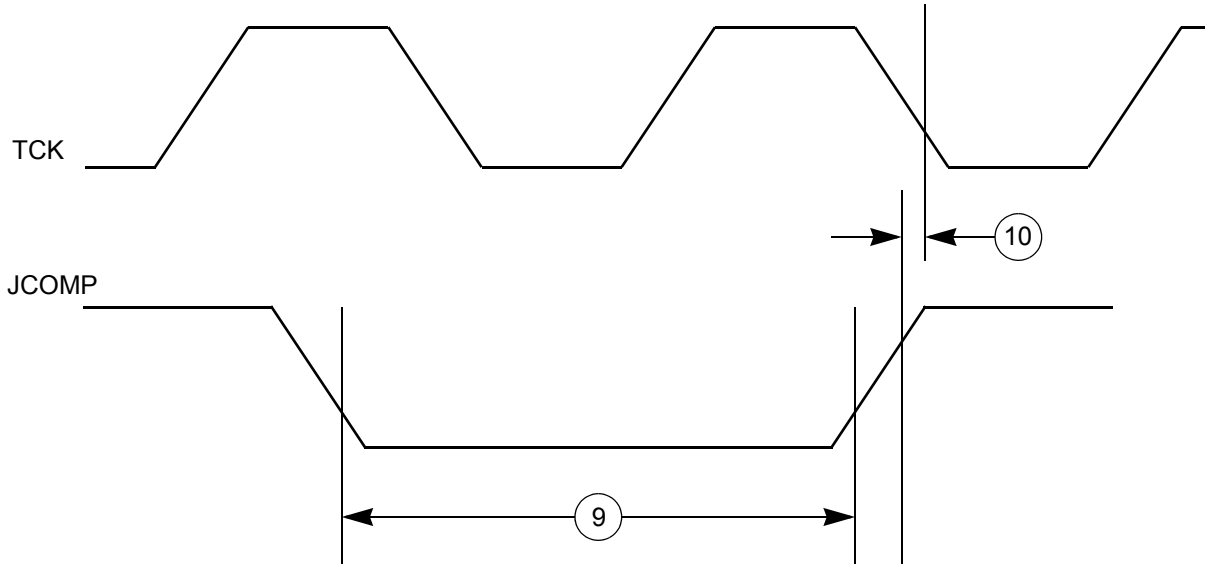
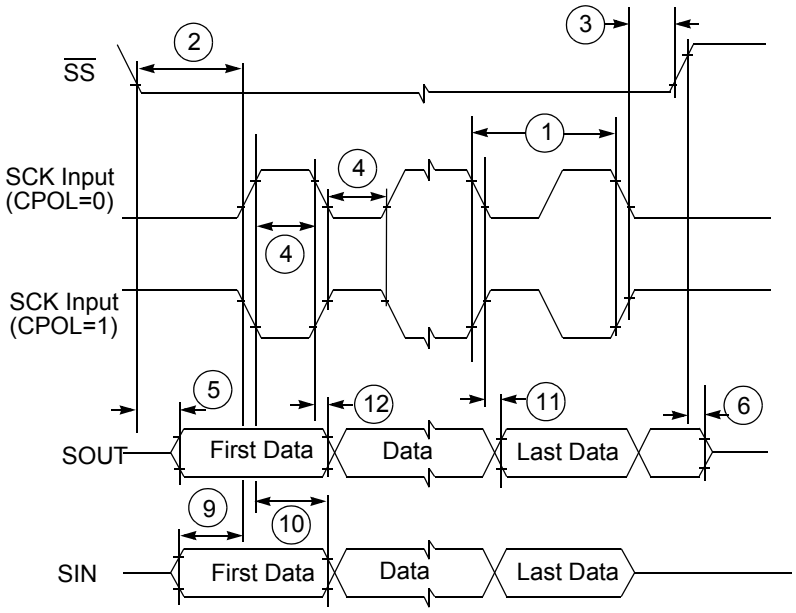
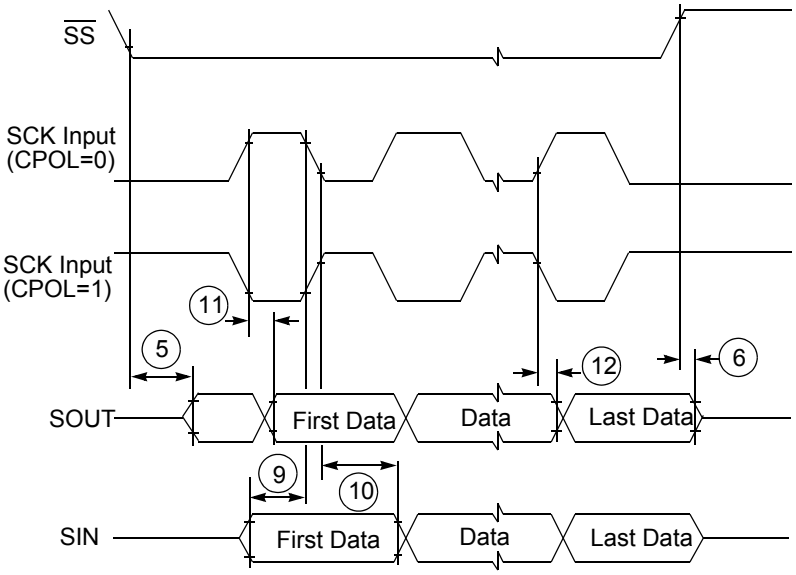


Figure 11. JTAG JCOMP timing



These numbers reference Table 40.

Figure 22. DSPI classic SPI timing – slave, CPHA = 0



These numbers reference Table 40.

Figure 23. DSPI classic SPI timing – slave, CPHA = 1

5.1.3 208 MAPBGA

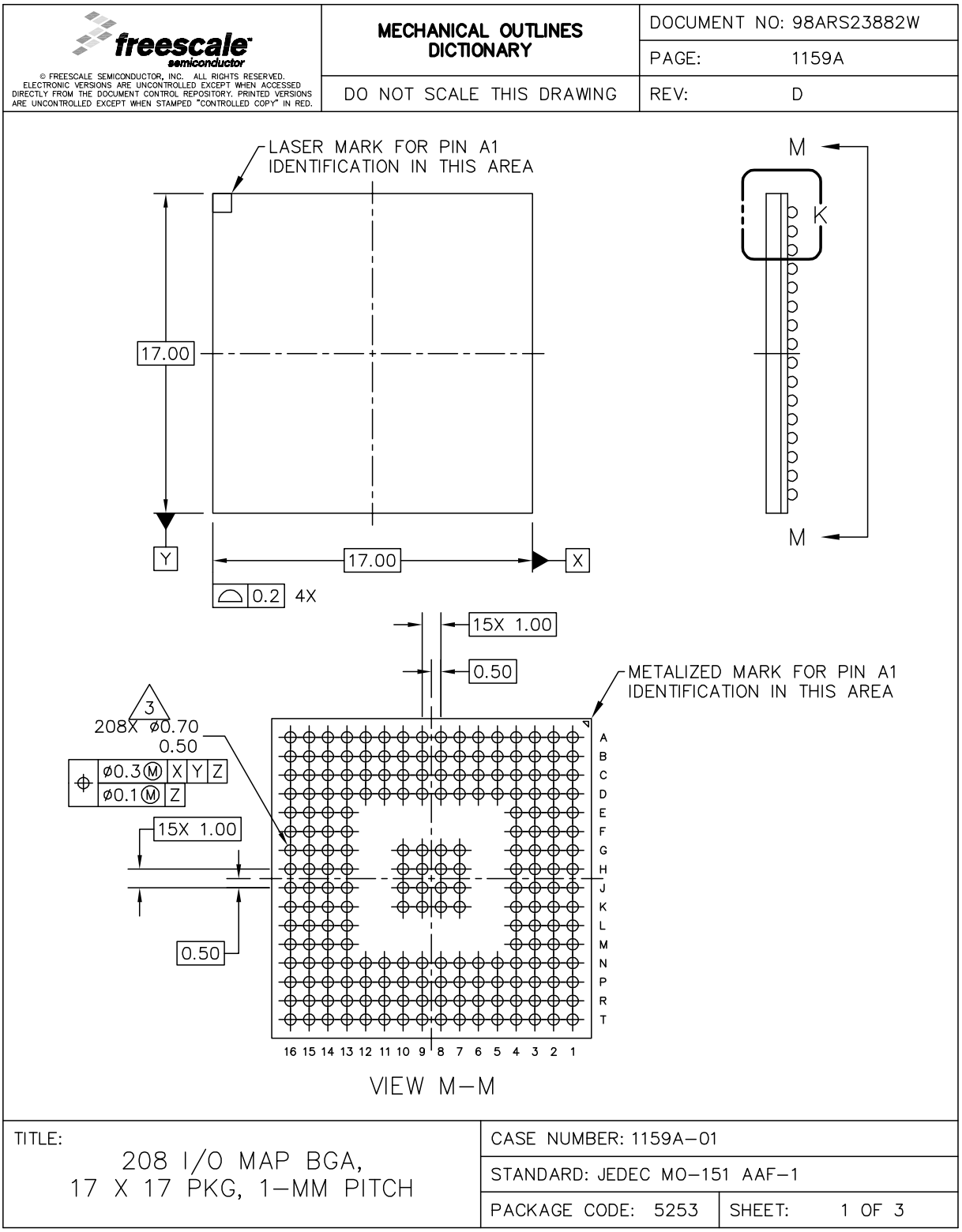


Figure 36. 208 MAPBGA package mechanical drawing (part 1)

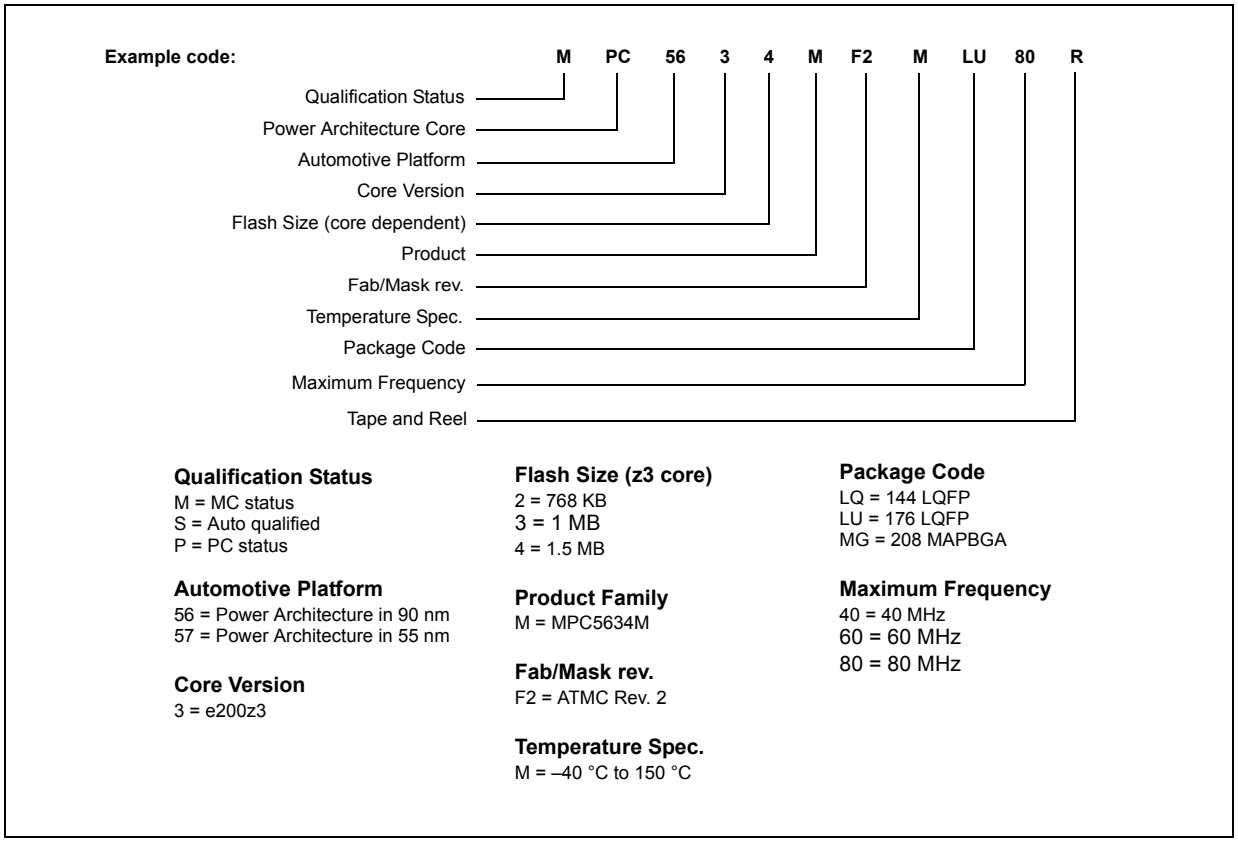


Figure 38. Commercial product code structure