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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z3
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	94K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5634mf1mlq60

- Allows selection of interrupt requests between external pins and DSPI

- Error correction status module (ECSM)
  - Configurable error-correcting codes (ECC) reporting
  - Single-bit error correction reporting
- On-chip flash memory
  - Up to 1.5 MB flash memory, accessed via a 64-bit wide bus interface
  - 16 KB shadow block
  - Fetch Accelerator
    - Provide single cycle flash access at 80 MHz
    - Quadruple 128-bit wide prefetch/burst buffers
    - Prefetch buffers can be configured to prefetch code or data or both
  - Censorship protection scheme to prevent flash content visibility
  - Flash divided into two independent arrays, allowing reading from one array while erasing/programming the other array (used for EEPROM emulation)
  - Memory block:
    - For MPC5634M: 18 blocks (4 × 16 KB, 2 × 32 KB, 2 × 64 KB, 10 × 128 KB)
    - For MPC5633M: 14 blocks (4 × 16 KB, 2 × 32 KB, 2 × 64 KB, 6 × 128 KB)
    - For MPC5632M: 12 blocks (4 × 16 KB, 2 × 32 KB, 2 × 64 KB, 4 × 128 KB)
  - Hardware programming state machine
- On-chip static RAM
  - For MPC5634M: 94 KB general purpose RAM of which 32 KB are on standby power supply
  - For MPC5633M: 64 KB general purpose RAM of which 32 KB are on standby power supply
  - For MPC5632M: 48 KB general purpose RAM of which 24 KB are on standby power supply
- Boot assist module (BAM)
  - Enables and manages the transition of MCU from reset to user code execution in the following configurations:
    - Execution from internal flash memory
    - Execution from external memory on the calibration bus
    - Download and execution of code via FlexCAN or eSCI
- Periodic interrupt timer (PIT)
  - 32-bit wide down counter with automatic reload
  - Four channels clocked by system clock
  - One channel clocked by crystal clock
  - Each channel can produce periodic software interrupt
  - Each channel can produce periodic triggers for eQADC queue triggering
  - One channel out of the five can be used as wake-up timer to wake device from low power stop mode
- System timer module (STM)
  - 32-bit up counter with 8-bit prescaler
  - Clocked from system clock
  - Four-channel timer compare hardware
  - Each channel can generate a unique interrupt request
  - Designed to address AUTOSAR task monitor function
- Software watchdog timer (SWT)
  - 32-bit timer
  - Clock by system clock or crystal clock
  - Can generate either system reset or non-maskable interrupt followed by system reset

- Sets up the MMU to allow user boot code to execute as either Power Architecture code (default) or as Freescale VLE code
- Detection of user boot code
- Automatic switch to serial boot mode if internal flash is blank or invalid
- Supports user programmable 64-bit password protection for serial boot mode
- Supports serial bootloading via FlexCAN bus and eSCI using Freescale protocol
- Supports serial bootloading via FlexCAN bus and eSCI with auto baud rate sensing
- Supports serial bootloading of either Power Architecture code (default) or Freescale VLE code
- Supports booting from calibration bus interface
- Supports censorship protection for internal flash memory
- Provides an option to enable the core watchdog timer
- Provides an option to disable the software watchdog timer

2.2.12 eMIOS

The eMIOS (Enhanced Modular Input Output System) module provides the functionality to generate or measure time events. The channels on this module provide a range of operating modes including the capability to perform dual input capture or dual output compare as well as PWM output.

The eMIOS provides the following features:

- 16 channels (24-bit timer resolution)
- For compatibility with other family members selected channels and timebases are implemented:
  - Channels 0 to 6, 8 to 15, and 23
  - Timebases A, B and C
- Channels 1, 3, 5 and 6 support modes:
  - General Purpose Input/Output (GPIO)
  - Single Action Input Capture (SAIC)
  - Single Action Output Compare (SAOC)
- Channels 2, 4, 11 and 13 support all the modes above plus:
  - Output Pulse Width Modulation Buffered (OPWMB)
- Channels 0, 8, 9, 10, 12, 14, 15, 23 support all the modes above plus:
  - Input Period Measurement (IPM)
  - Input Pulse Width Measurement (IPWM)
  - Double Action Output Compare (set flag on both matches) (DAOC)
  - Modulus Counter Buffered (MCB)
  - Output Pulse Width and Frequency Modulation Buffered (OPWFMB)
- Three 24-bit wide counter buses
  - Counter bus A can be driven by channel 23 or by the eTPU2 and all channels can use it as a reference
  - Counter bus B is driven by channel 0 and channels 0 to 6 can use it as a reference
  - Counter bus C is driven by channel 8 and channels 8 to 15 can use it as a reference
- Shared time bases with the eTPU2 through the counter buses
- Synchronization among internal and external time bases

2.2.13 eTPU2

The eTPU2 is an enhanced co-processor designed for timing control. Operating in parallel with the host CPU, eTPU2 processes instructions and real-time input events, performs output waveform generation, and accesses shared data without host

  - 32-bit microengine registers and 24-bit wide ALU, with 1 microcycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands, single-bit manipulation, shift operations, sign extension and conditional execution
  - Additional 24-bit Multiply/MAC/Divide unit which supports all signed/unsigned Multiply/MAC combinations, and unsigned 24-bit divide. The MAC/Divide unit works in parallel with the regular microcode commands
- Resource sharing features support channel use of common channel registers, memory and microengine time:
  - Hardware scheduler works as a “task management” unit, dispatching event service routines by predefined, host-configured priority
  - Automatic channel context switch when a “task switch” occurs, i.e., one function thread ends and another begins to service a request from other channel: channel-specific registers, flags and parameter base address are automatically loaded for the next serviced channel
  - SPRAM shared between host CPU and eTPU2, supporting communication either between channels and host or inter-channel
  - Dual-parameter coherency hardware support allows atomic access to two parameters by host
- Test and development support features:
  - Nexus Class 1 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions
  - Software breakpoints
  - SCM continuous signature-check built-in self test (MISC — multiple input signature calculator), runs concurrently with eTPU2 normal operation
- System enhancements
  - Software watchdog with programmable timeout
  - Real-time performance information
- Channel enhancements
  - Channels 1 and 2 can optionally drive angle clock hardware
- Programming enhancements
  - Engine relative addressing mode

2.2.14 eQADC

The enhanced queued analog to digital converter (eQADC) block provides accurate and fast conversions for a wide range of applications. The eQADC provides a parallel interface to two on-chip analog to digital converters (ADC), and a single master to single slave serial interface to an off-chip external device. Both on-chip ADCs have access to all the analog channels.

The eQADC prioritizes and transfers commands from six command conversion command ‘queues’ to the on-chip ADCs or to the external device. The block can also receive data from the on-chip ADCs or from an off-chip external device into the six result queues, in parallel, independently of the command queues. The six command queues are prioritized with Queue_0 having the highest priority and Queue_5 the lowest. Queue_0 also has the added ability to bypass all buffering and queuing and abort a currently running conversion on either ADC and start a Queue_0 conversion. This means that Queue_0 will always have a deterministic time from trigger to start of conversion, irrespective of what tasks the ADCs were performing when the trigger occurred. The eQADC supports software and external hardware triggers from other blocks to initiate transfers of commands from the queues to the on-chip ADCs or to the external device. It also monitors the fullness of command queues and result queues, and accordingly generates DMA or interrupt requests to control data movement between the queues and the system memory, which is external to the eQADC.

The ADCs also support features designed to allow the direct connection of high impedance acoustic sensors that might be used in a system for detecting engine knock. These features include differential inputs; integrated variable gain amplifiers for increasing the dynamic range; programmable pull-up and pull-down resistors for biasing and sensor diagnostics.

The eQADC also integrates a programmable decimation filter capable of taking in ADC conversion results at a high rate, passing them through a hardware low pass filter, then down-sampling the output of the filter and feeding the lower sample rate

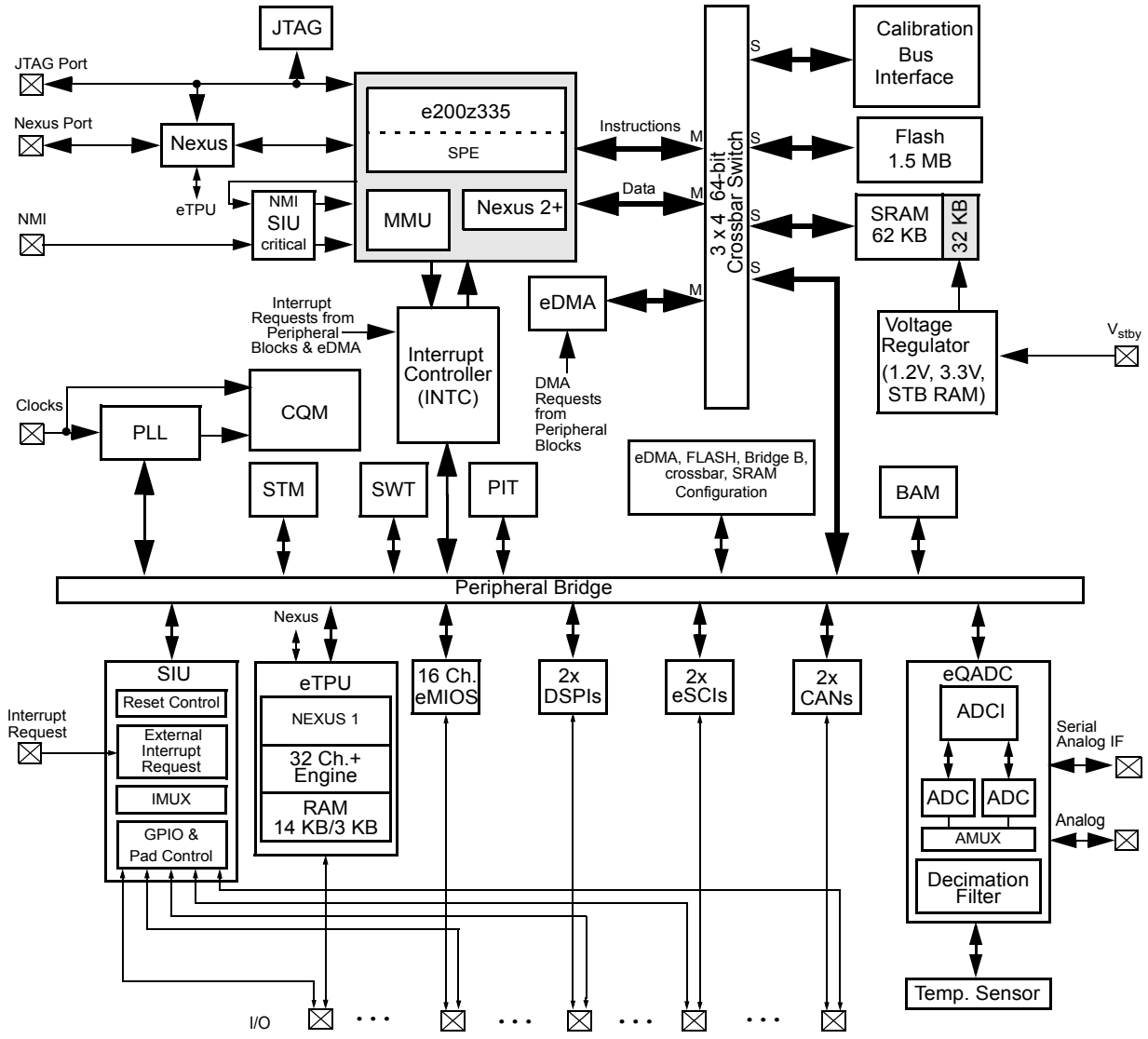


Figure 1. MPC5634M series block diagram

2.3.2 Block summary

Table 1 summarizes the functions of the blocks present on the MPC5634M series microcontrollers.

Table 1. MPC5634M series block summary

Block	Function
e200z3 core	Executes programs and interrupt handlers.
Flash memory	Provides storage for program code, constants, and variables
RAM (random-access memory)	Provides storage for program code, constants, and variables
Calibration bus	Transfers data across the crossbar switch to/from peripherals attached to the VertiCal connector

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPBGA
AN[38]-AN[8]-ANW	Single Ended Analog Input Multiplexed Analog Input	—	—	I	VDDA	I / –	AN[38] / –		9	9	B3
AN[39]-AN[10]-ANY	Single Ended Analog Input Multiplexed Analog Input	—	—	I	VDDA	I / –	AN[39] / –		8	8	D2
VRH	Voltage Reference High	—	—	I	VDDA	– / –	VRH		134	163	A8
VRL	Voltage Reference Low	—	—	I	VSSA0	– / –	VRL		133	162	A9
REFBYPC	Bypass Capacitor Input	—	—	I	VRL	– / –	REFBYPC		135	164	B7
eTPU2											
eTPU_A[0] eTPU_A[12] eTPU_A[19] GPIO[114]	eTPU_A Ch. eTPU_A Ch. eTPU_A Ch. GPIO	PCR[114]	011 010 100 000	I/O O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		52	61	L4, N3
eTPU_A[1] eTPU_A[13] GPIO[115]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[115]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		51	60	M3
eTPU_A[2] eTPU_A[14] GPIO[116]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[116]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		50	59	P2
eTPU_A[3] eTPU_A[15] GPIO[117]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[117]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		49	58	P1
eTPU_A[4] eTPU_A[16] GPIO[118]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[118]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		47	56	N2
eTPU_A[5] eTPU_A[17] DSPI_B_SCK_LVDS- GPIO[119]	eTPU_A Ch. eTPU_A Ch. DSPI_B CLOCK LVDS- GPIO	PCR[119]	001 010 100 000	I/O O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		45	54	M4
eTPU_A[6] eTPU_A[18] DSPI_B_SCK_LVDS+ GPIO[120]	eTPU_A Ch. eTPU_A Ch. DSPI_B Clock LVDS+ GPIO	PCR[120]	001 010 100 000	I/O O O I/O	VDDEH1b Medium	– / WKPCFG	– / WKPCFG		44	53	L3

[7] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.3.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)
$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)
P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} * P_D) \quad \textit{Eqn. 2}$$

where:

T_B = board temperature for the package perimeter (^oC)
$R_{\theta JB}$ = junction-to-board thermal resistance ($^oC/W$) per JESD51-8S
P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

Table 14. PMC electrical characteristics (continued)

ID	Name		C	Parameter	Min	Typ	Max	Unit	Notes
1d	—	CC	C	Bandgap reference supply voltage variation	—	3000	—	ppm /V	
2	Vdd	CC	C	Nominal VDD core supply internal regulator target DC output voltage[2]	—	1.28	—	V	
2a	—	CC	P	Nominal VDD core supply internal regulator target DC output voltage variation at power-on reset	Vdd – 6%	Vdd	Vdd + 10%	V	
2b	—	CC	P	Nominal VDD core supply internal regulator target DC output voltage variation after power-on reset	Vdd – 10[3]	Vdd	Vdd + 3%	V	
2c	—	CC	C	Trimming step Vdd	—	20	—	mV	
2d	Ivrcctl	CC	C	Voltage regulator controller for core supply maximum DC output current	20	—	—	mA	
3	Lvi1p2	CC	C	Nominal LVI for rising core supply[4,5]	—	1.160	—	V	
3a	—	CC	C	Variation of LVI for rising core supply at power-on reset[5,6]	1.120	1.200	1.280	V	
3b	—	CC	C	Variation of LVI for rising core supply after power-on reset[5,6]	Lvi1p2–3%	Lvi1p2	Lvi1p2+3%	V	
3c	—	CC	C	Trimming step LVI core supply[5]	—	20	—	mV	
3d	Lvi1p2_h	CC	C	LVI core supply hysteresis[5]	—	40	—	mV	
4	Por1.2V_r	CC	C	POR 1.2 V rising	—	0.709	—	V	
4a	—	CC	C	POR 1.2 V rising variation	Por1.2V_r– 35%	Por1.2V_r	Por1.2V_r+ 35%	V	
4b	Por1.2V_f	CC	C	POR 1.2 V falling	—	0.638	—	V	
4c	—	CC	C	POR 1.2 V falling variation	Por1.2V_f– 35%	Por1.2V_f	Por1.2V_f+ 35%	V	
5	Vdd33	CC	C	Nominal 3.3 V supply internal regulator DC output voltage	—	3.39	—	V	
5a	—	CC	P	Nominal 3.3 V supply internal regulator DC output voltage variation at power-on reset[6]	Vdd33 – 8.5%	Vdd33	Vdd3 + 7%	V	

Table 14. PMC electrical characteristics (continued)

ID	Name		C	Parameter	Min	Typ	Max	Unit	Notes
5b	—	CC	P	Nominal 3.3 V supply internal regulator DC output voltage variation after power-on reset	Vdd33 – 7.5%	Vdd33	Vdd33 + 7%	V	With internal load up to Idd3p3
5c	—	CC	D	Voltage regulator 3.3 V output impedance at maximum DC load	—	—	2	Ω	
5d	Idd3p3	CC	P	Voltage regulator 3.3 V maximum DC output current	80	—	—	mA	
5e	Vdd33 ILim[6]	CC	C	Voltage regulator 3.3 V DC current limit	—	130	—	mA	
6	Lvi3p3	CC	C	Nominal LVI for rising 3.3 V supply[5]	—	3.090	—	V	The Lvi3p3 specs are also valid for the Vddeh LVI
6a	—	CC	C	Variation of LVI for rising 3.3 V supply at power-on reset[5]	Lvi3p3–6%	Lvi3p3	Lvi3p3+6%	V	See note [7]
6b	—	CC	C	Variation of LVI for rising 3.3 V supply after power-on reset[5]	Lvi3p3–3%	Lvi3p3	Lvi3p3+3%	V	See note 7
6c	—	CC	C	Trimming step LVI 3.3 V[5]	—	20	—	mV	
6d	Lvi3p3_h	CC	C	LVI 3.3 V hysteresis[5]	—	60	—	mV	
7	Por3.3V_r	CC	C	Nominal POR for rising 3.3 V supply	—	2.07	—	V	The 3.3V POR specs are also valid for the Vddeh POR
7a	—	CC	C	Variation of POR for rising 3.3 V supply	Por3.3V_r–35%	Por3.3V_r	Por3.3V_r+35%	V	
7b	Por3.3V_f	CC	C	Nominal POR for falling 3.3 V supply	—	1.95	—	V	
7c	—	CC	C	Variation of POR for falling 3.3 V supply	Por3.3V_f–35%	Por3.3V_f	Por3.3V_f+35%	V	
8	Lvi5p0	CC	C	Nominal LVI for rising 5 V VDDREG supply[5]	—	4.290	—	V	
8a	—	CC	C	Variation of LVI for rising 5 V VDDREG supply at power-on reset[5]	Lvi5p0–6%	Lvi5p0	Lvi5p0+6%	V	
8b	—	CC	C	Variation of LVI for rising 5 V VDDREG supply power-on reset[5]	Lvi5p0–3%	Lvi5p0	Lvi5p0+3%	V	
8c	—	CC	C	Trimming step LVI 5 V[5]	—	20	—	mV	

4.6.1 Regulator example

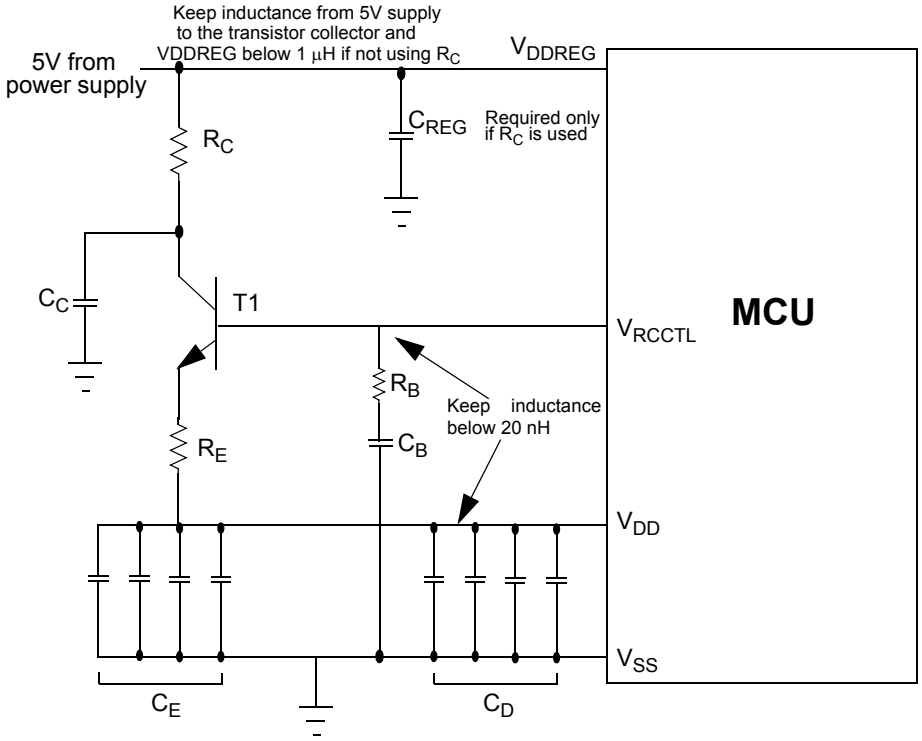


Figure 7. Core voltage regulator controller external components preferred configuration

There are three options for the bypassing and compensation networks for the 1.2V regulator controller. The component values in the following table are the same for all PMC network requirements.

Table 15. Required external PMC component values

Component	Symbol	Minimum	Typical	Maximum	Units	Comment
Pass Transistor	T1					NJD2873 or BCP68
VDDREG capacitor	C_{REG}		10		µF	X7R, -50%/+35%
Pass transistor Collector bypass capacitor	C_C			13.3	µF	X7R, -50%/+35%
Collector resistor[1]	R_C	1.1	—	5.6	Ω	

[1] The collector resistor may not be required. It depends on the allowable power dissipation of the pass transistor (T1).

Table 16, Table 17 and Table 18 show the required component values for the three different options.

Table 22. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
V_{OH_LS}	CC	P	Multi-voltage pad I/O output high voltage in low-swing mode[10,11,12,13,17]	I_{OH_LS} = 0.5 mA Min V_{DDEH} = 4.75 V	2.1	—	3.7	V
V_{OH_HS}	CC	P	Multi-voltage pad I/O output high voltage in high-swing mode[17]	—	0.8 V_{DDEH}	—	—	V
V_{HYS_S}	CC	C	Slow/medium/multi-voltage I/O input hysteresis	—	0.1 * V_{DDEH}	—	—	V
V_{HYS_F}	CC	C	Fast I/O input hysteresis	—	0.1 * V_{DDE}	—	—	V
V_{HYS_LS}	CC	C	Low-Swing-Mode Multi-Voltage I/O Input Hysteresis	hysteresis enabled	0.25	—	—	V
I_{DD}+I_{DDPLL}[19]	CC	P	Operating current 1.2 V supplies	V_{DD} = 1.32 V, 80 MHz	—	—	195	mA
	CC	P		V_{DD} = 1.32 V, 60 MHz	—	—	135	
	CC	P		V_{DD} = 1.32 V, 40 MHz	—	—	98	
I_{DDSTBY}	CC	T	Operating current 1 V supplies	T_J = 25 °C	—	—	80	µA
	CC	T		T_J = 55 °C	—	—	100	µA
$I_{DDSTBY150}$	CC	P	Operating current	T_J=150 °C	—	—	700	µA
I_{DDSLOW} I_{DDSTOP}	CC	P	V_{DD} low-power mode operating current @ 1.32 V	Slow mode[20]	—	—	50	mA
		C		Stop mode[21]	—	—	50	
I_{DD33}	CC	T	Operating current 3.3 V supplies @ 80 MHz	V_{RC33}[4,22]	—	—	70	mA
I_{DDA} I_{REF} I_{DDREG}	CC	P	Operating current 5.0 V supplies @ 80 MHz	V_{DDA}	—	—	30	mA
		P		Analog reference supply current	—	—	1.0	
		C		V_{DDREG}	—	—	70	

[15] Vxtal range is preliminary and subject to change pending characterization data.

[16] V_{IHEXT} cannot exceed V_{RC33} in external reference mode.

[17] This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

[18] Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50kHz.

4.11 Temperature sensor electrical characteristics

Table 28. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					min	typical	max	
—	CC	C	Temperature monitoring range		–40	—	150	°C
—	CC	C	Sensitivity		—	6.3	—	mV/°C
—	CC	P	Accuracy	T_J = –40 to 150 °C	–10	—	10	°C

4.12 eQADC electrical characteristics

NOTE

ADC performance is affected by several environmental elements, such as quality of the input signal source, presence of noise sources and quality of the PCB layout.

The DC or Static parameters (DNL, INL, OFFSET, GAIN, and TUE) are measured using methods that provide a very accurate evaluation using averaging.

The AC or Dynamic parameters (SNR, THD, SFDR, SINAD) are determined using a full scale peak-peak sinewave of 1kHz frequency at the input of the ADC.

Table 29. eQADC conversion specifications (operating)

Symbol		C	Parameter	Value		Unit
				min	max	
f_{ADCLK}	SR	—	ADC clock (ADCLK) frequency	2	16	MHz
CC	CC	D	Conversion cycles	2 + 13	128 + 14	ADCLK cycles
T_{SR}	CC	C	Stop mode recovery time[1]	—	10	µs
—	CC	D	Resolution[2]	1.25	—	mV
OFFNC	CC	C	Offset error without calibration	0	160	Counts
OFFWC	CC	C	Offset error with calibration	–4	4	Counts
GAINNC	CC	C	Full scale gain error without calibration	–160	0	Counts
GAINWC	CC	C	Full scale gain error with calibration	–4	4	Counts
I_{INJ}	CC	T	Disruptive input injection current [3, 4, 5, 6]	–3	3	mA
E_{INJ}	CC	T	Incremental error due to injection current[6,7,8]	–4	4	Counts

3 This parameter is supplied for reference and is not guaranteed by design and not tested.
4 Delay and rise/fall are measured to 20% or 80% of the respective signal.
5 This parameter is guaranteed by characterization before qualification rather than 100% tested.
6 In high swing mode, high/low swing pad Vol and Voh values are the same as those of the slew controlled output pads
7 Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
8 Output delay is shown in Figure 8. Add a maximum of one system clock to the output delay for delay with respect to system clock.
9 Can be used on the tester.
10 This drive select value is not supported. If selected, it will be approximately equal to 11.
11 Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
12 Selectable high/low swing IO pad with selectable slew in high swing mode only.
13 Fast pads are 3.3 V pads.
14 Stand alone input buffer. Also has weak pull-up/pull-down.

Table 34. Pad AC specifications (3.3 V)[1]

Pad Type		C	Output Delay (ns)[2,3] Low-to-High / High-to-Low		Rise/Fall Edge (ns)[3,4]		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium[5,6,7]	CC	D	5.8/4.4	18/17	2.7/2.1	10/10	50	11[8]
	CC	D	16/13	46/49	11.2/8.6	34/34	200	
	N/A							10[9]
	CC	D	14/16	37/45	6.5/6.7	19/19	50	01
	CC	D	27/27	69/82	15/13	43/43	200	
	CC	D	83/86	200/210	38/38	86/86	50	00
	CC	D	113/109	270/285	53/46	120/120	200	
Slow[7,10]	CC	D	9.2/6.9	27/28	5.5/4.1	20/20	50	11
	CC	D	30/23	81/87	21/16	63/63	200	
	N/A							10[9]
	CC	D	31/31	80/90	15.4/15.4	42/42	50	01
	CC	D	58/52	144/155	32/26	82/85	200	
	CC	D	162/168	415/415	80/82	190/190	50	00
	CC	D	216/205	533/540	106/95	250/250	200	
MultiV[7,11] (High Swing Mode)	CC	D		3.7/3.1		10/10	30	11[8]
	CC	D		46/49		37/37	200	
	N/A							10[9]
	CC	D		32		15/15	50	01
	CC	D		72		46/46	200	
	CC	D		210		100/100	50	00
	CC	D		295		134/134	200	

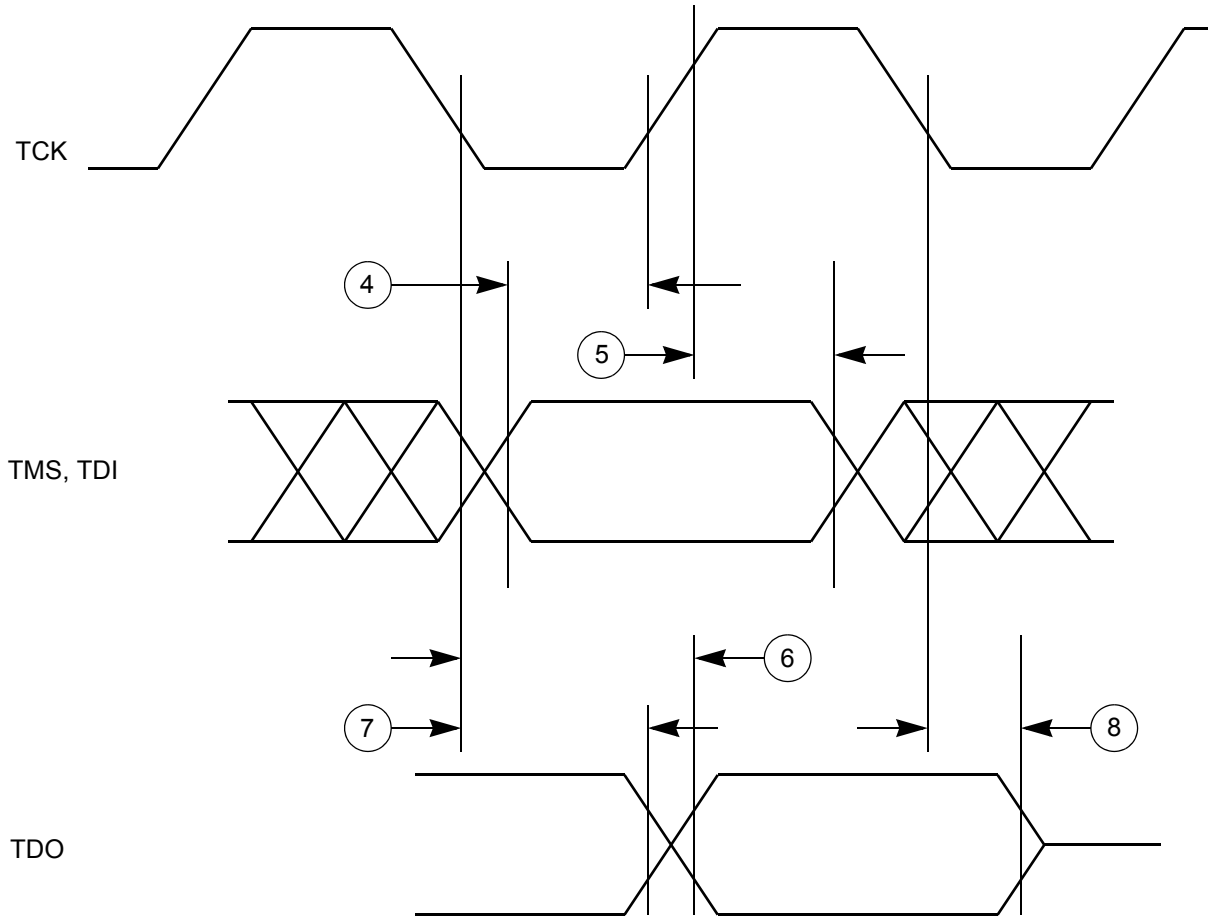


Figure 10. JTAG test access port timing

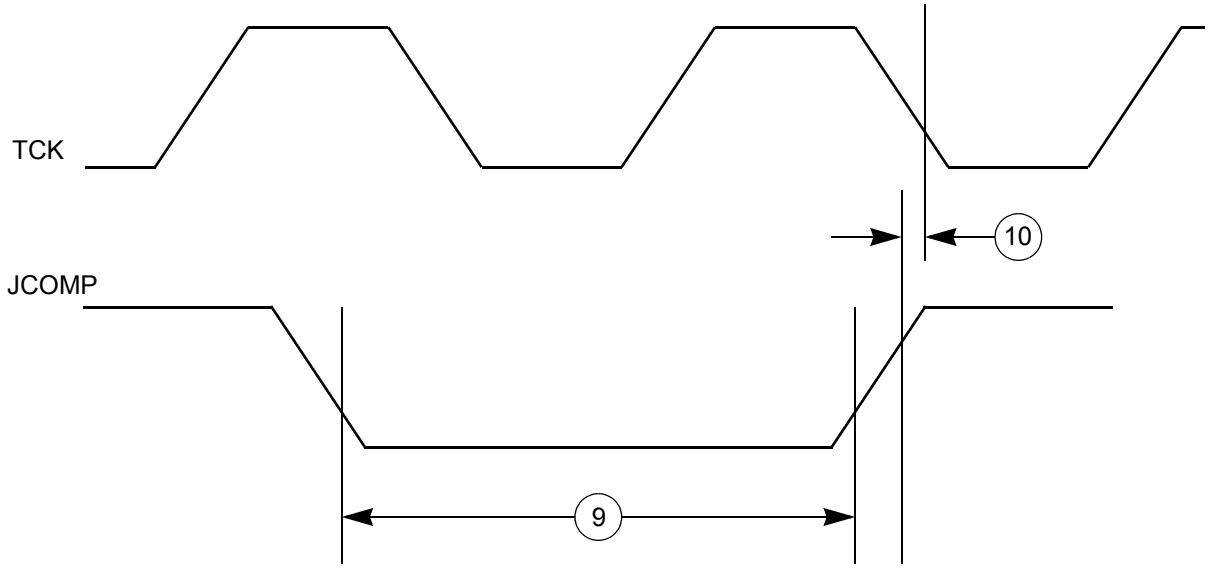


Figure 11. JTAG JCOMP timing

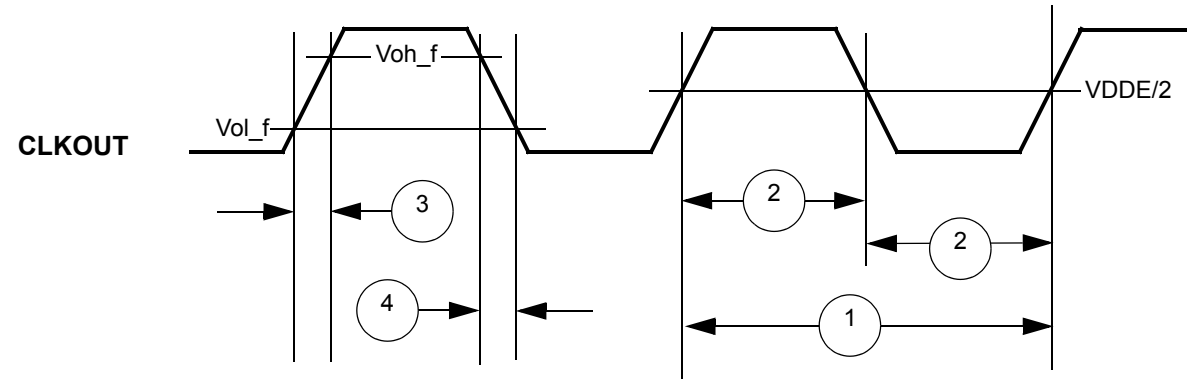


Figure 16. CLKOUT timing

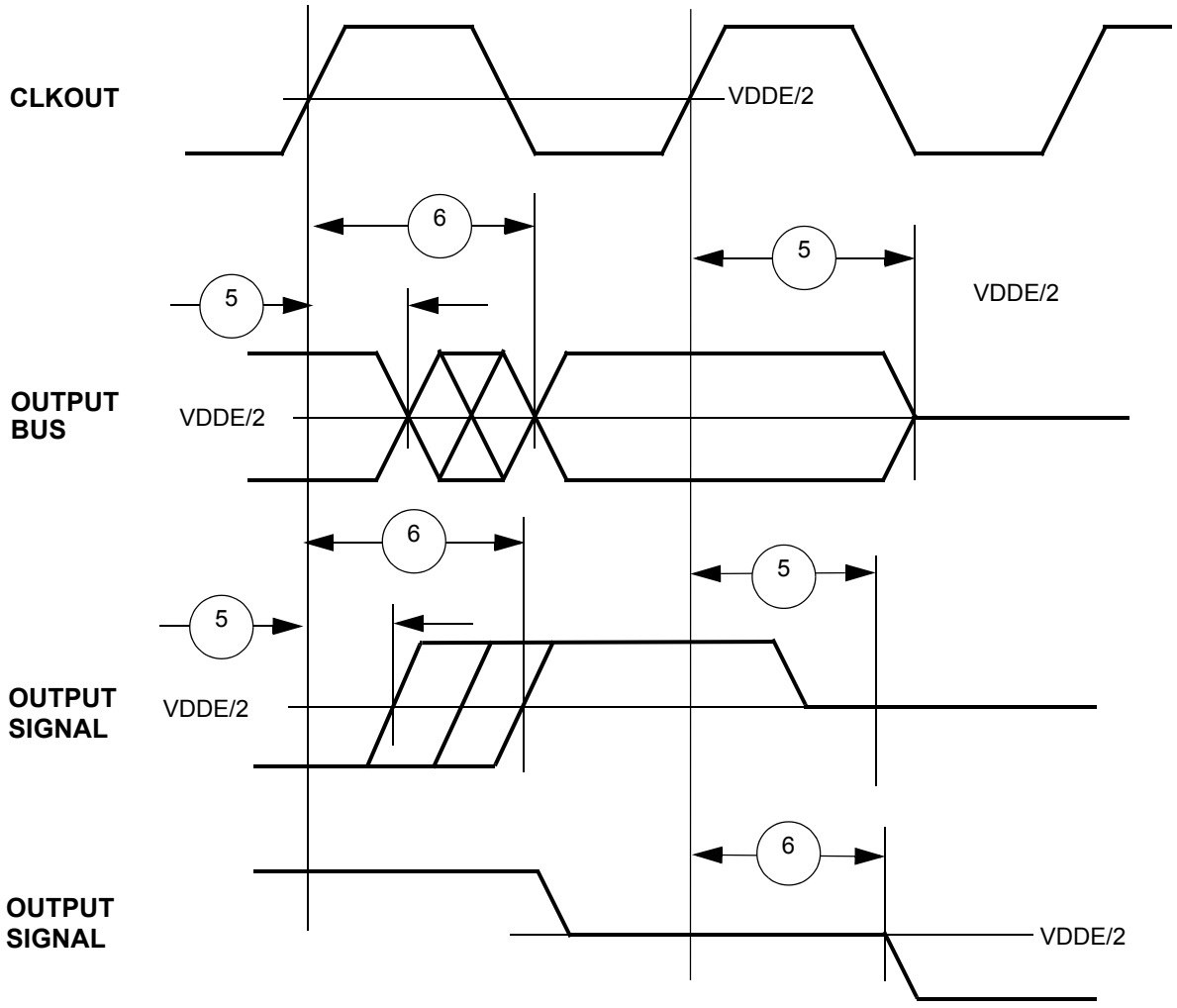


Figure 17. Synchronous output timing

Table 40. DSPI timing[1,2] (continued)

#	Symbol		C	Characteristic	40 MHz		60 MHz		80 MHz		Unit
					Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{HI}	CC	Data Hold Time for Inputs								
			D	Master (MTFE = 0)	–4	—	–4	—	–4	—	ns
			D	Slave	7	—	7	—	7	—	
			D	Master (MTFE = 1, CPHA = 0)[7]	45	—	25	—	21	—	
			D	Master (MTFE = 1, CPHA = 1)	–4	—	–4	—	–4	—	
11	t_{SUO}	CC	Data Valid (after SCK edge)								
			D	Master (MTFE = 0)	—	6	—	6	—	6	ns
			D	Slave	—	25	—	25	—	25	
			D	Master (MTFE = 1, CPHA=0)	—	45	—	25	—	21	
			D	Master (MTFE = 1, CPHA=1)	—	6	—	6	—	6	
12	t_{HO}	CC	Data Hold Time for Outputs								
			D	Master (MTFE = 0)	–5	—	–5	—	–5	—	ns
			D	Slave	5.5	—	5.5	—	5.5	—	
			D	Master (MTFE = 1, CPHA = 0)	8	—	4	—	3	—	
			D	Master (MTFE = 1, CPHA = 1)	–5	—	–5	—	–5	—	

1 All DSPI timing specifications use the fastest slew rate (SRC = 0b11) on pad type M or MH. DSPI signals using pad types of S or SH have an additional delay based on the slew rate. DSPI timing is specified at VDDEH = 3.0–5.25 V, TA = TL to TH, and CL = 50 pF with SRC = 0b11.

2 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 42 MHz parts allow for 40 MHz system clock + 2% FM; 62 MHz parts allow for a 60 MHz system clock + 2% FM, and 82 MHz parts allow for 80 MHz system clock + 2% FM.

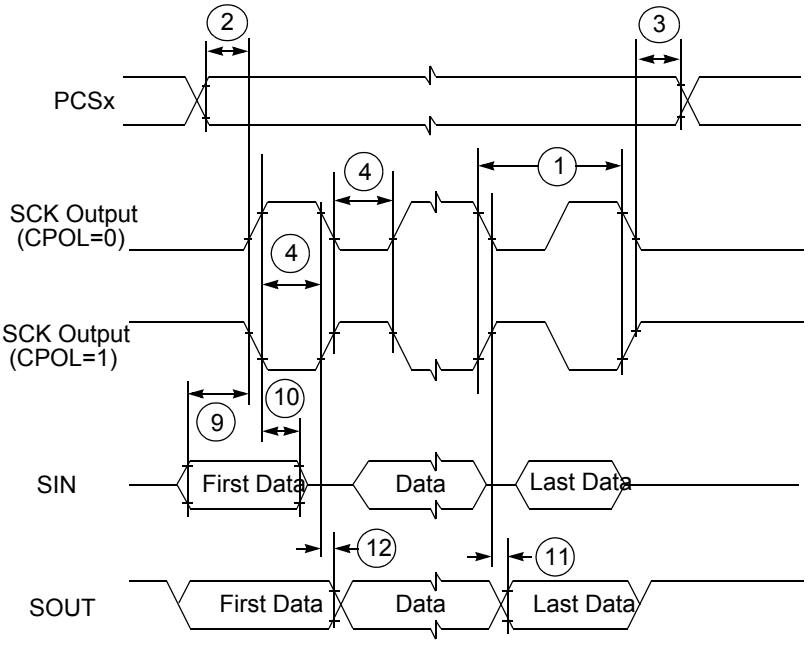
3 The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two MPC5634M devices communicating over a DSPI link.

4 The actual minimum SCK cycle time is limited by pad performance.

5 The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].

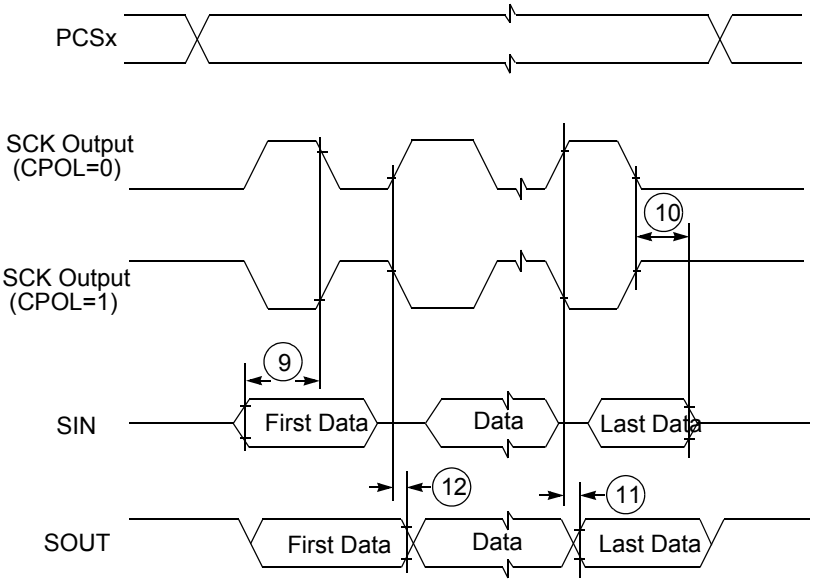
6 The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].

7 This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.



These numbers reference Table 40.

Figure 20. DSPI classic SPI timing – master, CPHA = 0



These numbers reference Table 40.

Figure 21. DSPI classic SPI timing – master, CPHA = 1

4.16.6 eQADC SSI timing

Table 41. eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V)[1]

CLOAD = 25pF on all outputs. Pad drive strength set to maximum.								
#	Symbol		C	Rating	Min	Typ	Max	Unit
1	f_{FCK}	CC	D	FCK Frequency [2, 3]	1/17 f_{SYS_CLK}		1/2 f_{SYS_CLK}	Hertz
1	t_{FCK}	CC	D	FCK Period (t_{FCK} = 1/ f_{FCK})	2 t_{SYS_CLK}		17t_{SYS_CLK}	seconds
2	t_{FCKHT}	CC	D	Clock (FCK) High Time	t_{SYS_CLK} − 6.5		$_{9*}$ t_{SYS_CLK} + 6.5	ns
3	t_{FCKLT}	CC	D	Clock (FCK) Low Time	t_{SYS_CLK} − 6.5		$_{8*}$ t_{SYS_CLK} + 6.5	ns
4	t_{SDS_LL}	CC	D	SDS Lead/Lag Time	–7.5		+7.5	ns
5	t_{SDO_LL}	CC	D	SDO Lead/Lag Time	–7.5		+7.5	ns
6	t_{DVFE}	CC	D	Data Valid from FCK Falling Edge (t_{FCKLT}+t_{SDO_LL})	1			ns
7	t_{EQ_SU}	CC	D	eQADC Data Setup Time (Inputs)	22			ns
8	t_{EQ_HO}	CC	D	eQADC Data Hold Time (Inputs)	1			ns

1 SS timing specified at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.25 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b00.

2 Maximum operating frequency is highly dependent on track delays, master pad delays, and slave pad delays.

3 FCK duty is not 50% when it is generated through the division of the system clock by an odd number.

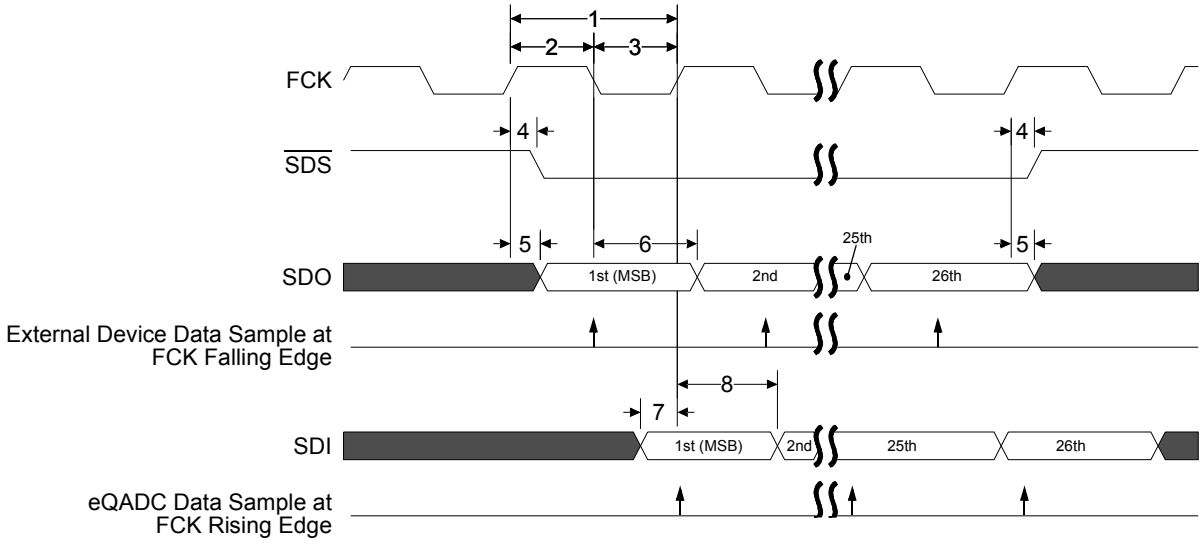


Figure 29. eQADC SSI timing

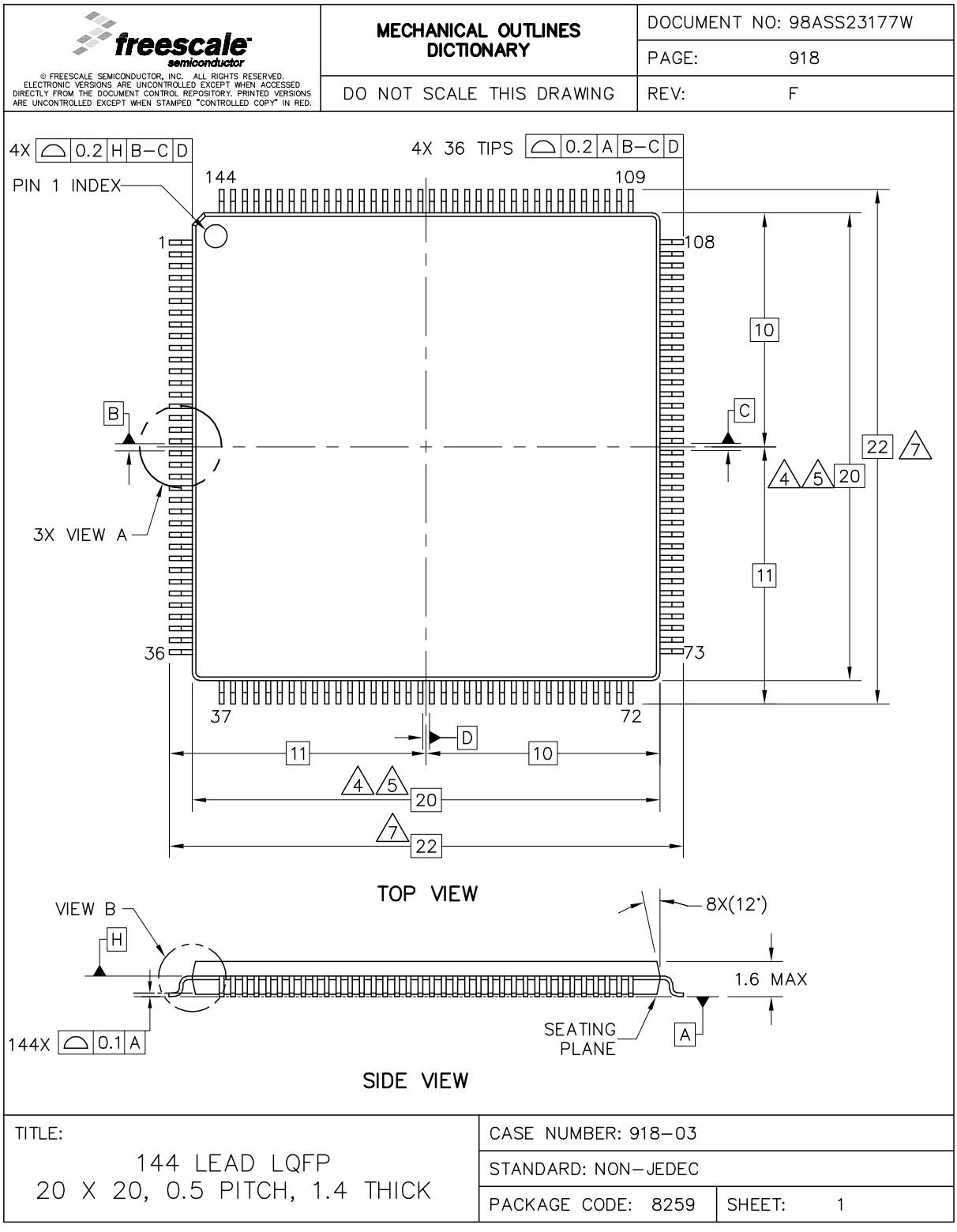
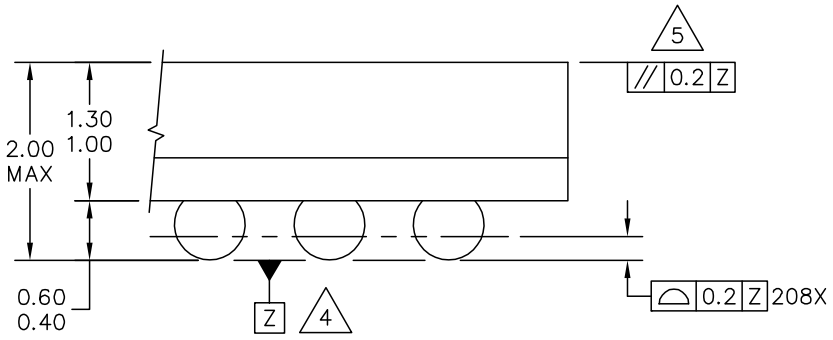


Figure 30. 144 LQFP package mechanical drawing (part 1)

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ARS23882W
		PAGE: 1159A
	DO NOT SCALE THIS DRAWING	REV: D



DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH	CASE NUMBER: 1159A–01	
	STANDARD: JEDEC MO–151 AAF–1	
	PACKAGE CODE: 5253	SHEET: 2 OF 3

Figure 37. 208 MAPBGA package mechanical drawing (part 2)

Table 43. Revision history (continued)

Revision	Date	Description of Changes
Rev 9	05/2012	In Section 4.6.1, “Regulator example • Updated ,Figure 7 “Core voltage regulator controller external components preferred configuration” to show R_C, R_B, R_E, C_C, C_B, C_E, C_D and C_{REG}. • Added Table 15 “Required external PMC component values”, Table 16 “Network 1 component values”, Table 17 “Network 2 component values” and Table 18 “Network 3 component values”. Updated Table 1: Number of eMIOS channels changed from ‘8’ to ‘16’ for MPC5632M. In Section 4.2, “Maximum ratings, Table 7 • V_{FLASH} maximum value changed from 3.6V to 5.5V and changed table note3 to: “The V_{FLASH} supply is connected to V_{DDEH}” • Removed table note 4, “Allowed 5.3 V for 10 hours cumulative time, remaining time at 3.3 V +10%” In Section 4.12, “eQADC electrical characteristics: • Added note. • In Table 29, additional five parameters added (SNR, THD, SFDR, SINAD and ENOB) and added footnotes # 9,10 and 11.