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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	94K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5634mf1mlq80

- Frequency Modulating Phase-locked loop (FMPLL)
  - Reference clock pre-divider (PREDIV) for finer frequency synthesis resolution
  - Reduced frequency divider (RFD) for reducing the FMPLL output clock frequency without forcing the FMPLL to re-lock
  - System clock divider (SYSDIV) for reducing the system clock frequency in normal or bypass mode
  - Input clock frequency range from 4 MHz to 20 MHz before the pre-divider, and from 4 MHz to 16 MHz at the FMPLL input
  - Voltage controlled oscillator (VCO) range from 256 MHz to 512 MHz
  - VCO free-running frequency range from 25 MHz to 125 MHz
  - Four bypass modes: crystal or external reference with PLL on or off
  - Two normal modes: crystal or external reference
  - Programmable frequency modulation
    - Triangle wave modulation
    - Register programmable modulation frequency and depth
  - Lock detect circuitry reports when the FMPLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
    - User-selectable ability to generate an interrupt request upon loss of lock
    - User-selectable ability to generate a system reset upon loss of lock
  - Clock quality monitor (CQM) module provides loss-of-clock detection for the FMPLL reference and output clocks
    - User-selectable ability to generate an interrupt request upon loss of clock
    - User-selectable ability to generate a system reset upon loss of clock
    - Backup clock (reference clock or FMPLL free-running) can be applied to the system in case of loss of clock
- Calibration bus interface (EBI)
  - Available only in the calibration package (496 CSP package)
  - 1.8 V to 3.3 V ± 10% I/O (1.6 V to 3.6 V)
  - Memory controller with support for various memory types
  - 16-bit data bus, up to 22-bit address bus
  - Selectable drive strength
  - Configurable bus speed modes
  - Bus monitor
  - Configurable wait states
- System integration unit (SIU)
  - Centralized GPIO control of 80 I/O pins
  - Centralized pad control on a per-pin basis
    - Pin function selection
    - Configurable weak pull-up or pull-down
    - Drive strength
    - Slew rate
    - Hysteresis
  - System reset monitoring and generation
  - External interrupt inputs, filtering and control
  - Critical Interrupt control
  - Non-Maskable Interrupt control
  - Internal multiplexer subblock (IMUX)
    - Allows flexible selection of eQADC trigger inputs (eTPU, eMIOS and external signals)

  - SCK to PCS delay
  - Delay between frames
  - Programmable serial frame size of 4 to 16 bits, expandable with software control
  - Continuously held chip select capability
- 6 Peripheral Chip Selects, expandable to 64 with external demultiplexer
- Deglitching support for up to 32 Peripheral Chip Selects with external demultiplexer
- DMA support for adding entries to TX FIFO and removing entries from RX FIFO:
  - TX FIFO is not full (TFFF)
  - RX FIFO is not empty (RFDF)
- 6 Interrupt conditions:
  - End of queue reached (EOQF)
  - TX FIFO is not full (TFFF)
  - Transfer of current frame complete (TCF)
  - Attempt to transmit with an empty Transmit FIFO (TFUF)
  - RX FIFO is not empty (RFDF)
  - FIFO Underrun (slave only and SPI mode, the slave is asked to transfer data when the TxFIFO is empty)
  - FIFO Overrun (serial frame received while RX FIFO is full)
- Modified transfer formats for communication with slower peripheral devices
- Continuous Serial Communications Clock (SCK)
- Power savings via support for Stop Mode
- Enhanced DSI logic to implement a 32-bit Timed Serial Bus (TSB) configuration, supporting the Microsecond Channel downstream frame format

The DSPIs also support these features unique to the DSI and CSI configurations:

- 2 sources of the serialized data:
  - eTPU_A and eMIOS output channels
  - Memory-mapped register in the DSPI
- Destinations for the deserialized data:
  - eTPU_A and eMIOS input channels
  - SIU External Interrupt Request inputs
  - Memory-mapped register in the DSPI
- Deserialized data is provided as Parallel Output signals and as bits in a memory-mapped register
- Transfer initiation conditions:
  - Continuous
  - Edge sensitive hardware trigger
  - Change in data
- Pin serialization/deserialization with interleaved SPI frames for control and diagnostics
- Continuous serial communications clock
- Support for parallel and serial chaining of up to four DSPI blocks

2.2.16 eSCI

The enhanced serial communications interface (eSCI) allows asynchronous serial communications with peripheral devices and other MCUs. It includes special support to interface to Local Interconnect Network (LIN) slave devices. The eSCI block provides the following features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format

3 Pinout and signal description

This section contains the pinouts for all production packages for the MPC5634M family of devices. Please note the following:

- Pins labeled “NC” are to be left unconnected. Any connection to an external circuit or voltage may cause unpredictable device behavior or damage.
- Pins labeled “NIC” have no internal connection.

3.1 144 LQFP pinout

Figure 2 shows the pinout for the 144-pin LQFP.

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPBGA
AN[13] MA[1] ETPU_A[21] SDO	Single Ended Analog Input Mux Address ETPU_A Ch. eQADC Serial Data Out	PCR[216]	011 010 100 000	I O O O	VDDEH7	I / –	AN[13] / –		118	147	B12
AN[14] MA[2] ETPU_A[27] SDI	Single Ended Analog Input Mux Address ETPU_A Ch. eQADC Serial Data In	PCR[217]	011 010 100 000	I O O I	VDDEH7	I / –	AN[14] / –		117	146	C12
AN[15] FCK ETPU_A[29]	Single Ended Analog Input eQADC Free Running Clock ETPU_A Ch.	PCR[218]	011 010 000	I O O	VDDEH7	I / –	AN[15] / –		116	145	C13
AN[16]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		3	3	C6
AN[17]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		2	2	C4
AN[18]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		1	1	D5
AN[21]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		144	173	B4
AN[22]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		132	161	B8
AN[23]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		131	160	C9
AN[24]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		130	159	D8
AN[25]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		129	158	B9
AN[27]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		128	157	A10
AN[28]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		127	156	B10
AN[30]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		126	155	D9
AN[31]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		125	154	D10
AN[32]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		124	153	C10
AN[33]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		123	152	C11
AN[34]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		122	151	C5
AN[35]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		121	150	D11
AN[36]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		—	174[7]	F4[8]
AN[37]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		—	175[7]	E3[8]

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPBGA
eTPU_A[28][28] DSPI_C_PCS[1] GPIO[142]	eTPU_A Ch. (Input and Output) DSPI_C Periph Chip Select GPIO	PCR[142]	10 01 00	I/O O I/O	VDDEH1a Medium	– / WKPCFG	– / WKPCFG		17	24	F1
eTPU_A[29][28] DSPI_C_PCS[2] GPIO[143]	eTPU_A Ch. (Input and Output) DSPI_C Periph Chip Select GPIO	PCR[143]	10 01 00	I/O O I/O	VDDEH1a Medium	– / WKPCFG	– / WKPCFG		16	23	F2
eTPU_A[30] DSPI_C_PCS[3] eTPU_A[11] GPIO[144]	eTPU_A Ch. DSPI_C Periph Chip Select eTPU_A Ch. GPIO	PCR[144]	011 010 001 000	I/O O O I/O	VDDEH1a Medium	– / WKPCFG	– / WKPCFG		15	22	E1
eTPU_A[31] DSPI_C_PCS[4] eTPU_A[13] GPIO[145]	eTPU_A Ch. DSPI_C Periph Chip Select eTPU_A Ch. GPIO	PCR[145]	011 010 001 000	I/O O O I/O	VDDEH1a Medium	– / WKPCFG	– / WKPCFG		14	21	E2
eMIOS											
eMIOS[0] eTPU_A[0] eTPU_A[25][29] GPIO[179]	eMIOS Ch. eTPU_A Ch. eTPU_A Ch. GPIO	PCR[179]	001 010 100 000	I/O O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		54	63	T4
eMIOS[1] eTPU_A[1] GPIO[180]	eMIOS Ch. eTPU_A Ch. GPIO	PCR[180]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		—	64[7]	T5[8]
eMIOS[2] eTPU_A[2] GPIO[181]	eMIOS Ch. eTPU_A Ch. GPIO	PCR[181]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		55	65	N7
eMIOS[4] eTPU_A[4] GPIO[183]	eMIOS Ch. eTPU_A Ch. GPIO	PCR[183]	01 10 00	I/O O I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		56	67	R5
eMIOS[8] eTPU_A[8][30] SCI_B_TX GPIO[187]	eMIOS Ch. eTPU_A Ch. eSCI_B Transmit GPIO	PCR[187]	001 010 100 000	I/O O O I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		57	70	P8

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPBGA
VSTBY	Power Supply for Standby RAM	—	—	I	VSTBY	I / –	—		12	12	C1
VRC33	3.3V Voltage Regulator Bypass Capacitor	—	—	O	VRC33	O / –	—		13	13	A15, D1, N6, N12
VRCCTL	Voltage Regulator Control Output	—	—	O	NA	O / –	—		11	11	N14
VDDA[34]	Analog Power Input for eQADC	—	—	I	VDDA (5.0 V)	I / –	—		6	6	—
VDDA0	Analog Power Input for eQADC	—	—	I	VDDA	I / –	—		—	—	B11
VSSA0	Analog Ground Input for eQADC	—	—	I	VSSA	I / –	—		—	—	A11
VDDA1	Analog Power Input for eQADC	—	—	I	VDDA	I / –	—		—	—	A4
VSSA1	Analog Ground Input for eQADC	—	—	I	VSSA	I / –	—		—	—	A5
VSSA[35]	Analog Ground Input for eQADC	—	—	I	VSSA	I / –	—		7	7	—
VDDREG	Voltage Regulator Supply	—	—	I	VDDREG (5.0 V)	I / –	—		10	10	K16
VDD	Internal Logic Supply Input	—	—	I	VDD (1.2 V)	I / –	—		26, 53, 86, 120	33, 62, 103, 149	B1, B16, C2, D3, E4, N5, P4, P13, R3, R14, T2, T15

3.7 Signal details

Table 4 contains details on the multiplexed signals that appear in Table 2, “MPC563xM signal properties”.

Table 4. Signal details

Signal	Module or Function	Description
CLKOUT	Clock Generation	MPC5634M clock output for the external/calibration bus interface
EXTAL	Clock Generation	Input pin for an external crystal oscillator or an external clock source based on the value driven on the PLLREF pin at reset.
EXTCLK	Clock Generation	External clock input
PLLREF	Clock Generation	PLLREF is used to select whether the oscillator operates in xtal mode or external reference mode from reset. PLLREF=0 selects external reference mode.
XTAL	Clock Generation	Crystal oscillator input
SCK_B_LVDS– SCK_B_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission
SOUT_B_LVDS– SOUT_B_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission
SCK_C_LVDS– SCK_C_LVDS+	DSPI	LVDS pair used for DSPI_C TSB mode transmission
SOUT_C_LVDS– SOUT_C_LVDS+	DSPI	LVDS pair used for DSPI_C TSB mode transmission
PCS_B[0] PCS_C[0]	DSPI_B – DSPI_C	Peripheral chip select when device is in master mode—slave select when used in slave mode
PCS_B[1:5] PCS_C[1:5]	DSPI_B – DSPI_C	Peripheral chip select when device is in master mode—not used in slave mode
SCK_B SCK_C	DSPI_B – DSPI_C	DSPI clock—output when device is in master mode; input when in slave mode
SIN_B SIN_C	DSPI_B – DSPI_C	DSPI data in
SOUT_B SOUT_C	DSPI_B – DSPI_C	DSPI data out
CAL_ADDR[12:30]	Calibration Bus	The CAL_ADDR[12:30] signals specify the physical address of the bus transaction.
CAL_$\overline{\text{CS}}$[0:3]	Calibration Bus	$\overline{\text{CS}}$x is asserted by the master to indicate that this transaction is targeted for a particular memory bank on the Primary external bus.
CAL_DATA[0:15]	Calibration Bus	The CAL_DATA[0:15] signals contain the data to be transferred for the current transaction.
CAL_$\overline{\text{OE}}$	Calibration Bus	$\overline{\text{OE}}$ is used to indicate when an external memory is permitted to drive back read data. External memories must have their data output buffers off when $\overline{\text{OE}}$ is negated. $\overline{\text{OE}}$ is only asserted for chip-select accesses.

[8] Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met.

[9] Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.

[10] Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.

[11] Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

[12] Total injection current for all analog input pins must not exceed 15 mA.

[13] Lifetime operation at these specification limits is not guaranteed.

[14] Solder profile per CDF-AEC-Q100.

[15] Moisture sensitivity per JEDEC test method A112.

4.3 Thermal characteristics

Table 8. Thermal characteristics for 144-pin LQFP

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[1]	Single layer board – 1s	43	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board – 2s2p	35	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Ambient (@200 ft/min)[2]	Single layer board –1s	34	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Ambient (@200 ft/min)[2]	Four layer board – 2s2p	29	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board[2]		22	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-Case (Top)[3]		8	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection[4]		2	°C/W

[1] Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

[2] Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

[3] Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

[4] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 9. Thermal characteristics for 176-pin LQFP[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Single layer board - 1s	38	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board - 2s2p	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	@200 ft./min., single layer board - 1s	30	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	@200 ft./min., four layer board - 2s2p	25	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board[3]		20	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-Case[4]		5	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection[5]		2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 10. Thermal characteristics for 208-pin MAPBGA[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection[2,3]	One layer board - 1s	39	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-ambient natural convection[2,4]	Four layer board - 2s2p	24	°C/W
$R_{\theta JA}$	CC	D	Junction-to-ambient (@200 ft/min)[2,4]	Single layer board	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-ambient (@200 ft/min)[2,4]	Four layer board 2s2p	20	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[5]	Four layer board - 2s2p	13	°C/W
$R_{\theta JC}$	CC	D	Junction-to-case[6]		6	°C/W
Ψ_{JT}	CC	D	Junction-to-package top natural convection[7]		2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

Table 14. PMC electrical characteristics (continued)

ID	Name		C	Parameter	Min	Typ	Max	Unit	Notes
1d	—	CC	C	Bandgap reference supply voltage variation	—	3000	—	ppm /V	
2	Vdd	CC	C	Nominal VDD core supply internal regulator target DC output voltage[2]	—	1.28	—	V	
2a	—	CC	P	Nominal VDD core supply internal regulator target DC output voltage variation at power-on reset	Vdd – 6%	Vdd	Vdd + 10%	V	
2b	—	CC	P	Nominal VDD core supply internal regulator target DC output voltage variation after power-on reset	Vdd – 10[3]	Vdd	Vdd + 3%	V	
2c	—	CC	C	Trimming step Vdd	—	20	—	mV	
2d	Ivrcctl	CC	C	Voltage regulator controller for core supply maximum DC output current	20	—	—	mA	
3	Lvi1p2	CC	C	Nominal LVI for rising core supply[4,5]	—	1.160	—	V	
3a	—	CC	C	Variation of LVI for rising core supply at power-on reset[5,6]	1.120	1.200	1.280	V	
3b	—	CC	C	Variation of LVI for rising core supply after power-on reset[5,6]	Lvi1p2–3%	Lvi1p2	Lvi1p2+3%	V	
3c	—	CC	C	Trimming step LVI core supply[5]	—	20	—	mV	
3d	Lvi1p2_h	CC	C	LVI core supply hysteresis[5]	—	40	—	mV	
4	Por1.2V_r	CC	C	POR 1.2 V rising	—	0.709	—	V	
4a	—	CC	C	POR 1.2 V rising variation	Por1.2V_r– 35%	Por1.2V_r	Por1.2V_r+ 35%	V	
4b	Por1.2V_f	CC	C	POR 1.2 V falling	—	0.638	—	V	
4c	—	CC	C	POR 1.2 V falling variation	Por1.2V_f– 35%	Por1.2V_f	Por1.2V_f+ 35%	V	
5	Vdd33	CC	C	Nominal 3.3 V supply internal regulator DC output voltage	—	3.39	—	V	
5a	—	CC	P	Nominal 3.3 V supply internal regulator DC output voltage variation at power-on reset[6]	Vdd33 – 8.5%	Vdd33	Vdd3 + 7%	V	

Table 22. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
V_{OH_LS}	CC	P	Multi-voltage pad I/O output high voltage in low-swing mode[10,11,12,13,17]	I_{OH_LS} = 0.5 mA Min V_{DDEH} = 4.75 V	2.1	—	3.7	V
V_{OH_HS}	CC	P	Multi-voltage pad I/O output high voltage in high-swing mode[17]	—	0.8 V_{DDEH}	—	—	V
V_{HYS_S}	CC	C	Slow/medium/multi-voltage I/O input hysteresis	—	0.1 * V_{DDEH}	—	—	V
V_{HYS_F}	CC	C	Fast I/O input hysteresis	—	0.1 * V_{DDE}	—	—	V
V_{HYS_LS}	CC	C	Low-Swing-Mode Multi-Voltage I/O Input Hysteresis	hysteresis enabled	0.25	—	—	V
I_{DD}+I_{DDPLL}[19]	CC	P	Operating current 1.2 V supplies	V_{DD} = 1.32 V, 80 MHz	—	—	195	mA
	CC	P		V_{DD} = 1.32 V, 60 MHz	—	—	135	
	CC	P		V_{DD} = 1.32 V, 40 MHz	—	—	98	
I_{DDSTBY}	CC	T	Operating current 1 V supplies	T_J = 25 °C	—	—	80	µA
	CC	T		T_J = 55 °C	—	—	100	µA
$I_{DDSTBY150}$	CC	P	Operating current	T_J=150 °C	—	—	700	µA
I_{DDSLOW} I_{DDSTOP}	CC	P	V_{DD} low-power mode operating current @ 1.32 V	Slow mode[20]	—	—	50	mA
		C		Stop mode[21]	—	—	50	
I_{DD33}	CC	T	Operating current 3.3 V supplies @ 80 MHz	V_{RC33}[4,22]	—	—	70	mA
I_{DDA} I_{REF} I_{DDREG}	CC	P	Operating current 5.0 V supplies @ 80 MHz	V_{DDA}	—	—	30	mA
		P		Analog reference supply current	—	—	1.0	
		C		V_{DDREG}	—	—	70	

Table 29. eQADC conversion specifications (operating) (continued)

Symbol		C	Parameter		Value		Unit
					min	max	
TUE8	CC	C	Total unadjusted error (TUE) at 8 MHz[9]		–4	4	Counts
TUE16	CC	C	Total unadjusted error at 16 MHz[10]		–8	8	Counts
SNR	CC	T	Signal to Noise Ratio[11]		55.2		dB
THD	CC	T	Total Harmonic Distorsion		70.0		dB
SFDR	CC	T	Spurious Free Dynamic Range		65.0		dB
SINAD	CC	T	Signal to Noise and Distorsion		55.0		dB
ENOB	CC	T	Effective Number of Bits		8.8		Counts
GAINVGA1	CC	–	Variable gain amplifier accuracy (gain=1)[12]				
	CC	C	INL	8 MHz ADC	–4	4	Counts[13]
	CC	C		16 MHz ADC	–8	8	Counts
	CC	C	DNL	8 MHz ADC	–3[14]	3[14]	Counts
	CC	C		16 MHz ADC	–3[14]	3[14]	Counts
GAINVGA2	CC	–	Variable gain amplifier accuracy (gain=2)[12]				
	CC	D	INL	8 MHz ADC	–5	5	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–3	3	Counts
	CC	D		16 MHz ADC	–3	3	Counts
GAINVGA4	CC	–	Variable gain amplifier accuracy (gain=4)[12]				
	CC	D	INL	8 MHz ADC	–7	7	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–4	4	Counts
	CC	D		16 MHz ADC	–4	4	Counts
$DIFF_{max}$	CC	C	Maximum differential voltage (DANx+ - DANx-) or (DANx- - DANx+)	PREGAIN set to 1X setting	–	(VRH - VRL)/2	V
$DIFF_{max2}$	CC	C		PREGAIN set to 2X setting	–	(VRH - VRL)/4	V
$DIFF_{max4}$	CC	C		PREGAIN set to 4X setting	–	(VRH - VRL)/8	V
$DIFF_{cmv}$	CC	C	Differential input Common mode voltage (DANx- + DANx+)/2[15]		(VRH - VRL)/2 - 5%	(VRH - VRL)/2 + 5%	V

1 Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions.Delay from power up to full accuracy = 8 ms.

2 At $V_{RH} – V_{RL}$ = 5.12 V, one count = 1.25 mV. Without using pregain.

3 Below disruptive current conditions, the channel being stressed has conversion values of 0x3FF for analog inputs greater then V_{RH} and 0x0 for values less then V_{RL}. Other channels are not affected by non-disruptive conditions.

[4] Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

[5] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA} + 0.5$ V and $V_{NEGCLAMP} = – 0.3$ V, then use the larger of the calculated values.

[6] Condition applies to two adjacent pins at injection limits.

[7] Performance expected with production silicon.

[8] All channels have same 10 kΩ < Rs < 100 kΩ; Channel under test has Rs=10 kΩ; I_{INJ}=I_{INJMAX},I_{INJMIN}.

[9] TUE is tested by averaging 10 samples.

[10] TUE is tested by averaging three samples.

[11] These values can be significantly improved by using three samples of averaging. Input frequency of 1 kHz was used as the reference for the Signal to Noise Ratio.

[12] Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed by as indicated.

[13] At $V_{RH} – V_{RL} = 5.12$ V, one LSB = 1.25 mV.

[14] Guaranteed 10-bit monotonicity.

[15] Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

Table 32. Flash module life

Symbol		Parameter	Conditions	Value		Unit
				Min	Typ	
P/E	C	Number of program/erase cycles per block for 16 Kbyte blocks over the operating temperature range (T_J)	—	100,000	—	cycles
P/E	C	Number of program/erase cycles per block for 32 and 64 Kbyte blocks over operating temperature range (T_J)	—	10,000	100,000	cycles
P/E	C	Number of program/erase cycles per block for 128 Kbyte blocks over the operating temperature range (T_J)	—	1,000	100,000	cycles
Retention	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0 – 1,000 P/E cycles	20	—	years
			Blocks with 10,000 P/E cycles	10	—	years
			Blocks with 100,000 P/E cycles	5	—	years

[1] Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

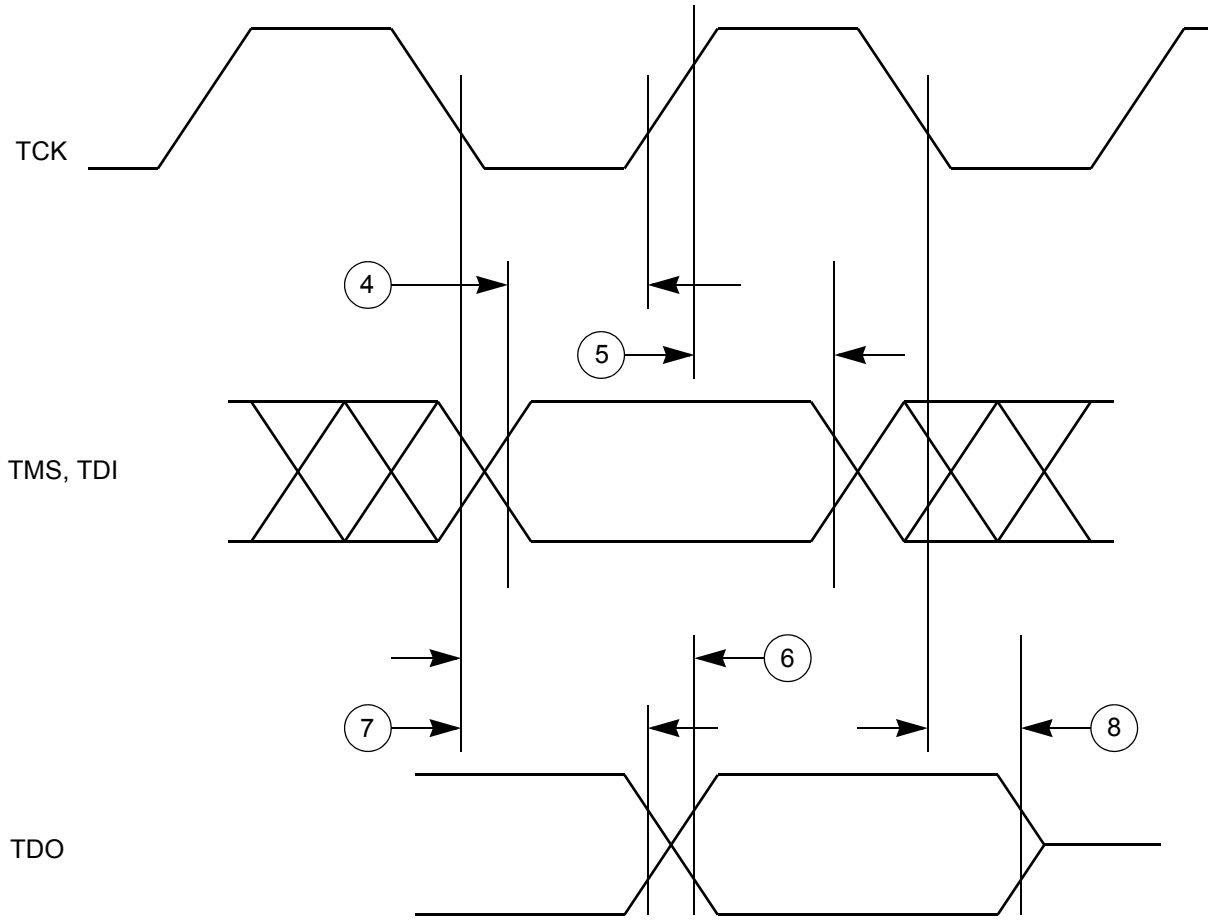

Figure 10. JTAG test access port timing

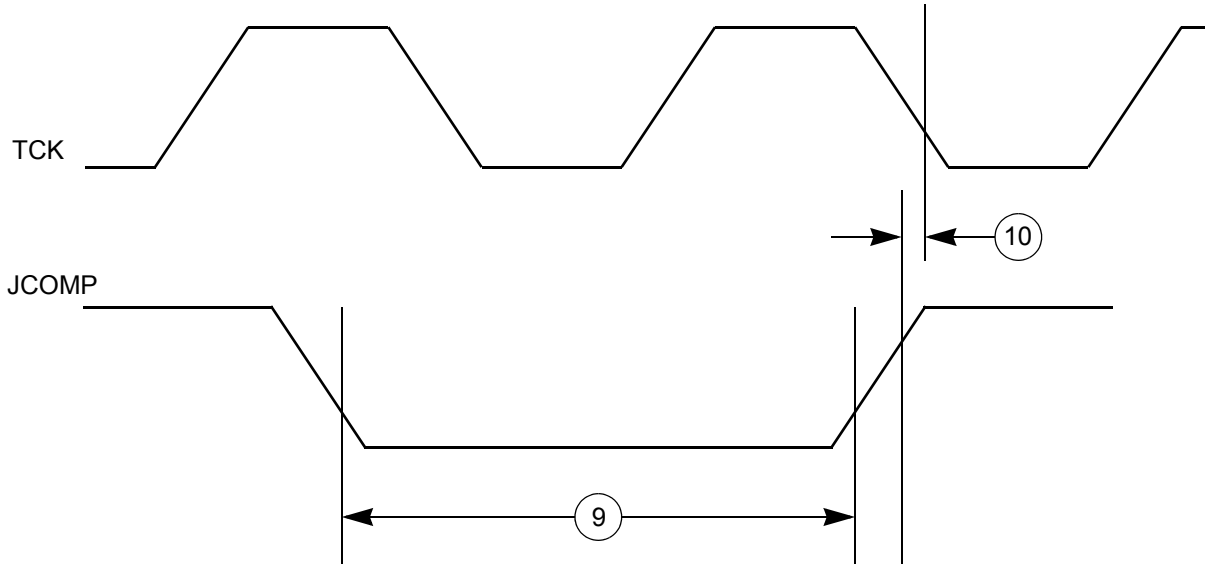

Figure 11. JTAG JCOMP timing

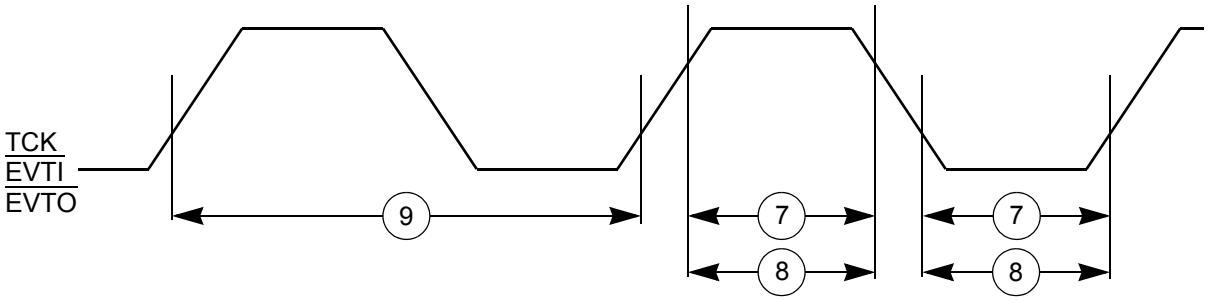

Figure 14. Nexus event trigger and test clock timings

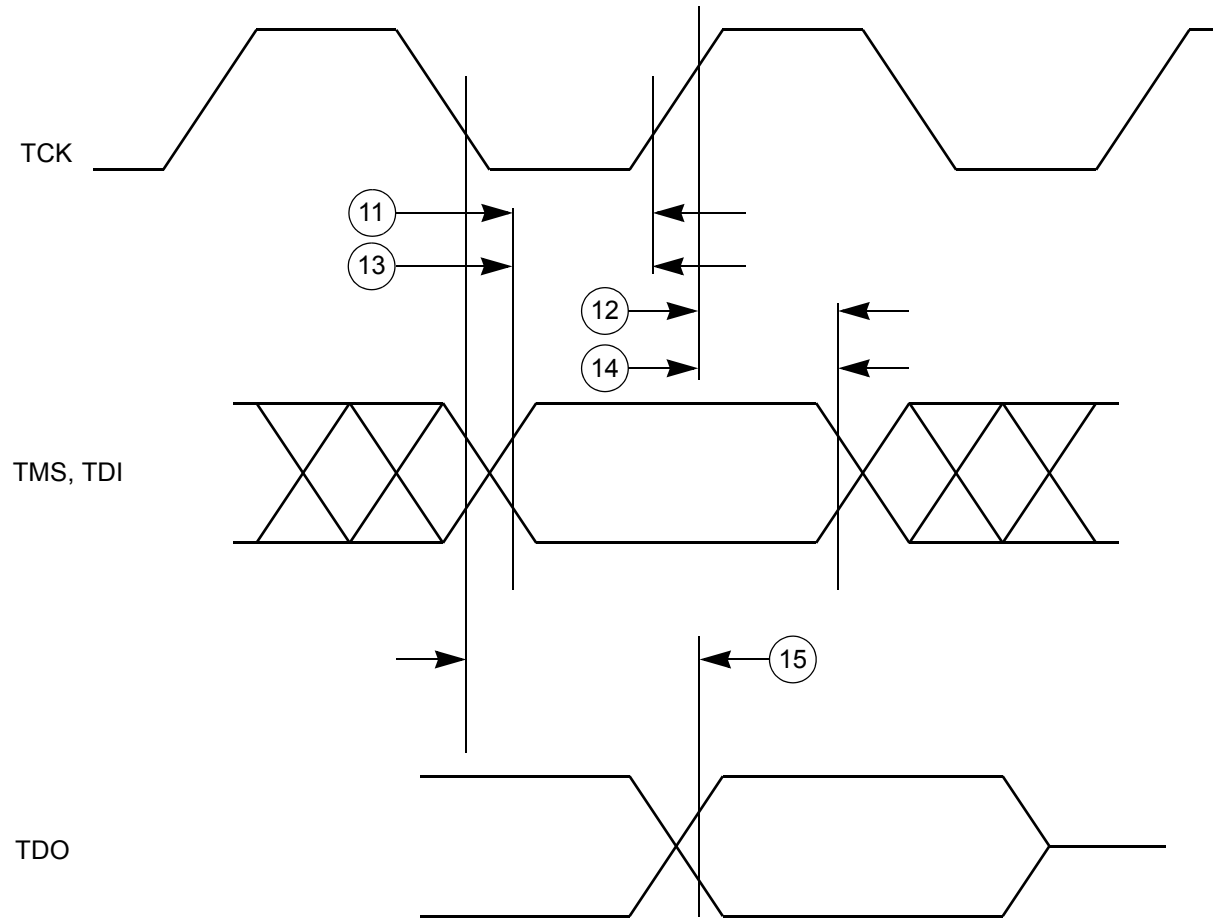

Figure 15. Nexus TDI, TMS, TDO timing

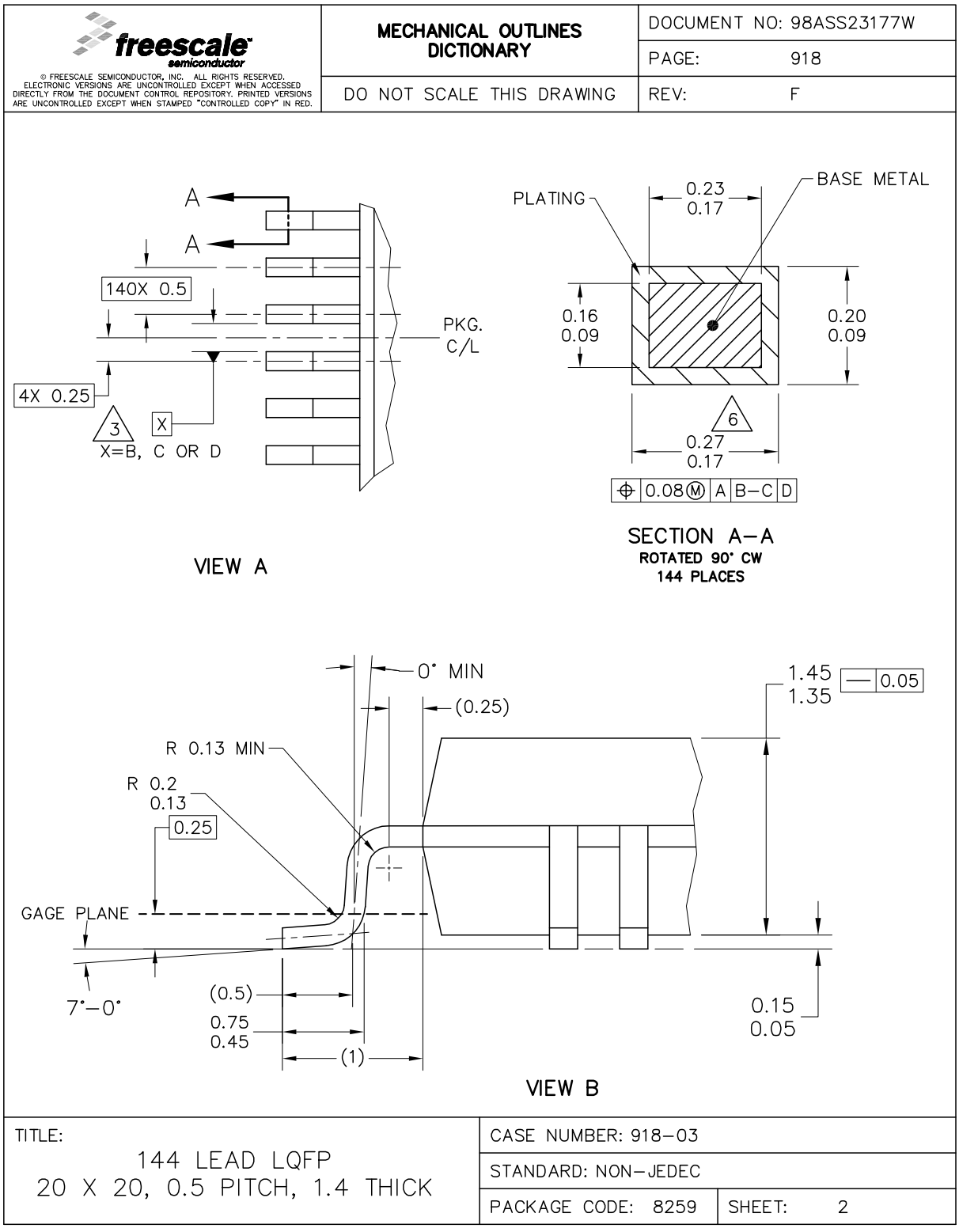

Figure 31. 144 LQFP package mechanical drawing (part 2)

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		PAGE: 918
	DO NOT SCALE THIS DRAWING	REV: F

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.
4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 mm.
5. THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.
7. THIS DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

TITLE: 144 LEAD LQFP 20 X 20, 0.5 PITCH, 1.4 THICK	CASE NUMBER: 918–03	
	STANDARD: NON–JEDEC	
	PACKAGE CODE: 8259	SHEET: 3

Figure 32. 144 LQFP package mechanical drawing (part 3)

Table 43. Revision history (continued)

Revision	Date	Description of Changes
Rev. 5 (cont.)	04/2010	Changes to flash memory specifications: • T_{BKPRG} 64 KB specification removed (not present in this device) • $T_{64kpperase}$ specification added • Flash module life P/E spec for 32 Kbyte blocks also applies to 64 Kbyte blocks Pad AC specifications (3.3 V) table updated
Rev. 6	04/2010	"Core Voltage Regulator Controller External Components Preferred Configuration" circuit diagram updated. • Clarification added to note: Emitter and collector capacitors (6.8 μF and 10 μF) should be matched (same type) and ESR should be lower than 200 mW. (Added emphasis that only 6.8 μF emitter capacitors need to be matched with collector capacitor. • 220 μF emitter capacitors changed to 220 nF.
Rev. 7	4/2010	No specification or product information changes: • Mechanical outline drawings section renamed to "Packages" and restructured. •
Rev. 8	01/2011	Removed the 208 BGA package from the device-summary table. Revised the "PMC Operating conditions and external regulators supply voltage" table. Revised the "PMC electrical characteristics" table. Revised the pad AC specifications. Revised the "DC electrical specifications" table. Revised the "DSPI LVDS pad specification" table: Revised the "PLLMRFM electrical specifications" table. Change to "Temperature sensor electrical characteristics" table: • Accuracy is guaranteed by production test Revised the "eQADC conversion specifications (operating)" table. Changes to "Calibration bus operation timing" table: • CLKOUT period is guaranteed by production test. All other parameters are guaranteed by design Changes to "Program and erase specifications" table in "Flash memory electrical characteristics" section. • Deleted Bank Program (512KB) (T_{BKPRG}) parameter • TYP P/E values added for 32- and 64 KB blocks and for 128 KB blocks. Changes to Recommended operating characteristics for external power transistor: • VCESAT should be between 200 and 600 mV • VBE should be 0.4V to 1.0V Removed footnote 8 from Vddeh in Maximum ratings. Deleted engineering names for pads in Power UP/DOWN Sequencing Section Changed "sin_c" to DSPI_C_SIN" and "sck_c" to DSPI_C_SCK" on 144 pin LQFP package. Updated the "Electromagnetic Interference Characteristics" table to reflect new parameter levels, test conditions. In the "APC, RWSC, WWSC settings vs. frequency of operation" table, changed 82 MHz entry for WWC from "11" to "01", added an extra row for "All 111 111 11"

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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
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Chaoyang District
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China
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