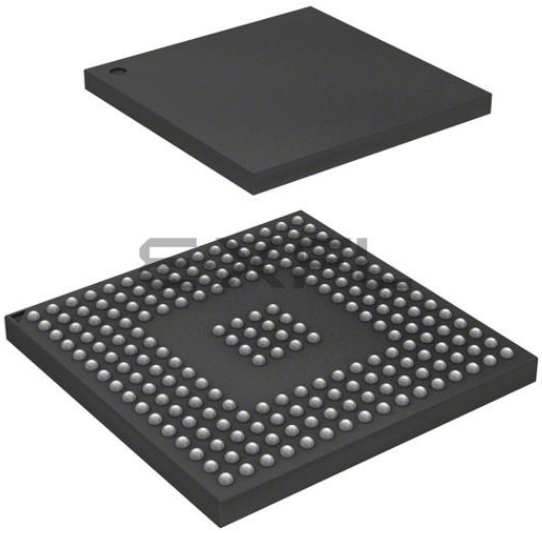

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	94K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BGA
Supplier Device Package	208-BGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5634mf1mmg80

— Four pairs of differential analog input channels
— Full duplex synchronous serial interface to an external device
  – Has a free-running clock for use by the external device
  – Supports a 26-bit message length
  – Transmits a null message when there are no triggered CFIFOs with commands bound for external CBuffers, or when there are triggered CFIFOs with commands bound for external CBuffers but the external CBuffers are full
— Parallel Side Interface to communicate with an on-chip companion module
— Zero jitter triggering for queue 0. (Queue 0 trigger causes current conversion to be aborted and the queued conversions in the CBUFFER to be bypassed. Delay from Trigger to start of conversion is 13 system clocks + 1 ADC clock.)
— eQADC Result Streaming. Generation of a continuous stream of ADC conversion results from a single eQADC command word. Controlled by two different trigger signals; one to define the rate at which results are generated and the other to define the beginning and ending of the stream. Used to digitize waveforms during specific time/angle windows, e.g., engine knock sensor sampling.
— Angular Decimation. The ability of the eQADC to sample an analog waveform in the time domain, perform Finite Impulse Response (FIR) or Infinite Impulse Response (IIR) filtering also in the time domain, but to down sample the results in the angle domain. Resulting in a time domain filtered result at a given engine angle.
— Priority Based CFIFOs
  – Supports six CFIFOs with fixed priority. The lower the CFIFO number, the higher its priority. When commands of distinct CFIFOs are bound for the same CBuffer, the higher priority CFIFO is always served first.
  – Supports software and several hardware trigger modes to arm a particular CFIFO
  – Generates interrupt when command coherency is not achieved
— External Hardware Triggers
  – Supports rising edge, falling edge, high level and low level triggers
  – Supports configurable digital filter
— Supports four external 8-to-1 muxes which can expand the input channel number from 34[1] to 59

- Two deserial serial peripheral interface modules (DSPI)
  — SPI
    – Full duplex communication ports with interrupt and DMA request support
    – Supports all functional modes from QSPI subblock of QSMCM (MPC5xx family)
    – Support for queues in RAM
    – 6 chip selects, expandable to 64 with external demultiplexers
    – Programmable frame size, baud rate, clock delay and clock phase on a per frame basis
    – Modified SPI mode for interfacing to peripherals with longer setup time requirements
    – LVDS option for output clock and data to allow higher speed communication
  — Deserial serial interface (DSI)
    – Pin reduction by hardware serialization and deserialization of eTPU, eMIOS channels and GPIO
    – 32 bits per DSPI module
    – Triggered transfer control and change in data transfer control (for reduced EMI)
    – Compatible with Microsecond Channel Version 1.0 downstream
- Two enhanced serial communication interface (eSCI) modules
  — UART mode provides NRZ format and half or full duplex interface
  — eSCI bit rate up to 1 Mbps

1. 176-pin and 208-pin packages have 34 input channels; 144-pin package has 32.
1. 176-pin and 208-ball packages.

- Channel transfers can be suspended by a higher priority channel

2.2.4 Interrupt controller

The INTC (interrupt controller) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems. The INTC allows interrupt request servicing from up to 191 peripheral interrupt request sources, plus 165 sources reserved for compatibility with other family members).

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

Multiple processors can assert interrupt requests to each other through software setable interrupt requests. These same software setable interrupt requests also can be used to break the work involved in servicing an interrupt request into a high priority portion and a low priority portion. The high priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software setable interrupt request to finish the servicing in a lower priority ISR. Therefore these software setable interrupt requests can be used instead of the peripheral ISR scheduling a task through the RTOS.

The INTC provides the following features:

- 356 peripheral interrupt request sources
- 8 software setable interrupt request sources
- 9-bit vector addresses
- Unique vector for each interrupt request source
- Hardware connection to processor or read from register
- Each interrupt source can be programmed to one of 16 priorities
- Preemptive prioritized interrupt requests to processor
- ISR at a higher priority preempts executing ISRs or tasks at lower priorities
- Automatic pushing or popping of preempted priority to or from a LIFO
- Ability to modify the ISR or task priority to implement the priority ceiling protocol for accessing shared resources
- Low latency—three clocks from receipt of interrupt request from peripheral to interrupt request to processor

This device also includes a non-maskable interrupt (NMI) pin that bypasses the INTC and multiplexing logic.

2.2.5 FMPLL

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 20 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable. The PLL has the following major features:

- Input clock frequency from 4 MHz to 20 MHz
- Voltage controlled oscillator (VCO) range from 256 MHz to 512 MHz, resulting in system clock frequencies from 16 MHz to 80 MHz with granularity of 4 MHz or better
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- 3 modes of operation
  - Bypass mode with PLL off
  - Bypass mode with PLL running (default mode out of reset)
  - PLL normal mode

The flash memory provides the following features:

- Supports a 64-bit data bus for instruction fetch, CPU loads and DMA access. Byte, halfword, word and doubleword reads are supported. Only aligned word and doubleword writes are supported.
- Fetch Accelerator
  - Architected to optimize the performance of the flash with the CPU to provide single cycle random access to the flash up to 80 MHz system clock speed
  - Configurable read buffering and line prefetch support
  - Four line read buffers (128 bits wide) and a prefetch controller
- Hardware and software configurable read and write access protections on a per-master basis
- Interface to the flash array controller is pipelined with a depth of one, allowing overlapped accesses to proceed in parallel for interleaved or pipelined flash array designs
- Configurable access timing allowing use in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (0-31 additional cycles) allowing use for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page size of 128 bits (four words)
- ECC with single-bit correction, double-bit detection
- Program page size of 64 bits (two words)
- ECC single-bit error corrections are visible to software
- Minimum program size is two consecutive 32-bit words, aligned on a 0-modulo-8 byte address, due to ECC
- Embedded hardware program and erase algorithm
- Erase suspend
- Shadow information stored in non-volatile shadow block
- Independent program/erase of the shadow block

2.2.10 SRAM

The MPC5634M SRAM module provides a general-purpose up to 94 KB memory block. The SRAM controller includes these features:

- Supports read/write accesses mapped to the SRAM memory from any master
- 32 KB or 24 KB block powered by separate supply for standby operation
- Byte, halfword, word and doubleword addressable
- ECC performs single-bit correction, double-bit detection on 32-bit data element

2.2.11 BAM

The BAM (Boot Assist Module) is a block of read-only memory that is programmed once by Freescale and is identical for all MPC5634M MCUs. The BAM program is executed every time the MCU is powered-on or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal flash memory
- Serial boot loading (A program is downloaded into RAM via eSCI or the FlexCAN and then executed)
- Booting from external memory on calibration bus

The BAM also reads the reset configuration half word (RCHW) from internal flash memory and configures the MPC5634M hardware accordingly. The BAM provides the following features:

- Sets up MMU to cover all resources and mapping all physical address to logical addresses with minimum address translation

  - SCK to PCS delay
  - Delay between frames
  - Programmable serial frame size of 4 to 16 bits, expandable with software control
  - Continuously held chip select capability
- 6 Peripheral Chip Selects, expandable to 64 with external demultiplexer
- Deglitching support for up to 32 Peripheral Chip Selects with external demultiplexer
- DMA support for adding entries to TX FIFO and removing entries from RX FIFO:
  - TX FIFO is not full (TFFF)
  - RX FIFO is not empty (RFDF)
- 6 Interrupt conditions:
  - End of queue reached (EOQF)
  - TX FIFO is not full (TFFF)
  - Transfer of current frame complete (TCF)
  - Attempt to transmit with an empty Transmit FIFO (TFUF)
  - RX FIFO is not empty (RFDF)
  - FIFO Underrun (slave only and SPI mode, the slave is asked to transfer data when the TxFIFO is empty)
  - FIFO Overrun (serial frame received while RX FIFO is full)
- Modified transfer formats for communication with slower peripheral devices
- Continuous Serial Communications Clock (SCK)
- Power savings via support for Stop Mode
- Enhanced DSI logic to implement a 32-bit Timed Serial Bus (TSB) configuration, supporting the Microsecond Channel downstream frame format

The DSPIs also support these features unique to the DSI and CSI configurations:

- 2 sources of the serialized data:
  - eTPU_A and eMIOS output channels
  - Memory-mapped register in the DSPI
- Destinations for the deserialized data:
  - eTPU_A and eMIOS input channels
  - SIU External Interrupt Request inputs
  - Memory-mapped register in the DSPI
- Deserialized data is provided as Parallel Output signals and as bits in a memory-mapped register
- Transfer initiation conditions:
  - Continuous
  - Edge sensitive hardware trigger
  - Change in data
- Pin serialization/deserialization with interleaved SPI frames for control and diagnostics
- Continuous serial communications clock
- Support for parallel and serial chaining of up to four DSPI blocks

2.2.16 eSCI

The enhanced serial communications interface (eSCI) allows asynchronous serial communications with peripheral devices and other MCUs. It includes special support to interface to Local Interconnect Network (LIN) slave devices. The eSCI block provides the following features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format

- 13-bit baud rate selection
- Programmable 8-bit or 9-bit, data format
- Programmable 12-bit or 13-bit data format for Timed Serial Bus (TSB) configuration to support the Microsecond Channel upstream
- Automatic parity generation
- LIN support
  - Autonomous transmission of entire frames
  - Configurable to support all revisions of the LIN standard
  - Automatic parity bit generation
  - Double stop bit after bit error
  - 10- or 13-bit break support
- Separately enabled transmitter and receiver
- Programmable transmitter output parity
- 2 receiver wake up methods:
  - Idle line wake-up
  - Address mark wake-up
- Interrupt-driven operation with flags
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection
- DMA support for both transmit and receive data
  - Global error bit stored with receive data in system RAM to allow post processing of errors

2.2.17 FlexCAN

The MPC5634M MCU contains two controller area network (FlexCAN) blocks. The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. FlexCAN module ‘A’ contains 64 message buffers (MB); FlexCAN module ‘C’ contains 32 message buffers.

The FlexCAN module provides the following features:

- Based on and including all existing features of the Freescale TouCAN module
- Full Implementation of the CAN protocol specification, Version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - Zero to eight bytes data length
  - Programmable bit rate up to 1 Mbit/s
- Content-related addressing
- 64 / 32 message buffers of zero to eight bytes data length
- Individual Rx Mask Register per message buffer
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Includes 1056 / 544 bytes of embedded memory for message buffer storage
- Includes a 256-byte and a 128-byte memories for storing individual Rx mask registers
- Full featured Rx FIFO with storage capacity for six frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against 8 extended, 16 standard or 32 partial (8 bits) IDs, with individual masking capability

- Independent interrupt source for each channel
- Counter can be stopped in debug mode

2.2.19 Software Watchdog Timer (SWT)

The Software Watchdog Timer (SWT) is a second watchdog module to complement the standard Power Architecture watchdog integrated in the CPU core. The SWT is a 32-bit modulus counter, clocked by the system clock or the crystal clock, that can provide a system reset or interrupt request when the correct software key is not written within the required time window.

The following features are implemented:

- 32-bit modulus counter
- Clocked by system clock or crystal clock
- Optional programmable watchdog window mode
- Can optionally cause system reset or interrupt request on timeout
- Reset by writing a software key to memory mapped register
- Enabled out of reset
- Configuration is protected by a software key or a write-once register

2.2.20 Debug features

2.2.20.1 Nexus port controller

The NPC (Nexus Port Controller) block provides real-time development support capabilities for the MPC5634MPower Architecture-based MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NPC block is an integration of several individual Nexus blocks that are selected to provide the development support interface for MPC5634M. The NPC block interfaces to the host processor (e200z335), eTPU, and internal buses to provide development support as per the IEEE-ISTO 5001-2003 standard. The development support provided includes program trace and run-time access to the MCUs internal memory map and access to the Power Architecture and eTPU internal registers during halt. The Nexus interface also supports a JTAG only mode using only the JTAG pins. MPC5634Min the production 144 LQFP supports a 3.3 V reduced (4-bit wide) Auxiliary port. These Nexus port pins can also be used as 5 V I/O signals to increase usable I/O count of the device. When using this Nexus port as IO, Nexus trace is still possible using VertiCal calibration. In the VertiCal calibration package, the full 12-bit Auxiliary port is available.

NOTE

In the VertiCal package, the full Nexus Auxiliary port shares balls with the addresses of the calibration bus. Therefore multiplexed address/data bus mode must be used for the calibration bus when using full width Nexus trace in VertiCal assembly.

The following features are implemented:

- 5-pin JTAG port (JCOMP, TDI, TDO, TMS, and TCK)
  - Always available in production package
  - Supports both JTAG Boundary Scan and debug modes
  - 3.3 V interface
  - Supports Nexus class 1 features
  - Supports Nexus class 3 read/write feature
- 9-pin Reduced Port interface in 144 LQFP production package
  - Alternate function as IO
  - 5 V (in GPIO or alternate function mode), 3.3 V (in Nexus mode) interface

standard. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE 1149.1-2001 standard and supports the following features:

- IEEE 1149.1-2001 Test Access Port (TAP) interface 4 pins (TDI, TMS, TCK, and TDO)
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD, HIGHZ, CLAMP
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC
  - ACCESS_AUX_TAP_ONCE
  - ACCESS_AUX_TAP_eTPU
  - ACCESS_CENSOR
- 3 test data registers to support JTAG Boundary Scan mode
  - Bypass register
  - Boundary scan register
  - Device identification register
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- Censorship Inhibit Register
  - 64-bit Censorship password register
  - If the external tool writes a 64-bit password that matches the Serial Boot password stored in the internal flash shadow row, Censorship is disabled until the next system reset.

2.3 MPC5634M series architecture

2.3.1 Block diagram

Figure 1 shows a top-level block diagram of the MPC5634M series.

Table 1. MPC5634M series block summary (continued)

Block	Function
DMA (direct memory access)	Performs complex data movements with minimal intervention from the core
DSPI (deserial serial peripheral interface)	Provides a synchronous serial interface for communication with external devices
eMIOS (enhanced modular input-output system)	Provides the functionality to generate or measure events
eQADC (enhanced queued analog-to-digital converter)	Provides accurate and fast conversions for a wide range of applications
eSCI (serial communication interface)	Allows asynchronous serial communications with peripheral devices and other microcontroller units
eTPU (enhanced time processor unit)	Processes real-time input events, performs output waveform generation, and accesses shared data without host intervention
FlexCAN (controller area network)	Supports the standard CAN communications protocol
FMPLL (frequency-modulated phase-locked loop)	Generates high-speed system clocks and supports the programmable frequency modulation of these clocks
INTC (interrupt controller)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
NPC (Nexus Port Controller)	Provides real-time development support capabilities in compliance with the IEEE-ISTO 5001-2003 standard
PIT (peripheral interrupt timer)	Produces periodic interrupts and triggers
Temperature sensor	Provides the temperature of the device as an analog value
SWT (Software Watchdog Timer)	Provides protection from runaway code
STM (System Timer Module)	Timer providing a set of output compare events to support AutoSAR and operating system tasks

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPB GA
CAL_$\overline{CS}$[3][11] CAL_ADDR[11]	Calibration Chip Selects Calibration Address Bus	PCR[339]	11 10	O O	VDDE12 Fast	O / High	CAL_$\overline{CS}$ / High		—	—	—
CAL_DATA[0:9][11]	Calibration Data Bus	PCR[341]		I/O	VDDE12 Fast	– / Up	– / Up		—	—	—
CAL_DATA[10:15][11]	Calibration Data Bus	PCR[341]		I/O	VDDE12 Fast	– / Up	– / Up		—	—	—
CAL_$\overline{OE}$[11]	Calibration Output Enable	PCR[342]	—	O	VDDE12 Fast	O / High	CAL_$\overline{OE}$ / High		—	—	—
CAL_RD_$\overline{WR}$[11]	Calibration Read/Write	PCR[342]	—	O	VDDE12 Fast	O / High	CAL_RD_$\overline{WR}$ /High		—	—	—
CAL_$\overline{TS}$_ALE[11]	Calibration Transfer Start Address Latch Enable	PCR[343]	TS=0b1 ALE=0b0	O O	VDDE12 Fast	O / High	CAL_$\overline{TS}$ / High		—	—	—
CAL_$\overline{WE}$_BE[0:1][11]	Calibration Write Enable Byte Enable	PCR[342]	—	O	VDDE12 Fast	O / High	CAL_$\overline{WE}$ / High		—	—	—
NEXUS[20]											
$\overline{EVTI}$[21] eTPU_A[2] GPIO[231]	Nexus Event In eTPU A Ch. GPIO	PCR[231]	01 10 00	I O I/O	VDDEH7 Multi-V	– / –	– / –		103	126	P10
$\overline{EVTO}$ [21] eTPU_A[4] GPIO[227]	Nexus Event Out eTPU A Ch. GPIO	PCR[227]	01[22] 10 00	O O I/O	VDDEH7 Multi-V	I / Up	I / Up		106	129	T10
MCKO[21] GPIO[219]	Nexus Msg Clock Out GPIO	PCR[219]	N/A[22] 00	O I/O	VDDEH7 Multi-V	– / –	– / –		99	122	T6
MDO[0][21] eTPU_A[13] GPIO[220]	Nexus Msg Data Out eTPU A Ch. GPIO	PCR[220]	01 10 00	O O I/O	VDDEH7 Multi-V	– / –	– / –		110	135	T11
MDO[1][21] eTPU_A[19] GPIO[221]	Nexus Msg Data Out eTPU A Ch. GPIO	PCR[221]	01[22] 10 00	O O I/O	VDDEH7 Multi-V	– / –	– / –		111	136	N11
MDO[2][21] eTPU_A[21] GPIO[222]	Nexus Msg Data Out eTPU A Ch. GPIO	PCR[222]	01[22] 10 00	O O I/O	VDDEH7 Multi-V	– / –	– / –		112	137	P11

[39] VDDEH6A and VDDEH6B are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[40] If using JTAG or Nexus, the I/O segment that contains the JTAG and Nexus pins must be powered by a 5 V supply. The 3.3 V Nexus/JTAG signals are derived from the 5 volt power supply.

[41] In the calibration package this signal is named VDDE12.

Table 3. Pad types

Pad Type	Name	Supply Voltage
Slow	pad_ssr_hv	3.0 V – 5.25 V
Medium	pad_msr_hv	3.0 V – 5.25 V
Fast	pad_fc	3.0 V – 3.6 V
MultiV	pad_multv_hv	3.0 V – 5.25 V (high swing mode) 4.5 V – 5.25 V (low swing mode)
Analog	pad_ae_hv	0.0 – 5.25 V
LVDS	pad_lo_lv	—

Table 16. Network 1 component values

Component	Symbol	Minimum	Typical	Maximum	Units	Comment
Transistor emitter bypass capacitance	C_E	4 x 2.35	4 x 4.7	4 x 6.35	µF	X7R, -50%/+35%
		1 x 5	1 x 10	1 x 13.5	µF	X7R, -50%/+35%
	R_{ESR}	5		50	mΩ	Equivalent ESR of C_E capacitors
MCU decoupling capacitor	C_D	4 x 50	4 x 100	4 x 135	nF	X7R, -50%/+35%
Base "snubber" capacitor	C_B	1.1	2.2	2.97	µF	X7R, -50%/+35%
Base "snubber" resistor	R_B	6.12	6.8	7.48	Ω	±10%
Emitter resistor	R_E	0	0	0	Ω	Not required (short)

Table 17. Network 2 component values

Component	Symbol	Minimum	Typical	Maximum	Units	Comment
Transistor emitter bypass capacitance	C_E	3 x 2.35	3 x 4.7	3 x 6.35	µF	X7R, -50%/+35%
		1 x 5	1 x 10	1 x 13.5	µF	X7R, -50%/+35%
	R_{ESR}	5		50	mΩ	Equivalent ESR of C_E capacitors
MCU decoupling capacitor	C_D	4 x 50	4 x 100	4 x 135	nF	X7R, -50%/+35%
Base "snubber" capacitor	C_B	1.1	2.2	2.97	µF	X7R, -50%/+35%
Base "snubber" resistor	R_B	9	10	11	Ω	±10%
Emitter resistor	R_E	0.252	0.280	0.308	Ω	Not required (short)

The following component configuration is acceptable when using the BCP68 transistor, however, is not recommended for new designs. Either option 1 or option 2 should be used for new designs. This option should not be used with the NJD2873 transistor.

Table 18. Network 3 component values

Component	Symbol	Minimum	Typical	Maximum	Units	Comment
Transistor emitter bypass capacitance	C_E	4 x 3.4	4 x 6.8	4 x 9.18	µF	X7R, -50%/+35%
	R_{ESR}	5		50	mΩ	Equivalent ESR of C_E capacitors
MCU decoupling capacitor	C_D	4 x 110	4 x 220	4 x 297	nF	X7R, -50%/+35%
Base "snubber" capacitor	C_B	1.1	2.2	2.97	µF	X7R, -50%/+35%
Base "snubber" resistor	R_B	13.5	15	16.5	Ω	±10%
Emitter resistor	R_E	0	0	0	Ω	Not required (short)

4.6.2 Recommended power transistors

The following NPN transistors are recommended for use with the on-chip voltage regulator controller: ON Semiconductor™ BCP68T1 or NJD2873 as well as Philips Semiconductor™ BCP68. The collector of the external transistor is preferably connected to the same voltage supply source as the output stage of the regulator.

Table 19. Recommended operating characteristics

Symbol	Parameter	Value	Unit
h_{FE} (β)	DC current gain (Beta)	60 – 550	—
P_D	Absolute minimum power dissipation	>1.0 (1.5 preferred)	W
I_{CMaxDC}	Minimum peak collector current	1.0	A
VCE_{SAT}	Collector-to-emitter saturation voltage	200–600[1]	mV
V_{BE}	Base-to-emitter voltage	0.4–1.0	V

[1] Adjust resistor at bipolar transistor collector for 3.3 V/5.0 V to avoid VCE < VCE_{SAT}

4.7 Power up/down sequencing

There is no power sequencing required among power sources during power up and power down, in order to operate within specification but use of the following sequence is strongly recommended when the internal regulator is bypassed:

5 V → 3.3 V and 1.2 V

This is also the normal sequence when the internal regulator is enabled.

Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies according to table Table 20 for all pins with fast pads and Table 21 for all pins with medium, slow and multi-voltage pads.[1]

Table 20. Power sequence pin states for fast pads

V_{DDE}	V_{RC33}	V_{DD}	Fast (pad_fc)
LOW	X	X	LOW
V_{DDE}	LOW	X	HIGH
V_{DDE}	V_{RC33}	LOW	HIGH IMPEDANCE
V_{DDE}	V_{RC33}	V_{DD}	FUNCTIONAL

Table 21. Power sequence pin states for medium, slow and multi-voltage pads

V_{DDEH}	V_{DD}	Medium (pad_msr_hv) Slow (pad_ssr_hv) Multi-voltage (pad_multv_hv)
LOW	X	LOW
V_{DDEH}	LOW	HIGH IMPEDANCE
V_{DDEH}	V_{DD}	FUNCTIONAL

1.If an external 3.3V external regulator is used to supply current to the 1.2V pass transistor and this supply also supplies current for the other 3.3V supplies, then the 5V supply must always be greater than or equal to the external 3.3V supply.

[8] V_{FLASH} is only available in the calibration package.

[9] Regulator is functional, with derated performance, with supply voltage down to 4.0 V.

[10] Multi-voltage pads (type pad_multv_hv) must be supplied with a power supply between 4.75 V and 5.25 V.

[11] The slew rate (SRC) setting must be 0b11 when in low-swing mode.

[12] While in low-swing mode there are no restrictions in transitioning to high-swing mode.

[13] Pin in low-swing mode can accept a 5 V input.

[14] Values are pending characterization.

[15] Pin in low-swing mode can accept a 5 V input.

[16] Characterization based capability:

IOH_S = {6, 11.6} mA and IOL_S = {9.2, 17.7} mA for {slow, medium} I/O with VDDEH=4.5 V;
IOH_S = {2.8, 5.4} mA and IOL_S = {4.2, 8.1} mA for {slow, medium} I/O with VDDEH=3.0 V

[17] Characterization based capability:

IOH_F = {12, 20, 30, 40} mA and IOL_F = {24, 40, 50, 65} mA for {00, 01,10, 11} drive mode with VDDE=3.0 V;
IOH_F = {7, 13, 18, 25} mA and IOL_F = {18, 30, 35, 50} mA for {00, 01, 10, 11} drive mode with VDDE=2.25 V;
IOH_F = {3, 7, 10, 15} mA and IOL_F = {12, 20, 27, 35} mA for {00, 01, 10, 11} drive mode with VDDE=1.62 V

[18] All VOL/VOH values 100% tested with ± 2 mA load.

[19] Run mode as follows:

System clock = 40/60/80 MHz + FM 2%
Code executed from flash memory
ADC0 at 16 MHz with DMA enabled
ADC1 at 8 MHz
eMIOS pads toggle in PWM mode with a rate between 100 kHz and 500 kHz
eTPU pads toggle in PWM mode with a rate between 10 kHz and 500 kHz
CAN configured for a bit rate of 500 kHz
DSPI configured in master mode with a bit rate of 2 MHz
eSCI transmission configured with a bit rate of 100 kHz

[20] Bypass mode, system clock at 1 MHz (using system clock divider), PLL shut down, CPU running simple executive code, 4 x ADC conversion every 10 ms, 2 × PWM channels at 1 kHz, all other modules stopped.

[21] Bypass mode, system clock at 1 MHz (using system clock divider), CPU stopped, PIT running, all other modules stopped.

[22] When using the internal regulator only, a bypass capacitor should be connected to this pin. External circuits should not be powered by the internal regulator. The internal regulator can be used as a reference for an external debugger.

[23] Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. See Table 23 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.

[24] Absolute value of current, measured at V_{IL} and V_{IH}.

[25] Weak pull up/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to pad types: fast (pad_fc).

[26] Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 ^{o}C, in the ambient temperature range of 50 to 125 ^{o}C. Applies to pad types: pad_a and pad_ae.

[27] Applies to CLKOUT, external bus pins, and Nexus pins.

[28] Applies to the FCK, SDI, SDO, and $\overline{SDS}$ pins.

[29] This programmable option applies only to eQADC differential input channels and is used for biasing and sensor diagnostics.

[30] When the pull-up and pull-down of the same nominal 200 KΩ or 100 KΩ value are both enabled, assuming no interference from external devices, the resulting pad voltage will be 0.5*V_{DDE} ± 2.5%

Table 26. DSPI LVDS pad specification [1, 2] (continued)

12	Diff Skew ltphla-tplhbl or ltplhb-tphlal	T_{SKEW}	CC	D				0.5	ns
Termination									
13	Trans. Line (differential Zo)		CC	D		95	100	105	Ω
14	Temperature		CC	D		–40		150	°C

1 These are typical values that are estimated from simulation.

2 These specifications are subject to change per device characterization.

3 Preliminary target values. Actual specifications to be determined.

4.10 Oscillator and PLLMRFM electrical characteristics

Table 27. PLLMRFM electrical specifications[1]

(V_{DDPLL} =1.14 V to 1.32 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H)

Symbol		C	Parameter		Conditions	Value		Unit
						min	max	
$f_{ref\_crystal}$ f_{ref_ext}	CC	D	PLL reference frequency range[2]		Crystal reference	4	20	MHz
		C			External reference	4	80	
f_{pll_in}	CC	P	Phase detector input frequency range (after pre-divider)		—	4	16	MHz
f_{vco}	CC	P	VCO frequency range[3]		—	256	512	MHz
f_{sys}	CC	C	On-chip PLL frequency[2]		—	16	80	MHz
f_{sys}	CC	T	System frequency in bypass mode[4]		Crystal reference	4	20	MHz
		P			External reference	0	80	
t_{CYC}	CC	D	System clock period		—	—	1 / f_{sys}	ns
f_{LORL} f_{LORH}	CC	D	Loss of reference frequency window[5]		Lower limit	1.6	3.7	MHz
		D			Upper limit	24	56	
f_{SCM}	CC	P	Self-clocked mode frequency [6,7]		—	1.2	75	MHz
C_{JITTER}	CC	T	CLKOUT period jitter[8,9,10,11]	Peak-to-peak (clock edge to clock edge)	f_{SYS} maximum	–5	5	% f_{CLKOUT}
		T		Long-term jitter (avg. over 2 ms interval)		–6	6	ns
t_{cst}	CC	T	Crystal start-up time [12, 13]		—	—	10	ms
V_{IHEXT}	CC	T	EXTAL input high voltage		Crystal Mode[14], 0.8 ≤ Vxtal ≤ 1.5V[15]	Vxtal + 0.4	—	V
		T			External Reference[14, 16]	V_{RC33}/2 + 0.4	V_{RC33}	

[4] Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

[5] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA} + 0.5$ V and $V_{NEGCLAMP} = – 0.3$ V, then use the larger of the calculated values.

[6] Condition applies to two adjacent pins at injection limits.

[7] Performance expected with production silicon.

[8] All channels have same 10 kΩ < Rs < 100 kΩ; Channel under test has Rs=10 kΩ; I_{INJ}=I_{INJMAX},I_{INJMIN}.

[9] TUE is tested by averaging 10 samples.

[10] TUE is tested by averaging three samples.

[11] These values can be significantly improved by using three samples of averaging. Input frequency of 1 kHz was used as the reference for the Signal to Noise Ratio.

[12] Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed by as indicated.

[13] At $V_{RH} – V_{RL} = 5.12$ V, one LSB = 1.25 mV.

[14] Guaranteed 10-bit monotonicity.

[15] Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

4.13 Platform flash controller electrical characteristics

Table 30. APC, RWSC, WWSC settings vs. frequency of operation[1]

Target Max Frequency (MHz)	APC[2]	RWSC[2]	WWSC
21[3]	000	000	01
41[3]	001	001	01
62[3]	010	010	01
82[3]	011	011	01
All	111	111	111

1 Illegal combinations exist, all entries must be taken from the same row

2 APC must be equal to RWSC

3 Maximum Frequency includes FM modulation

4.14 Flash memory electrical characteristics

Table 31. Program and erase specifications

Symbol		Parameter	Min Value	Typical Value[1]	Initial Max[2]	Max[3]	Unit
$T_{dwprogram}$	P	Double Word (64 bits) Program Time[4]	—	22	50	500	µs
$T_{16kpperase}$	P	16 KB Block Pre-program and Erase Time	—	300	500	5000	ms
$T_{32kpperase}$	P	32 KB Block Pre-program and Erase Time	—	400	600	5000	ms
$T_{64kpperase}$	P	64 KB Block Pre-program and Erase Time	—	600	900	5000	ms
$T_{128kpperase}$	P	128 KB Block Pre-program and Erase Time	—	800	1300	7500	ms

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program & erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

5.1.2 176 LQFP

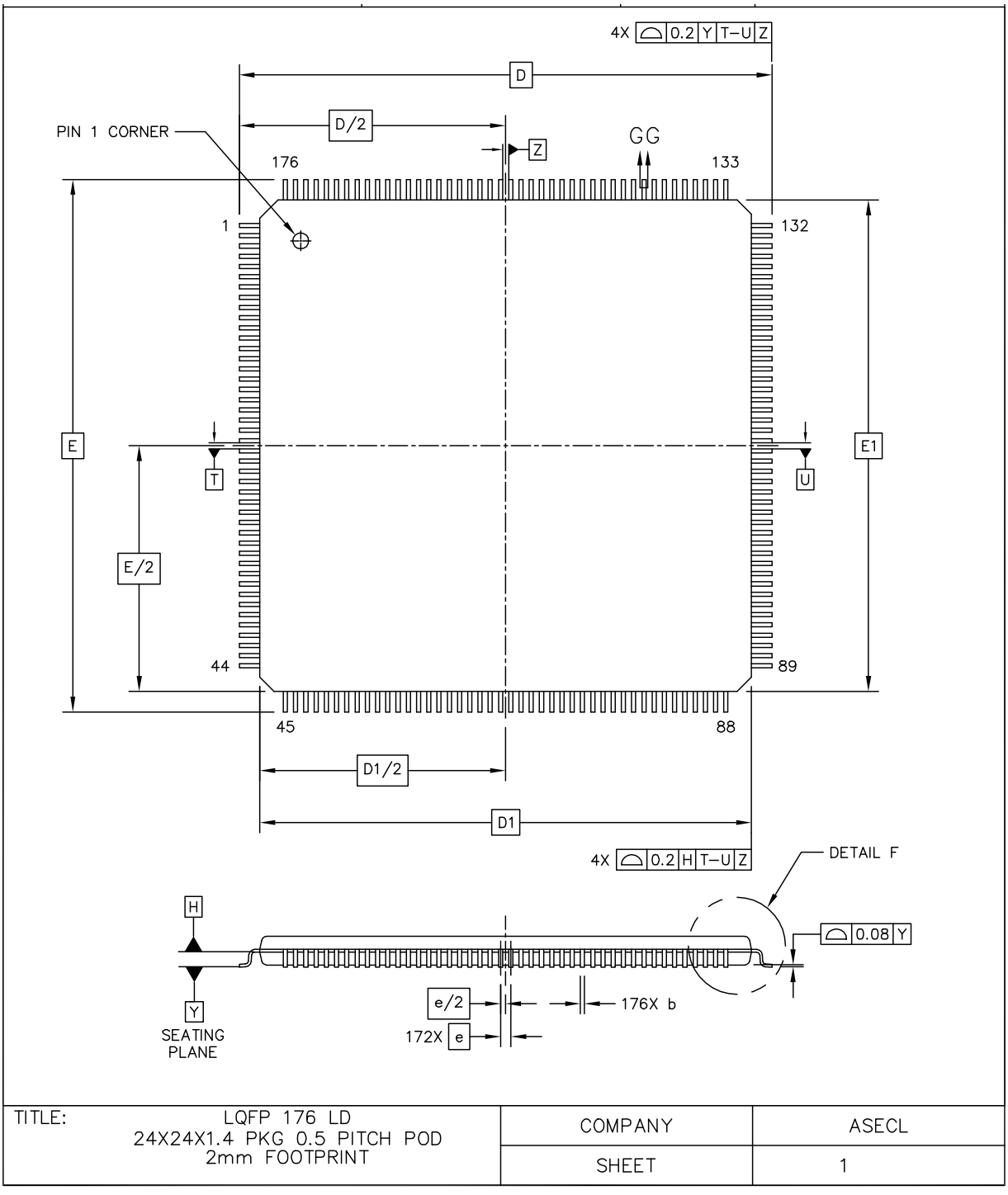
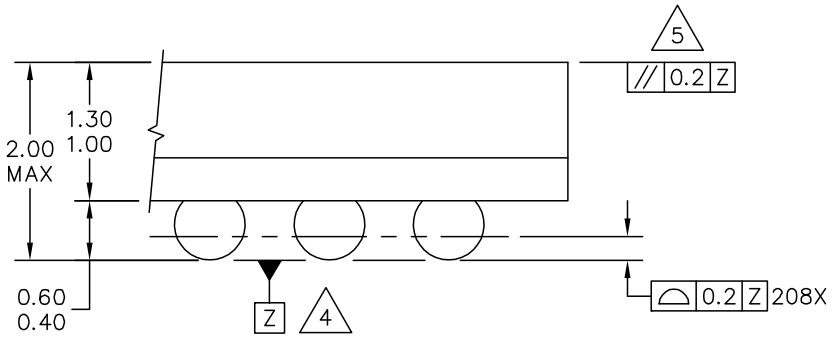


Figure 33. 176 LQFP package mechanical drawing (part 1)

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ARS23882W
		PAGE: 1159A
	DO NOT SCALE THIS DRAWING	REV: D



DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH	CASE NUMBER: 1159A–01	
	STANDARD: JEDEC MO–151 AAF–1	
	PACKAGE CODE: 5253	SHEET: 2 OF 3

Figure 37. 208 MAPBGA package mechanical drawing (part 2)

6 Ordering information

Table 42 shows the orderable part numbers for the MPC5634M series.

Table 42. Orderable part number summary

Part Number	Flash/SRAM (Kbytes)	Package	Speed (MHz)
SPC5632MF2MLQ60	768 / 48	144 LQFP Pb-free	60
SPC5632MF2MLQ40	768 / 48	144 LQFP Pb-free	40
SPC5633MF2MMG80	1024 / 64	208 MAPBGA Pb-free	80
SPC5633MF2MLU80	1024 / 64	176 LQFP Pb-free	80
SPC5633MF2MLQ80	1024 / 64	144 LQFP Pb-free	80
SPC5633MF2MMG60	1024 / 64	208 MAPBGA Pb-free	60
SPC5633MF2MLU60	1024 / 64	176 LQFP Pb-free	60
SPC5633MF2MLQ60	1024 / 64	144 LQFP Pb-free	60
SPC5633MF2MLQ40	1024 / 64	144 LQFP Pb-free	40
SPC5634MF2MMG80	1536 / 94	208 MAPBGA Pb-free	80
SPC5634MF2MLU80	1536 / 94	176 LQFP Pb-free	80
SPC5634MF2MLQ80	1536 / 94	144 LQFP Pb-free	80
SPC5634MF2MMG60	1536 / 94	208 MAPBGA Pb-free	60
SPC5634MF2MLU60	1536 / 94	176 LQFP Pb-free	60
SPC5634MF2MLQ60	1536 / 94	144 LQFP Pb-free	60
SPC563M60L3CPBY			
SPC563M60L3CPAY			

Table 43. Revision history (continued)

Revision	Date	Description of Changes
Rev. 5	04/2010	Updates to features list: • MMU is 16-entry (previously noted as 8-entry) • ECSM features include single-bit error correction reporting • eTPU2 is object code compatible with previous eTPU versions Updates to feature details: • Programming feature: eTPU2 channel flags can be tested Pinout/ballmap changes: 144 pin LQFP package: • Pin 46 is now VDDEH1B (was VDDEH4A) • Pin 61 is now VDDEH6A (was VDDEH4B) 176 pin LQFP package (1.5M devices) • Pin 55 is now VDDEH1B (was VDDEH4A) • Pin 74 is now VDDEH6A (was VDDEH4B) 176 pin LQFP package (1.5M devices) • Pin 55 is now VDDEH1B (was VDDEH4A) • Pin 74 is now VDDEH6A (was VDDEH4B) 208 ball BGA package (all devices) Ball N9 changed to VDDEH1/6 (was VDDEH6). In a future revision of the device this may be changed to NC (no connect). Changes to calibration ball names on devices with 1 MB flash memory: • CAL_MDO0 changed to ALT_MDO0 • CAL_MDO1 changed to ALT_MDO1 • CAL_MDO2 changed to ALT_MDO2 • CAL_MDO3 changed to ALT_MDO3 • CAL_MSEO0 changed to ALT_MSEO0 • CAL_MSEO1 changed to ALT_MSEO1 • CAL_EVTI changed to ALT_EVTI • CAL_EVTO changed to ALT_EVTO • CAL_MCKO changed to ALT_MCKO Power/ground segment changes: • The following pins are on VDDE7 I/O segment only on the 208-ball BGA package: ALT_MDO[0:3], ALT_MSEO[0:1], ALT_EVTI, ALT_EVTO, ALT_MCKO. • Power segments VDDEH4, VDDEH4A and VDDEH4B have been removed. CLKOUT power segment is VDDE5 (was VDDE12) Thermal characteristics for 176-pin LQFP updated (all parameter values)