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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	94K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5634mf2mlu80

- Advanced error detection, and optional parity generation and detection
- Word length programmable as 8, 9, 12 or 13 bits
- Separately enabled transmitter and receiver
- LIN support
- DMA support
- Interrupt request support
- Programmable clock source: system clock or oscillator clock
- Support Microsecond Channel (Timed Serial Bus - TSB) upstream Version 1.0

- Two FlexCAN
  - One with 32 message buffers; the second with 64 message buffers
  - Full implementation of the CAN protocol specification, Version 2.0B
  - Based on and including all existing features of the Freescale TouCAN module
  - Programmable acceptance filters
  - Short latency time for high priority transmit messages
  - Arbitration scheme according to message ID or message buffer number
  - Listen only mode capabilities
  - Programmable clock source: system clock or oscillator clock
  - Message buffers may be configured as mailboxes or as FIFO
- Nexus port controller (NPC)
  - Per IEEE-ISTO 5001-2003
  - Real time development support for Power Architecture core and eTPU engine through Nexus class 2/1
  - Read and write access (Nexus class 3 feature that is supported on this device)
    - Run-time access of entire memory map
    - Calibration
  - Support for data value breakpoints / watchpoints
    - Run-time access of entire memory map
    - Calibration

      Table constants calibrated using MMU and internal and external RAM

      Scalar constants calibrated using cache line locking
  - Configured via the IEEE 1149.1 (JTAG) port
- IEEE 1149.1 JTAG controller (JTAGC)
  - IEEE 1149.1-2001 Test Access Port (TAP) interface
  - 5-bit instruction register that supports IEEE 1149.1-2001 defined instructions
  - 5-bit instruction register that supports additional public instructions
  - Three test data registers: a bypass register, a boundary scan register, and a device identification register
  - Censorship disable register. By writing the 64-bit serial boot password to this register, Censorship may be disabled until the next reset
  - TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- On-chip Voltage Regulator for single 5 V supply operation
  - On-chip regulator 5 V to 3.3 V for internal supplies
  - On-chip regulator controller 5 V to 1.2 V (with external bypass transistor) for core logic
- Low-power modes
  - SLOW Mode. Allows device to be run at very low speed (approximately 1 MHz), with modules (including the PLL) selectively disabled in software
  - STOP Mode. System clock stopped to all modules including the CPU. Wake-up timer used to restart the system clock after a predetermined time

- Channel transfers can be suspended by a higher priority channel

2.2.4 Interrupt controller

The INTC (interrupt controller) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems. The INTC allows interrupt request servicing from up to 191 peripheral interrupt request sources, plus 165 sources reserved for compatibility with other family members).

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

Multiple processors can assert interrupt requests to each other through software setable interrupt requests. These same software setable interrupt requests also can be used to break the work involved in servicing an interrupt request into a high priority portion and a low priority portion. The high priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software setable interrupt request to finish the servicing in a lower priority ISR. Therefore these software setable interrupt requests can be used instead of the peripheral ISR scheduling a task through the RTOS.

The INTC provides the following features:

- 356 peripheral interrupt request sources
- 8 software setable interrupt request sources
- 9-bit vector addresses
- Unique vector for each interrupt request source
- Hardware connection to processor or read from register
- Each interrupt source can be programmed to one of 16 priorities
- Preemptive prioritized interrupt requests to processor
- ISR at a higher priority preempts executing ISRs or tasks at lower priorities
- Automatic pushing or popping of preempted priority to or from a LIFO
- Ability to modify the ISR or task priority to implement the priority ceiling protocol for accessing shared resources
- Low latency—three clocks from receipt of interrupt request from peripheral to interrupt request to processor

This device also includes a non-maskable interrupt (NMI) pin that bypasses the INTC and multiplexing logic.

2.2.5 FMPLL

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 20 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable. The PLL has the following major features:

- Input clock frequency from 4 MHz to 20 MHz
- Voltage controlled oscillator (VCO) range from 256 MHz to 512 MHz, resulting in system clock frequencies from 16 MHz to 80 MHz with granularity of 4 MHz or better
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- 3 modes of operation
  - Bypass mode with PLL off
  - Bypass mode with PLL running (default mode out of reset)
  - PLL normal mode

intervention. Consequently, for each timer event, the host CPU setup and service times are minimized or eliminated. A powerful timer subsystem is formed by combining the eTPU2 with its own instruction and data RAM. High-level assembler/compiler and documentation allows customers to develop their own functions on the eTPU2.

The eTPU2 includes these distinctive features:

- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.
- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.
- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.
- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.
- 32 channels, each channel is associated with one input and one output signal
  - Enhanced input digital filters on the input pins for improved noise immunity.
  - Identical, orthogonal channels: each channel can perform any time function. Each time function can be assigned to more than one channel at a given time, so each signal can have any functionality.
  - Each channel has an event mechanism which supports single and double action functionality in various combinations. It includes two 24-bit capture registers, two 24-bit match registers, 24-bit greater-equal and equal-only comparators
  - Input and output signal states visible from the host
- 2 independent 24-bit time bases for channel synchronization:
  - First time base clocked by system clock with programmable prescale division from 2 to 512 (in steps of 2), or by output of second time base prescaler
  - Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
  - Both time bases can be exported to the eMIOS timer module
  - Both time bases visible from the host
- Event-triggered microengine:
  - Fixed-length instruction execution in two-system-clock microcycle
  - 14 KB of code memory (SCM)
  - 3 KB of parameter (data) RAM (SPRAM)
  - Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations

results to the result FIFOs. This allows the ADCs to sample the sensor at a rate high enough to avoid aliasing of out-of-band noise; while providing a reduced sample rate output to minimize the amount DSP processing bandwidth required to fully process the digitized waveform.

The eQADC provides the following features:

- Dual on-chip ADCs
  - 2 × 12-bit ADC resolution
  - Programmable resolution for increased conversion speed (12 bit, 10 bit, 8 bit)
    - 12-bit conversion time – 1 µs (1M sample/sec)
    - 10-bit conversion time – 867 ns (1.2M sample/second)
    - 8-bit conversion time – 733 ns (1.4M sample/second)
  - Up to 10-bit accuracy at 500 KSample/s and 9-bit accuracy at 1 MSample/s
  - Differential conversions
  - Single-ended signal range from 0 to 5 V
  - Variable gain amplifiers on differential inputs (×1, ×2, ×4)
  - Sample times of 2 (default), 8, 64 or 128 ADC clock cycles
  - Provides time stamp information when requested
  - Parallel interface to eQADC CFIFOs and RFIFOs
  - Supports both right-justified unsigned and signed formats for conversion results
- Up to 34[1] input channels (accessible by both ADCs)
- 23 additional internal channels for measuring control and monitoring voltages inside the device
  - Including Core voltage, I/O voltage, LVI voltages, etc.
- An internal bandgap reference to allow absolute voltage measurements
- 4 pairs of differential analog input channels
  - Programmable pull-up/pull-down resistors on each differential input for biasing and sensor diagnostic (200 kΩ, 100 kΩ, 5 kΩ)
- Silicon die temperature sensor
  - provides temperature of silicon as an analog value
  - read using an internal ADC analog channel
  - may be read with either ADC
- Decimation Filter
  - Programmable decimation factor (2 to 16)
  - Selectable IIR or FIR filter
  - Up to 4th order IIR or 8th order FIR
  - Programmable coefficients
  - Saturated or non-saturated modes
  - Programmable Rounding (Convergent; Two’s Complement; Truncated)
  - Pre-fill mode to pre-condition the filter before the sample window opens
- Full duplex synchronous serial interface to an external device
  - Free-running clock for use by an external device
  - Supports a 26-bit message length
- Priority based Queues
  - Supports six Queues with fixed priority. When commands of distinct Queues are bound for the same ADC, the higher priority Queue is always served first

1. 176-pin and 208-pin packages have 34 input channels; 144-pin package has 32.

- Independent interrupt source for each channel
- Counter can be stopped in debug mode

2.2.19 Software Watchdog Timer (SWT)

The Software Watchdog Timer (SWT) is a second watchdog module to complement the standard Power Architecture watchdog integrated in the CPU core. The SWT is a 32-bit modulus counter, clocked by the system clock or the crystal clock, that can provide a system reset or interrupt request when the correct software key is not written within the required time window.

The following features are implemented:

- 32-bit modulus counter
- Clocked by system clock or crystal clock
- Optional programmable watchdog window mode
- Can optionally cause system reset or interrupt request on timeout
- Reset by writing a software key to memory mapped register
- Enabled out of reset
- Configuration is protected by a software key or a write-once register

2.2.20 Debug features

2.2.20.1 Nexus port controller

The NPC (Nexus Port Controller) block provides real-time development support capabilities for the MPC5634MPower Architecture-based MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NPC block is an integration of several individual Nexus blocks that are selected to provide the development support interface for MPC5634M. The NPC block interfaces to the host processor (e200z335), eTPU, and internal buses to provide development support as per the IEEE-ISTO 5001-2003 standard. The development support provided includes program trace and run-time access to the MCUs internal memory map and access to the Power Architecture and eTPU internal registers during halt. The Nexus interface also supports a JTAG only mode using only the JTAG pins. MPC5634Min the production 144 LQFP supports a 3.3 V reduced (4-bit wide) Auxiliary port. These Nexus port pins can also be used as 5 V I/O signals to increase usable I/O count of the device. When using this Nexus port as IO, Nexus trace is still possible using VertiCal calibration. In the VertiCal calibration package, the full 12-bit Auxiliary port is available.

NOTE

In the VertiCal package, the full Nexus Auxiliary port shares balls with the addresses of the calibration bus. Therefore multiplexed address/data bus mode must be used for the calibration bus when using full width Nexus trace in VertiCal assembly.

The following features are implemented:

- 5-pin JTAG port (JCOMP, TDI, TDO, TMS, and TCK)
  - Always available in production package
  - Supports both JTAG Boundary Scan and debug modes
  - 3.3 V interface
  - Supports Nexus class 1 features
  - Supports Nexus class 3 read/write feature
- 9-pin Reduced Port interface in 144 LQFP production package
  - Alternate function as IO
  - 5 V (in GPIO or alternate function mode), 3.3 V (in Nexus mode) interface

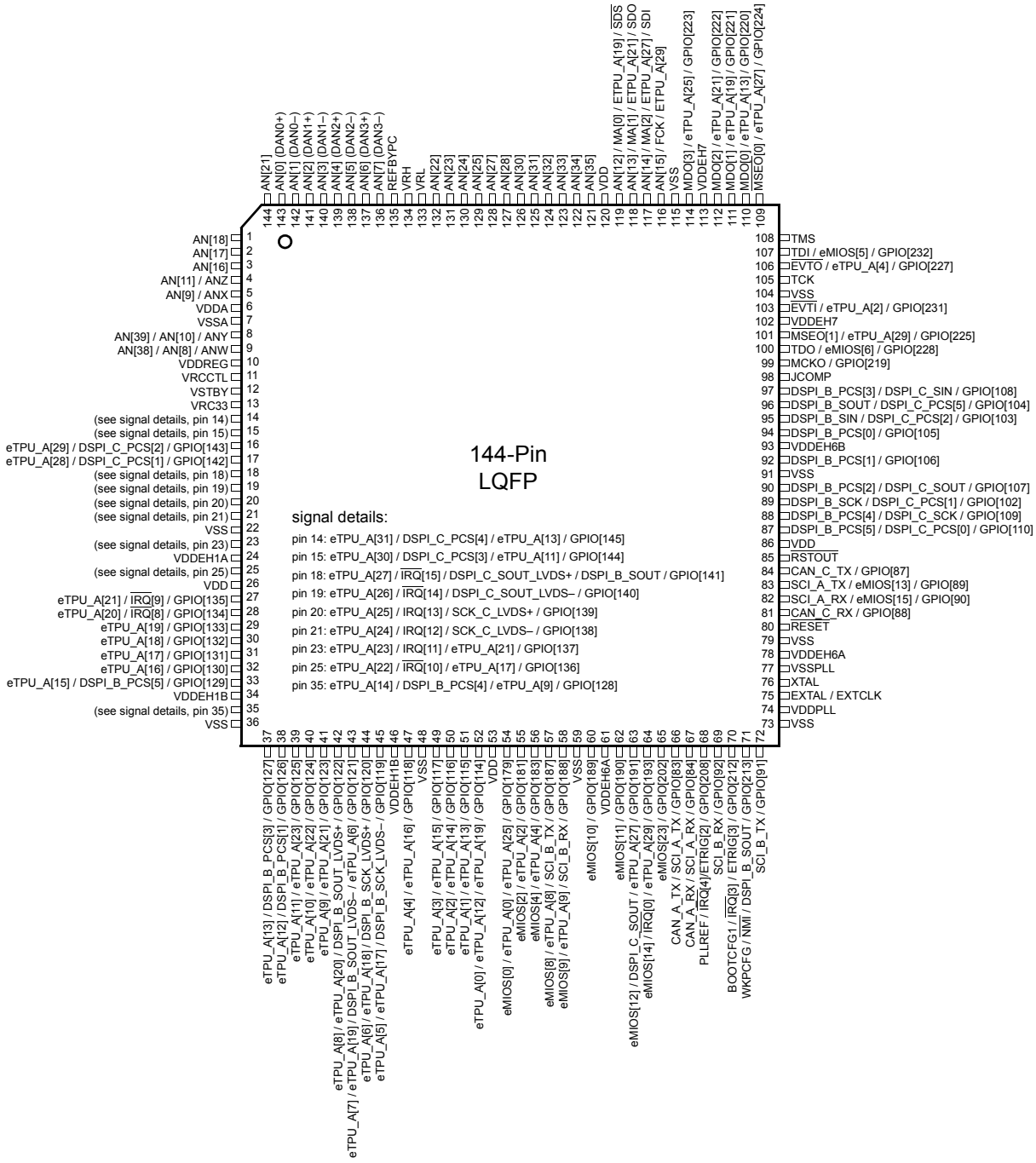


Figure 2. 144-pin LQFP pinout (top view; all 144-pin devices)

3.2 176 LQFP pinout (MPC5634M)

Figure 3 shows the 176-pin LQFP pinout for the MPC5634M (1536 KB flash memory).

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPBGA
MDO[3][21] eTPU_A[25] GPIO[223]	Nexus Msg Data Out eTPU A Ch. GPIO	PCR[223]	01[22] 10 00	O O I/O	VDDEH7 Multi-V	– / –	– / –		114	139	T7
$\overline{\text{MSEO}}$[0][21] eTPU_A[27] GPIO[224]	Nexus Msg Start/End Out eTPU A Ch. GPIO	PCR[224]	01[22] 10 00	O O I/O	VDDEH7 Multi-V	– / –	– / –		109	134	R10
$\overline{\text{MSEO}}$[1][21] eTPU_A[29] GPIO[225]	Nexus Msg Start/End Out eTPU A Ch. GPIO	PCR[225]	01[22] 10 00	O O I/O	VDDEH7 Multi-V	– / –	– / –		101	124	P9
JTAG / TEST											
TCK	JTAG Test Clock Input	—	—	I	VDDEH7 Multi-V	TCK / Down	TCK / Down		105	128	C16
TDI[23] eMIOS[5] GPIO[232]	JTAG Test Data Input eMIOS Ch. GPIO	PCR[232]	01[24] 10 00	I O I/O	VDDEH7 Multi-V	– / –	– / –		107	130	E14
TDO[23] eMIOS[6] GPIO[228]	JTAG Test Data Output eMIOS Ch. GPIO	PCR[228]	01[24] 10 00	O O I/O	VDDEH7 Multi-V	– / –	– / –		100	123	F14
TMS	JTAG Test Mode Select Input	—	—	I	VDDEH7 Multi-V	TMS / Up	TMS / Up		108	131	D14
JCOMP	JTAG TAP Controller Enable	—	—	I	VDDEH7 Multi-V	JCOMP / Down	JCOMP / Down		98	121	F16
CAN											
CAN_A_TX SCI_A_TX GPIO[83]	CAN_A Transmit eSCI_A Transmit GPIO	PCR[83]	01 10 00	O O I/O	VDDEH6a Slow	– / Up	– / Up[25]		66	81	P12
CAN_A_RX SCI_A_RX GPIO[84]	CAN_A Receive eSCI_A Receive GPIO	PCR[84]	01 10 00	I I I/O	VDDEH6a Slow	– / Up	– / Up		67	82	R12
CAN_C_TX GPIO[87]	CAN_C Transmit GPIO	PCR[87]	01 00	O I/O	VDDEH6a Medium	– / Up	– / Up		84	101	K13
CAN_C_RX GPIO[88]	CAN_C Receive GPIO	PCR[88]	01 00	I I/O	VDDEH6a Slow	– / Up	– / Up		81	98	L14

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPBGA
DSPI_B_PCS[5] DSPI_C_PCS[0] GPIO[110]	DSPI_B Periph Chip Select DSPI_C Periph Chip Select GPIO	PCR[110]	01 10 00	O O I/O	VDDEH6b Medium	– / Up	– / Up		87	104	J13
eQADC											
AN[0][27] DAN0+	Single Ended Analog Input Positive Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[0] / –		143	172	B5
AN[1][27] DAN0-	Single Ended Analog Input Negative Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[1] / –		142	171	A6
AN[2][27] DAN1+	Single Ended Analog Input Positive Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[2] / –		141	170	D6
AN[3][27] DAN1-	Single Ended Analog Input Negative Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[3] / –		140	169	C7
AN[4][27] DAN2+	Single Ended Analog Input Positive Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[4] / –		139	168	B6
AN[5][27] DAN2-	Single Ended Analog Input Negative Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[5] / –		138	167	A7
AN[6][27] DAN3+	Single Ended Analog Input Positive Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[6] / –		137	166	D7
AN[7][27] DAN3-	Single Ended Analog Input Negative Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[7] / –		136	165	C8
AN[8]	See AN[38]-AN[8]-ANW										
AN[9] ANX	Single Ended Analog Input External Multiplexed Analog Input	—	—	I I	VDDA	I / –	AN[9] / –		5	5	A2
AN[10]	See AN[39]-AN[10]-ANY										
AN[11] ANZ	Single Ended Analog Input External Multiplexed Analog Input	—	—	I I	VDDA	I / –	AN[11] / –		4	4	A3
AN[12] MA[0] ETPU_A[19] $\overline{SDS}$	Single Ended Analog Input Mux Address ETPU_A Ch. eQADC Serial Data Strobe	PCR[215]	011 010 100 000	I O O O	VDDEH7	I / –	AN[12] / –		119	148	A12

Table 4. Signal details (continued)

Signal	Module or Function	Description
CAL_RD_$\overline{WR}$	Calibration Bus	RD_$\overline{WR}$ indicates whether the current transaction is a read access or a write access.
CAL_$\overline{TS}$_ALE	Calibration Bus	The Transfer Start signal ($\overline{TS}$) is asserted by the MPC5634M to indicate the start of a transfer. The Address Latch Enable (ALE) signal is used to demultiplex the address from the data bus.
CAL_$\overline{EVTO}$	Calibration Bus	Nexus Event Out
CAL_MCKO	Calibration Bus	Nexus Message Clock Out
NEXUSCFG	Nexus/Calibration Bus	Nexus/Calibration Bus selector
eMIOS[0:23]	eMIOS	eMIOS I/O channels
AN[0:39]	eQADC	Single-ended analog inputs for analog-to-digital converter
FCK	eQADC	eQADC free running clock for eQADC SSI.
MA[0:2]	eQADC	These three control bits are output to enable the selection for an external Analog Mux for expansion channels.
REFBYPC	eQADC	Bypass capacitor input
SDI	eQADC	Serial data in
SDO	eQADC	Serial data out
SDS	eQADC	Serial data select
VRH	eQADC	Voltage reference high input
VRL	eQADC	Voltage reference low input
SCI_A_RX SCI_B_RX	eSCI_A – eSCI_B	eSCI receive
SCI_A_TX SCI_B_TX	eSCI_A – eSCI_B	eSCI transmit
ETPU_A[0:31]	eTPU	eTPU I/O channel
CAN_A_TX CAN_C_TX	FlexCan_A – FlexCAN_C	FlexCAN transmit
CAN_A_RX CAN_C_RX	FlexCAN_A – FlexCAN_C	FlexCAN receive
JCOMP	JTAG	Enables the JTAG TAP controller.
TCK	JTAG	Clock input for the on-chip test and debug logic.
TDI	JTAG	Serial test instruction and data input for the on-chip test and debug logic.
TDO	JTAG	Serial test data output for the on-chip test logic.
TMS	JTAG	Controls test mode operations for the on-chip test and debug logic.

4 Electrical characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5634M series of MCUs.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol "CC" for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol "SR" for System Requirement is included in the Symbol column.

4.1 Parameter classification

The electrical parameters shown in this document are guaranteed by various methods. To provide a better understanding, the classifications listed in Table 6 are used and the parameters are tagged accordingly in the tables. Note that only controller characteristics ("CC") are classified. System requirements ("SR") are operating conditions that must be provided to ensure normal device operation.

Table 6. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled "C" in the parameter tables where appropriate.

4.2 Maximum ratings

Table 7. Absolute maximum ratings[1]

Symbol		Parameter	Conditions	Value		Unit
				min	max	
V_{DD}	SR	1.2 V core supply voltage[2]		– 0.3	1.32	V
V_{FLASH}	SR	Flash core voltage[3]		– 0.3	5.5	V
V_{STBY}	SR	SRAM standby voltage[4]		– 0.3	5.5	V
V_{DDPLL}	SR	Clock synthesizer voltage		– 0.3	1.32	V
V_{RC33}[5]	SR	Voltage regulator control input voltage		– 0.3	3.6	V

[7] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.3.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)
$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)
P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} * P_D) \quad \textit{Eqn. 2}$$

where:

T_B = board temperature for the package perimeter (^oC)
$R_{\theta JB}$ = junction-to-board thermal resistance ($^oC/W$) per JESD51-8S
P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

- B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

4.4 Electromagnetic Interference (EMI) characteristics

Table 11. EMI testing specifications[1]

Symbol	Parameter	Conditions	f_{OSC}/f_{BUS}	Frequency	Level (Typ)	Unit
Radiated Emissions	V_{EME}	Device Configuration, test conditions and EM testing per standard IEC61967-2; Supply Voltage = 5.0V DC, Ambient Temperature = 25°C, Worst-case Orientation	Oscillator Frequency = 8 MHz; System Bus Frequency = 80 MHz; No PLL Frequency Modulation	150 kHz – 50 MHz	26	dBμV
				50–150 MHz	24	
				150–500 MHz	24	
				500–1000 MHz	21	
				IEC Level	K	—
			Oscillator Frequency = 8 MHz; System Bus Frequency = 80 MHz; 1% PLL Frequency Modulation	150 kHz – 50 MHz	20	dBμV
				50–150 MHz	19	
				150–500 MHz	14	
				500–1000 MHz	7	
				IEC Level	L	—

1 IEC Classification Level: L = 24dBuV; K = 30dBuV.

4.5 Electromagnetic static discharge (ESD) characteristics

Table 12. ESD ratings[1,2]

Symbol		Parameter	Conditions	Value	Unit
—	SR	ESD for Human Body Model (HBM)	—	2000	V
R1	SR	HBM circuit description	—	1500	Ω
C	SR		—	100	pF
—	SR	ESD for field induced charge Model (FCDM)	All pins	500	V
			Corner pins	750	
—	SR	Number of pulses per pin	Positive pulses (HBM)	1	—
			Negative pulses (HBM)	1	—
—	SR	Number of pulses	—	1	—

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature.”

Table 22. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
I_{DDH1} I_{DDH6} I_{DDH7} I_{DD7} I_{DDH9} I_{DD12}	CC	D	Operating current V_{DDE}[23] supplies @ 80 MHz	V_{DDEH1}	—	—	See note [23]	mA
		D		V_{DDEH6}	—	—		
		D		V_{DDEH7}	—	—		
		D		V_{DDE7}	—	—		
		D		V_{DDEH9}	—	—		
		D		V_{DDE12}	—	—		
I_{ACT_S}	CC	C	Slow/medium I/O weak pull up/down current[24]	3.0 V – 3.6 V	15	—	95	µA
		P		4.75 V – 5.25 V	35	—	200	
I_{ACT_F}	CC	D	Fast I/O weak pull up/down current[24]	1.62 V – 1.98 V	36	—	120	µA
		D		2.25 V – 2.75 V	34	—	139	
		D		3.0 V – 3.6 V	42	—	158	
$I_{ACT\_MV\_PU}$	CC	C	Multi-voltage pad weak pullup current	V_{DDEH}= 3.0–3.6 V[10], pad_multv_hv, all process corners, high swing mode only	10	—	75	µA
		P		4.75 V – 5.25 V	25	—	200	
$I_{ACT\_MV\_PD}$	CC	C	Multivoltage pad weak pulldown current	V_{DDEH}= 3.0–3.6 V[10], pad_multv_hv, all process corners, high swing mode only	10	—	60	µA
		P		4.75 V – 5.25 V	25	—	200	
I_{INACT_D}	CC	P	I/O input leakage current[25]	—	–2.5	—	2.5	µA
I_{IC}	CC	T	DC injection current (per pin)	—	–1.0	—	1.0	mA
I_{INACT_A}	CC	P	Analog input current, channel off, AN[0:7], AN38, AN39[26]	—	–250	—	250	nA
		P	Analog input current, channel off, all other analog pins (ANx)[26]	—	–150	—	150	

Table 25. V_{RC33} pad average DC current[1]

Pad Type	Symbol		C	Period (ns)	Load[2] (pF)	V_{RC33} (V)	V_{DDE} (V)	Drive Select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Fast	I_{DRV_FC}	CC	D	10	50	3.6	3.6	11	2.35	6.12
		CC	D	10	30	3.6	3.6	10	1.75	4.3
		CC	D	10	20	3.6	3.6	01	1.41	3.43
		CC	D	10	10	3.6	3.6	00	1.06	2.9
		CC	D	10	50	3.6	1.98	11	1.75	4.56
		CC	D	10	30	3.6	1.98	10	1.32	3.44
		CC	D	10	20	3.6	1.98	01	1.14	2.95
		CC	D	10	10	3.6	1.98	00	0.95	2.62

1 These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

2 All loads are lumped.

4.9.2 LVDS pad specifications

LVDS pads are implemented to support the MSC (Microsecond Channel) protocol which is an enhanced feature of the DSPI module. The LVDS pads are compliant with LVDS specifications and support data rates up to 50 MHz.

Table 26. DSPI LVDS pad specification [1, 2]

#	Characteristic	Symbol	C		Condition	Min. Value	Typ. Value	Max. Value	Unit
Data Rate									
4	Data Frequency	$F_{LVDSCLK}$	CC	D			50		MHz
Driver Specs									
5	Differential output voltage	V_{OD}[3]	CC	P	SRC=0b00 or 0b11	150		430	mV
			CC	P	SRC=0b01	90		340	
			CC	P	SRC=0b10	155		480	
6	Common mode voltage (LVDS), V_{OS}	V_{OS}[3]	CC	P		0.8	1.2	1.6	V
7	Rise/Fall time	T_R/T_F	CC	D			2		ns
8	Propagation delay (Low to High)	T_{PLH}	CC	D			4		ns
9	Propagation delay (High to Low)	T_{PHL}	CC	D			4		ns
10	Delay (H/L), sync Mode	t_{PDSYNC}	CC	D			4		ns
11	Delay, Z to Normal (High/Low)	T_{DZ}	CC	D			500		ns

Table 26. DSPI LVDS pad specification [1, 2] (continued)

12	Diff Skew ltphla-tplhbl or ltplhb-tphlal	T_{SKEW}	CC	D				0.5	ns
Termination									
13	Trans. Line (differential Zo)		CC	D		95	100	105	Ω
14	Temperature		CC	D		–40		150	°C

1 These are typical values that are estimated from simulation.

2 These specifications are subject to change per device characterization.

3 Preliminary target values. Actual specifications to be determined.

4.10 Oscillator and PLLMRFM electrical characteristics

Table 27. PLLMRFM electrical specifications[1]

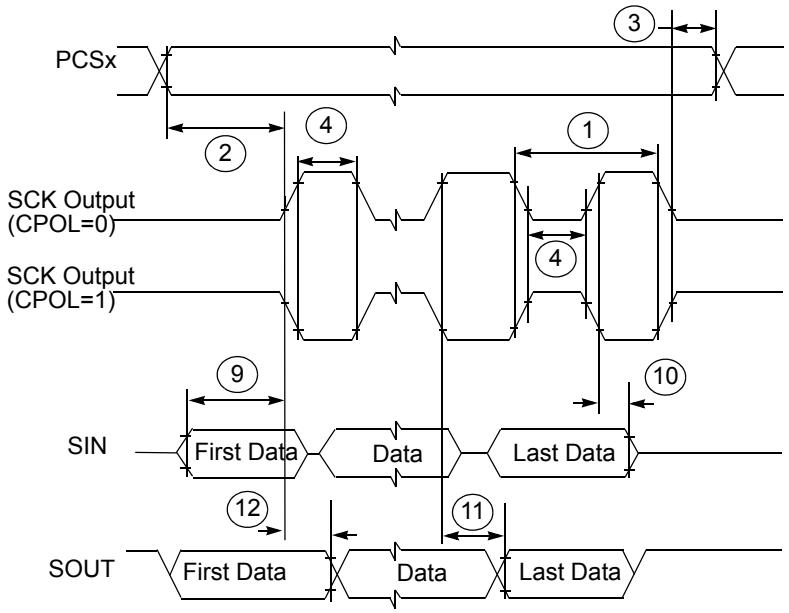
(V_{DDPLL} =1.14 V to 1.32 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H)

Symbol		C	Parameter		Conditions	Value		Unit
						min	max	
$f_{ref\_crystal}$ f_{ref_ext}	CC	D	PLL reference frequency range[2]		Crystal reference	4	20	MHz
		C			External reference	4	80	
f_{pll_in}	CC	P	Phase detector input frequency range (after pre-divider)		—	4	16	MHz
f_{vco}	CC	P	VCO frequency range[3]		—	256	512	MHz
f_{sys}	CC	C	On-chip PLL frequency[2]		—	16	80	MHz
f_{sys}	CC	T	System frequency in bypass mode[4]		Crystal reference	4	20	MHz
		P			External reference	0	80	
t_{CYC}	CC	D	System clock period		—	—	1 / f_{sys}	ns
f_{LORL} f_{LORH}	CC	D	Loss of reference frequency window[5]		Lower limit	1.6	3.7	MHz
		D			Upper limit	24	56	
f_{SCM}	CC	P	Self-clocked mode frequency [6,7]		—	1.2	75	MHz
C_{JITTER}	CC	T	CLKOUT period jitter[8,9,10,11]	Peak-to-peak (clock edge to clock edge)	f_{SYS} maximum	–5	5	% f_{CLKOUT}
		T		Long-term jitter (avg. over 2 ms interval)		–6	6	ns
t_{cst}	CC	T	Crystal start-up time [12, 13]		—	—	10	ms
V_{IHEXT}	CC	T	EXTAL input high voltage		Crystal Mode[14], 0.8 ≤ Vxtal ≤ 1.5V[15]	Vxtal + 0.4	—	V
		T			External Reference[14, 16]	V_{RC33}/2 + 0.4	V_{RC33}	

3 This parameter is supplied for reference and is not guaranteed by design and not tested.
4 Delay and rise/fall are measured to 20% or 80% of the respective signal.
5 This parameter is guaranteed by characterization before qualification rather than 100% tested.
6 In high swing mode, high/low swing pad Vol and Voh values are the same as those of the slew controlled output pads
7 Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
8 Output delay is shown in Figure 8. Add a maximum of one system clock to the output delay for delay with respect to system clock.
9 Can be used on the tester.
10 This drive select value is not supported. If selected, it will be approximately equal to 11.
11 Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
12 Selectable high/low swing IO pad with selectable slew in high swing mode only.
13 Fast pads are 3.3 V pads.
14 Stand alone input buffer. Also has weak pull-up/pull-down.

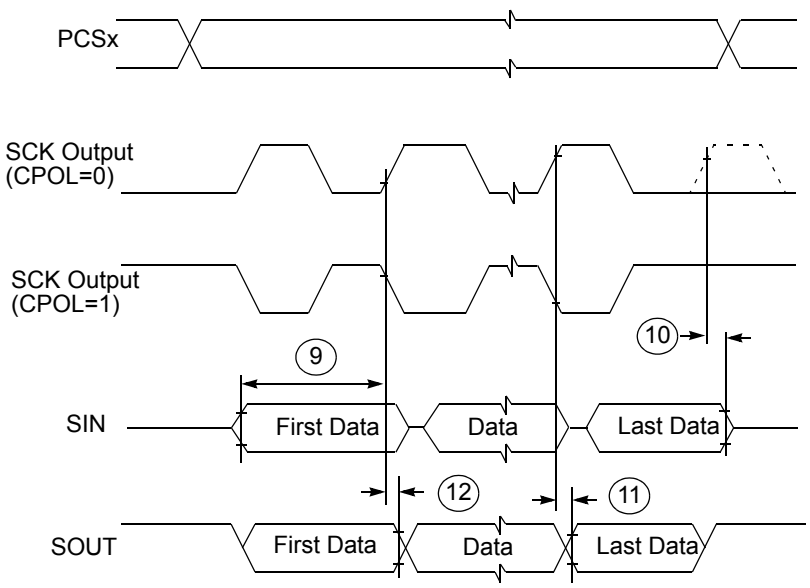
Table 34. Pad AC specifications (3.3 V)[1]

Pad Type		C	Output Delay (ns)[2,3] Low-to-High / High-to-Low		Rise/Fall Edge (ns)[3,4]		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium[5,6,7]	CC	D	5.8/4.4	18/17	2.7/2.1	10/10	50	11[8]
	CC	D	16/13	46/49	11.2/8.6	34/34	200	
	N/A							10[9]
	CC	D	14/16	37/45	6.5/6.7	19/19	50	01
	CC	D	27/27	69/82	15/13	43/43	200	
	CC	D	83/86	200/210	38/38	86/86	50	00
	CC	D	113/109	270/285	53/46	120/120	200	
Slow[7,10]	CC	D	9.2/6.9	27/28	5.5/4.1	20/20	50	11
	CC	D	30/23	81/87	21/16	63/63	200	
	N/A							10[9]
	CC	D	31/31	80/90	15.4/15.4	42/42	50	01
	CC	D	58/52	144/155	32/26	82/85	200	
	CC	D	162/168	415/415	80/82	190/190	50	00
	CC	D	216/205	533/540	106/95	250/250	200	
MultiV[7,11] (High Swing Mode)	CC	D		3.7/3.1		10/10	30	11[8]
	CC	D		46/49		37/37	200	
	N/A							10[9]
	CC	D		32		15/15	50	01
	CC	D		72		46/46	200	
	CC	D		210		100/100	50	00
	CC	D		295		134/134	200	



These numbers reference Table 40.

Figure 24. DSPI modified transfer format timing – master, CPHA = 0



These numbers reference Table 40.

Figure 25. DSPI modified transfer format timing – master, CPHA = 1

5 Packages

5.1 Package mechanical data

5.1.1 144 LQFP

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23177W
		PAGE: 918
	DO NOT SCALE THIS DRAWING	REV: F

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.
4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 mm.
5. THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.
7. THIS DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

TITLE: 144 LEAD LQFP 20 X 20, 0.5 PITCH, 1.4 THICK	CASE NUMBER: 918–03	
	STANDARD: NON–JEDEC	
	PACKAGE CODE: 8259	SHEET: 3

Figure 32. 144 LQFP package mechanical drawing (part 3)

Table 43. Revision history (continued)

Revision	Date	Description of Changes
Rev. 5 (cont.)	04/2010	PMC Operating conditions and external regulators supply voltage specifications updated • (2) PMC 5 V supply voltage VDDREG min value is 4.5 V (was 4.75 V) PMC electrical characteristics specifications updated • (1d) Bandgap reference supply voltage variation is 3000 ppm/V (was 1500 ppm/V) • (5a) Nominal 3.3 V supply internal regulator DC output voltage variation at power-on reset min value is Vdd33-8.5% (was unspecified previously) • (5a) Nominal 3.3 V supply internal regulator DC output voltage variation at power-on reset max value is Vdd3+7% (was unspecified previously) • (9a) Variation of POR for rising 5 V VDDREG supply max value is Por5V_r + 50% (was Por5V_r + 35%) • (9c) Variation of POR for falling 5 V VDDREG supply max value is Por5V_f + 50% (was Por5V_f + 35%) • (9c) note added: Minimum loading (<10 mA) for reading trim values from flash, powering internal RC oscillator, and IO consumption during POR. “Core Voltage Regulator Controller External Components Preferred Configuration” circuit diagram updated Changes to DC Electrical Specifications: • Footnote added to V_{DDE}. V_{DDE} must be less than V_{RC33} or there is additional leakage on pins supplied by V_{DDE}. • Low range SRAM standby voltage (V_{STBY}) minimum changed to 0.95 V (was 0.9 V) • Low range SRAM standby voltage (V_{STBY}) maximum changed to 1.2 V (was 1.3 V) • High range SRAM standby voltage (V_{STBY}) minimum changed to 2.0 V (was 2.5 V) • V_{IL_LS} max value (Hysteresis disabled) changed to 0.9 V (was 1.1 V) • V_{OH_LS} min value changed to 2 V (was 2.3 V) • I_{DDSLOW} max value is 50 mA • I_{DDSTOP} max value is 50 mA • I_{DDA} max value is 30 mA (was 15.0 mA) • I_{DD4} and V_{DDEH4} removed—they no longer exist I/O pad average I_{DDE} specifications table updated I/O pad V_{RC33} average I_{DDE} specifications table updated LVDS pad specifications table updated • V_{OS} min value is 0.9 V (was 1.075 V) • V_{OS} max value is 1.6 V (was 1.325 V) Updates to PLLMRFM electrical specifications: • Maximum values for XTAL load capacitance added. The maximum value varies with frequency. • For a 20 MHz crystal the maximum load should be 17 pF. Temperature sensor accuracy is ±10 °C (was ±5 °C) Updates to eQADC conversion specifications (operating): • Offset error without calibration max value is 160 (was 100) • Full scale gain error without calibration min value is –160 (was –120) Changes to Platform flash controller electrical characteristics: • APC, RWSC, WWSC settings vs. frequency of operation table updated