Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	E200z335
Core Size	32-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	94K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 34x12b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BGA
Supplier Device Package	208-BGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5634mf2mmg80

— Enabled out of reset

- Enhanced modular I/O system (eMIOS)
  - 16 timer channels (up to 14 channels in 144 LQFP)
  - 24-bit timer resolution
  - Supports a subset of the timer modes found in eMIOS on MPC5554
  - 3 selectable time bases plus shared time or angle counter bus from eTPU2
  - DMA and interrupt request support
  - Motor control capability
- Second-generation enhanced time processor unit (eTPU2)
  - Object-code compatible with eTPU—no changes are required to hardware or software if only eTPU features are used
  - Intelligent co-processor designed for timing control
  - High level tools, assembler and compiler available
  - 32 channels (each channel has dedicated I/O pin in all packages)
  - 24-bit timer resolution
  - 14 KB code memory and 3 KB data memory
  - Double match and capture on all channels
  - Angle clock hardware support
  - Shared time or angle counter bus with eMIOS
  - DMA and interrupt request support
  - Nexus Class 1 debug support
  - eTPU2 enhancements
    - Counters and channels can run at full system clock speed
    - Software watchdog
    - Real-time performance monitor
    - Instruction set enhancements for smaller more flexible code generation
    - Programmable channel mode for customization of channel operation
- Enhanced queued A/D converter (eQADC)
  - Two independent on-chip redundant signed digit (RSD) cyclic ADCs
    - 8-, 10-, and 12-bit resolution
    - Differential conversions
    - Targets up to 10-bit accuracy at 500 KSample/s (ADC_CLK = 7.5 MHz) and 8-bit accuracy at 1 MSample/s (ADC_CLK = 15 MHz) for differential conversions
    - Differential channels include variable gain amplifier (VGA) for improved dynamic range (×1; ×2; ×4)
    - Differential channels include programmable pull-up and pull-down resistors for biasing and sensor diagnostics (200 kΩ; 100 kΩ; low value of 5 kΩ)
    - Single-ended signal range from 0 to 5 V
    - Sample times of 2 (default), 8, 64 or 128 ADC clock cycles
    - Provides time stamp information when requested
    - Parallel interface to eQADC command FIFOs (CFIFOs) and result FIFOs (RFIFOs)
    - Supports both right-justified unsigned and signed formats for conversion results
    - Temperature sensor to enable measurement of die temperature
    - Ability to measure all power supply pins directly
  - Automatic application of ADC calibration constants
    - Provision of reference voltages (25% VREF and 75% VREF) for ADC calibration purposes
  - Up to 34[1] input channels available to the two on-chip ADCs

results to the result FIFOs. This allows the ADCs to sample the sensor at a rate high enough to avoid aliasing of out-of-band noise; while providing a reduced sample rate output to minimize the amount DSP processing bandwidth required to fully process the digitized waveform.

The eQADC provides the following features:

- Dual on-chip ADCs
  - 2 × 12-bit ADC resolution
  - Programmable resolution for increased conversion speed (12 bit, 10 bit, 8 bit)
    - 12-bit conversion time – 1 µs (1M sample/sec)
    - 10-bit conversion time – 867 ns (1.2M sample/second)
    - 8-bit conversion time – 733 ns (1.4M sample/second)
  - Up to 10-bit accuracy at 500 KSample/s and 9-bit accuracy at 1 MSample/s
  - Differential conversions
  - Single-ended signal range from 0 to 5 V
  - Variable gain amplifiers on differential inputs (×1, ×2, ×4)
  - Sample times of 2 (default), 8, 64 or 128 ADC clock cycles
  - Provides time stamp information when requested
  - Parallel interface to eQADC CFIFOs and RFIFOs
  - Supports both right-justified unsigned and signed formats for conversion results
- Up to 34[1] input channels (accessible by both ADCs)
- 23 additional internal channels for measuring control and monitoring voltages inside the device
  - Including Core voltage, I/O voltage, LVI voltages, etc.
- An internal bandgap reference to allow absolute voltage measurements
- 4 pairs of differential analog input channels
  - Programmable pull-up/pull-down resistors on each differential input for biasing and sensor diagnostic (200 kΩ, 100 kΩ, 5 kΩ)
- Silicon die temperature sensor
  - provides temperature of silicon as an analog value
  - read using an internal ADC analog channel
  - may be read with either ADC
- Decimation Filter
  - Programmable decimation factor (2 to 16)
  - Selectable IIR or FIR filter
  - Up to 4th order IIR or 8th order FIR
  - Programmable coefficients
  - Saturated or non-saturated modes
  - Programmable Rounding (Convergent; Two’s Complement; Truncated)
  - Pre-fill mode to pre-condition the filter before the sample window opens
- Full duplex synchronous serial interface to an external device
  - Free-running clock for use by an external device
  - Supports a 26-bit message length
- Priority based Queues
  - Supports six Queues with fixed priority. When commands of distinct Queues are bound for the same ADC, the higher priority Queue is always served first

1. 176-pin and 208-pin packages have 34 input channels; 144-pin package has 32.

- Selectable backwards compatibility with previous FlexCAN versions
- Programmable clock source to the CAN Protocol Interface, either system clock or oscillator clock
- Listen only mode capability
- Programmable loop-back mode supporting self-test operation
- 3 programmable Mask Registers
- Programmable transmit-first scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Warning interrupts when the Rx and Tx Error Counters reach 96
- Independent of the transmission medium (an external transceiver is assumed)
- Multi master concept
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode, with programmable wake-up on bus activity

2.2.18 System timers

The system timers provide two distinct types of system timer:

- Periodic interrupts/triggers using the Periodic Interrupt Timer (PIT)
- Operating system task monitors using the System Timer Module (STM)

2.2.18.1 Periodic Interrupt Timer (PIT)

The PIT provides five independent timer channels, capable of producing periodic interrupts and periodic triggers. The PIT has no external input or output pins and is intended to be used to provide system ‘tick’ signals to the operating system, as well as periodic triggers for eQADC queues. Of the five channels in the PIT, four are clocked by the system clock, one is clocked by the crystal clock. This one channel is also referred to as Real Time Interrupt (RTI) and is used to wakeup the device from low power stop mode.

The following features are implemented in the PIT:

- 5 independent timer channels
- Each channel includes 32-bit wide down counter with automatic reload
- 4 channels clocked from system clock
- 1 channel clocked from crystal clock (wake-up timer)
- Wake-up timer remains active when System STOP mode is entered. Used to restart system clock after predefined timeout period
- Each channel can optionally generate an interrupt request or a trigger event (to trigger eQADC queues) when the timer reaches zero

2.2.18.2 System Timer Module (STM)

The System Timer Module (STM) is designed to implement the software task monitor as defined by AUTOSAR (see http://www.autosar.org). It consists of a single 32-bit counter, clocked by the system clock, and four independent timer comparators. These comparators produce a CPU interrupt when the timer exceeds the programmed value.

The following features are implemented in the STM:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels

  - Auxiliary Output port
    - 1 MCKO (message clock out) pin
    - 4 MDO (message data out) pins
    - 2 $\overline{\text{MSEO}}$ (message start/end out) pins
    - 1 $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port
    - 1 $\overline{\text{EVTI}}$ (event in) pin
- 17-pin Full Port interface in calibration package used on VertiCal boards
  - 3.3 V interface
  - Auxiliary Output port
    - 1 MCKO (message clock out) pin
    - 4 (reduced port mode) or 12 (full port mode) MDO (message data out) pins; 8 extra full port pins shared with calibration bus
    - 2 $\overline{\text{MSEO}}$ (message start/end out) pins
    - 1 $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port
    - 1 $\overline{\text{EVTI}}$ (event in) pin
- Host processor (e200) development support features
  - IEEE-ISTO 5001-2003 standard class 2 compliant
  - Program trace via branch trace messaging (BTM). Branch trace messaging displays program flow discontinuities (direct branches, indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus, static code may be traced.
  - Watchpoint trigger enable of program trace messaging
  - Data Value Breakpoints (JTAG feature of the e200z335 core): allows CPU to be halted when the CPU writes a specific value to a memory location
    - 4 data value breakpoints
    - CPU only
    - Detects ‘equal’ and ‘not equal’
    - Byte, half word, word (naturally aligned)

NOTE

This feature is imprecise due to CPU pipelining.

  - Subset of Power Architecture software debug facilities with OnCE block (Nexus class 1 features)
- eTPU development support features
  - IEEE-ISTO 5001-2003 standard class 1 compliant for the eTPU
  - Nexus based breakpoint configuration and single step support (JTAG feature of the eTPU)
- Run-time access to the on-chip memory map via the Nexus read/write access protocol. This feature supports accesses for run-time internal visibility, calibration variable acquisition, calibration constant tuning, and external rapid prototyping for powertrain automotive development systems.
- All features are independently configurable and controllable via the IEEE 1149.1 I/O port
- Power-on-reset status indication during reset via MDO[0] in disabled and reset modes

2.2.20.2 JTAG

The JTAGC (JTAG Controller) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001

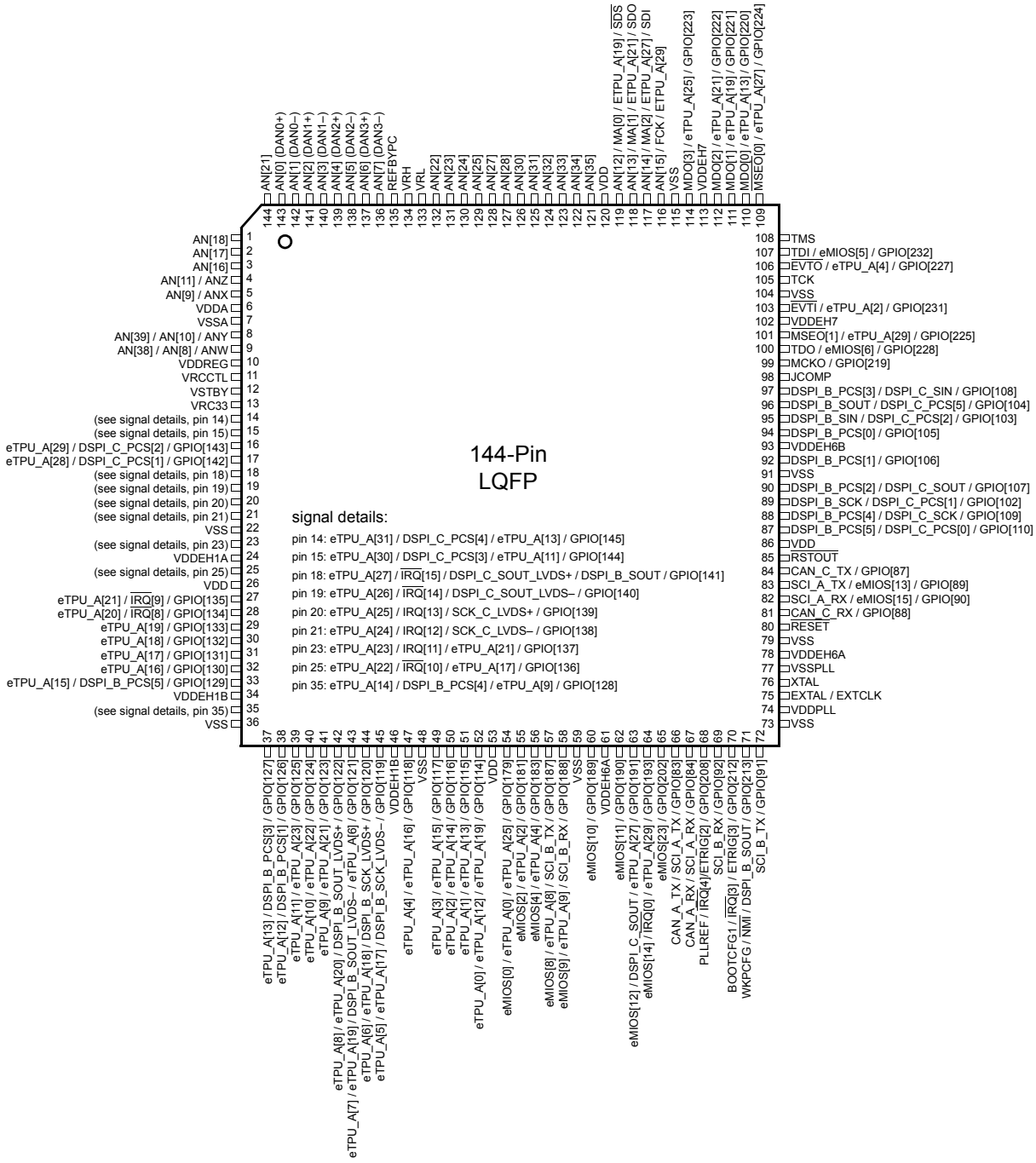
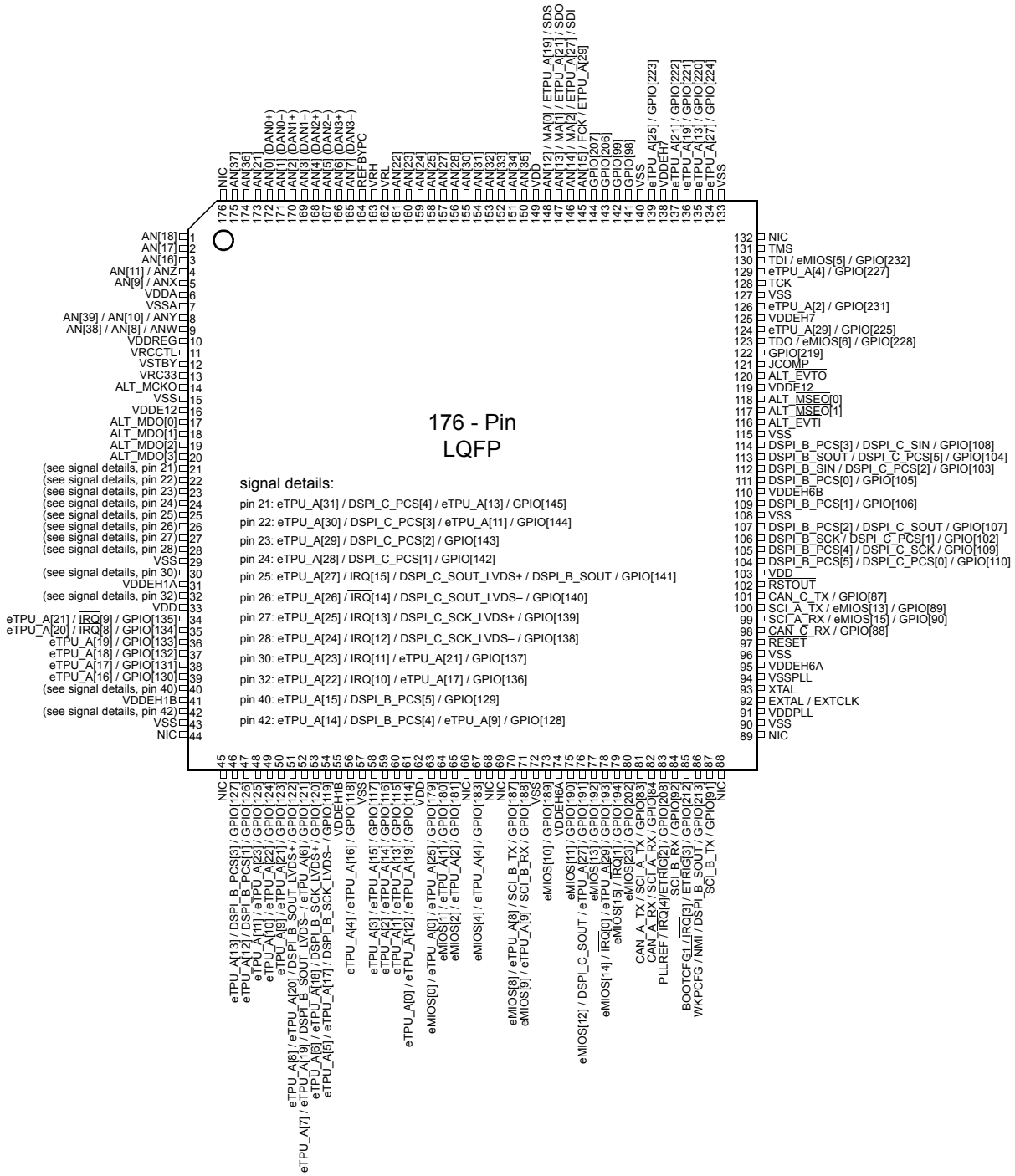


Figure 2. 144-pin LQFP pinout (top view; all 144-pin devices)

3.2 176 LQFP pinout (MPC5634M)

Figure 3 shows the 176-pin LQFP pinout for the MPC5634M (1536 KB flash memory).



Note: Pins marked “NIC” have no internal connection.

Figure 3. 176-pin LQFP pinout (MPC5634M; top view)

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]	Pin No.			
									144 LQFP	176 LQFP	208 MAPBGA
VSS	Ground	—	—	–	VSS0	I / –	—		22, 36, 48, 59, 73, 79, 91, 104, 115	15, 29, 43, 57, 72, 90, 96, 108, 115[7], 127, 133, 140	A1, A16, B2, B15, C3, C14, D4, D13, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, N4, N13, P3, P14, R2, R15, T1, T16
VDDEH1A[36] VDDEH1B[36]	I/O Supply Input	—	—	I	VDDEH1[37] (3.3V – 5.0V)	I / –	—		24, 34, 46	31, 41 55	K4
VDDE5	I/O Supply Input	—	—	I	VDDE5	I / –	—		—	—	T13
VDDEH6a[38, 39] VDDEH6b[39]	I/O Supply Input	—	—	I	VDDEH6 (3.3V – 5.0V)	I / –	—		78, 93, 61	95, 110, 74	—
VDDEH6	I/O Supply Input	—	—	I	VDDEH6	I / –	—		—	—	F13
VDDEH7	I/O Supply Input	—	—	I	VDDEH7[40] (3.3V – 5.0V)	I / –	—		102, 113	125, 138	D12
VDDE7[41]	I/O Supply Input	—	—	I	VDDE7 (3.3V)	I / –	—		—	16, 119[7]	E13, P6

1 For each pin in the table, each line in the Function column is a separate function of the pin. For all I/O pins the selection of primary pin function or secondary function or GPIO is done in the SIU except where explicitly noted.

2 Values in this column refer to registers in the System Integration Unit (SIU). The actual register name is “SIU_PCR” suffixed by the PCR number. For example, PCR[190] refers to the SIU register named SIU_PCR190.

3 The Pad Configuration Register (PCR) PA field is used by software to select pin function.

4 The VDDE and VDDEH supply inputs are broken into segments. Each segment of slow I/O pins (VDDEH) may have a separate supply in the 3.3 V to 5.0 V range (–10%/+5%). Each segment of fast I/O (VDDE) may have a separate supply in the 1.8 V to 3.3 V range (+/– 10%).

5 Terminology is O — output, I — input, Up — weak pull up enabled, Down — weak pull down enabled, Low — output driven low, High — output driven high. A dash for the function in this column denotes that both the input and output buffer are turned off.

6 Function after reset of GPI is general purpose input. A dash for the function in this column denotes that both the input and output buffer are turned off.

7 Not available on 1 MB version of 176-pin package.

8 Not available on 1 MB version of 208-pin package.

Table 14. PMC electrical characteristics (continued)

ID	Name		C	Parameter	Min	Typ	Max	Unit	Notes
5b	—	CC	P	Nominal 3.3 V supply internal regulator DC output voltage variation after power-on reset	Vdd33 – 7.5%	Vdd33	Vdd33 + 7%	V	With internal load up to Idd3p3
5c	—	CC	D	Voltage regulator 3.3 V output impedance at maximum DC load	—	—	2	Ω	
5d	Idd3p3	CC	P	Voltage regulator 3.3 V maximum DC output current	80	—	—	mA	
5e	Vdd33 ILim[6]	CC	C	Voltage regulator 3.3 V DC current limit	—	130	—	mA	
6	Lvi3p3	CC	C	Nominal LVI for rising 3.3 V supply[5]	—	3.090	—	V	The Lvi3p3 specs are also valid for the Vddeh LVI
6a	—	CC	C	Variation of LVI for rising 3.3 V supply at power-on reset[5]	Lvi3p3–6%	Lvi3p3	Lvi3p3+6%	V	See note [7]
6b	—	CC	C	Variation of LVI for rising 3.3 V supply after power-on reset[5]	Lvi3p3–3%	Lvi3p3	Lvi3p3+3%	V	See note 7
6c	—	CC	C	Trimming step LVI 3.3 V[5]	—	20	—	mV	
6d	Lvi3p3_h	CC	C	LVI 3.3 V hysteresis[5]	—	60	—	mV	
7	Por3.3V_r	CC	C	Nominal POR for rising 3.3 V supply	—	2.07	—	V	The 3.3V POR specs are also valid for the Vddeh POR
7a	—	CC	C	Variation of POR for rising 3.3 V supply	Por3.3V_r–35%	Por3.3V_r	Por3.3V_r+35%	V	
7b	Por3.3V_f	CC	C	Nominal POR for falling 3.3 V supply	—	1.95	—	V	
7c	—	CC	C	Variation of POR for falling 3.3 V supply	Por3.3V_f–35%	Por3.3V_f	Por3.3V_f+35%	V	
8	Lvi5p0	CC	C	Nominal LVI for rising 5 V VDDREG supply[5]	—	4.290	—	V	
8a	—	CC	C	Variation of LVI for rising 5 V VDDREG supply at power-on reset[5]	Lvi5p0–6%	Lvi5p0	Lvi5p0+6%	V	
8b	—	CC	C	Variation of LVI for rising 5 V VDDREG supply power-on reset[5]	Lvi5p0–3%	Lvi5p0	Lvi5p0+3%	V	
8c	—	CC	C	Trimming step LVI 5 V[5]	—	20	—	mV	

Table 22. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
I_{DDH1} I_{DDH6} I_{DDH7} I_{DD7} I_{DDH9} I_{DD12}	CC	D	Operating current V_{DDE}[23] supplies @ 80 MHz	V_{DDEH1}	—	—	See note [23]	mA
		D		V_{DDEH6}	—	—		
		D		V_{DDEH7}	—	—		
		D		V_{DDE7}	—	—		
		D		V_{DDEH9}	—	—		
		D		V_{DDE12}	—	—		
I_{ACT_S}	CC	C	Slow/medium I/O weak pull up/down current[24]	3.0 V – 3.6 V	15	—	95	µA
		P		4.75 V – 5.25 V	35	—	200	
I_{ACT_F}	CC	D	Fast I/O weak pull up/down current[24]	1.62 V – 1.98 V	36	—	120	µA
		D		2.25 V – 2.75 V	34	—	139	
		D		3.0 V – 3.6 V	42	—	158	
$I_{ACT\_MV\_PU}$	CC	C	Multi-voltage pad weak pullup current	V_{DDEH}= 3.0–3.6 V[10], pad_multv_hv, all process corners, high swing mode only	10	—	75	µA
		P		4.75 V – 5.25 V	25	—	200	
$I_{ACT\_MV\_PD}$	CC	C	Multivoltage pad weak pulldown current	V_{DDEH}= 3.0–3.6 V[10], pad_multv_hv, all process corners, high swing mode only	10	—	60	µA
		P		4.75 V – 5.25 V	25	—	200	
I_{INACT_D}	CC	P	I/O input leakage current[25]	—	–2.5	—	2.5	µA
I_{IC}	CC	T	DC injection current (per pin)	—	–1.0	—	1.0	mA
I_{INACT_A}	CC	P	Analog input current, channel off, AN[0:7], AN38, AN39[26]	—	–250	—	250	nA
		P	Analog input current, channel off, all other analog pins (ANx)[26]	—	–150	—	150	

Table 22. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
C_L	CC	D	Load capacitance (fast I/O)[27]	DSC(PCR[8:9]) = 0b00	—	—	10	pF
		D		DSC(PCR[8:9]) = 0b01	—	—	20	
		D		DSC(PCR[8:9]) = 0b10	—	—	30	
		D		DSC(PCR[8:9]) = 0b11	—	—	50	
C_{IN}	CC	D	Input capacitance (digital pins)	—	—	—	7	pF
C_{IN_A}	CC	D	Input capacitance (analog pins)	—	—	—	10	pF
C_{IN_M}	CC	D	Input capacitance (digital and analog pins[28])	—	—	—	12	pF
$R_{PUPD200K}$	CC	P	Weak Pull-Up/Down Resistance[29,30] 200 kΩ Option	—	130	—	280	kΩ
$R_{PUPDMATCH}$	CC	C	200KΩ Option		–2.5		2.5	%
$R_{PUPD100K}$	CC	P	Weak Pull-Up/Down Resistance[29,30] 100 kΩ Option	—	65	—	140	kΩ
$R_{PUPDMATCH}$	CC	C	100KΩ Option		–2.5		2.5	%
R_{PUPD5K}	CC	D	Weak Pull-Up/Down Resistance[29] 5 kΩ Option	5 V ± 5% supply	1.4	—	7.5	kΩ
T_A (T_L to T_H)	SR	—	Operating temperature range - ambient (packaged)	—	–40.0	—	125.0	°C
—	SR	—	Slew rate on power supply pins	—	—	—	50	V/ms

1 These specifications are design targets and subject to change per device characterization.

2 TBD: To Be Defined.

3 V_{DDE} must be lower than V_{RC33}, otherwise there is additional leakage on pins supplied by V_{DDE}.

4 These specifications apply when V_{RC33} is supplied externally, after disabling the internal regulator (V_{DDREG} = 0).

5 ADC is functional with 4 V ≤ V_{DDA} ≤ 4.75 V but with derated accuracy. This means the ADC will continue to function at full speed with no bad behavior, but the accuracy will be degraded.

6 Internal structures hold the input voltage less than V_{DDA} + 1.0 V on all pads powered by V_{DDA} supplies, if the maximum injection current specification is met (3 mA for all pins) and V_{DDA} is within the operating voltage specifications.

7 The V_{DDF} supply is connected to V_{DD} in the package substrate. This specification applies to calibration package devices only.

Table 26. DSPI LVDS pad specification [1, 2] (continued)

12	Diff Skew ltphla-tplhbl or ltplhb-tphlal	T_{SKEW}	CC	D				0.5	ns
Termination									
13	Trans. Line (differential Zo)		CC	D		95	100	105	Ω
14	Temperature		CC	D		–40		150	°C

1 These are typical values that are estimated from simulation.

2 These specifications are subject to change per device characterization.

3 Preliminary target values. Actual specifications to be determined.

4.10 Oscillator and PLLMRFM electrical characteristics

Table 27. PLLMRFM electrical specifications[1]

(V_{DDPLL} =1.14 V to 1.32 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H)

Symbol		C	Parameter		Conditions	Value		Unit
						min	max	
$f_{ref\_crystal}$ f_{ref_ext}	CC	D	PLL reference frequency range[2]		Crystal reference	4	20	MHz
		C			External reference	4	80	
f_{pll_in}	CC	P	Phase detector input frequency range (after pre-divider)		—	4	16	MHz
f_{vco}	CC	P	VCO frequency range[3]		—	256	512	MHz
f_{sys}	CC	C	On-chip PLL frequency[2]		—	16	80	MHz
f_{sys}	CC	T	System frequency in bypass mode[4]		Crystal reference	4	20	MHz
		P			External reference	0	80	
t_{CYC}	CC	D	System clock period		—	—	1 / f_{sys}	ns
f_{LORL} f_{LORH}	CC	D	Loss of reference frequency window[5]		Lower limit	1.6	3.7	MHz
		D			Upper limit	24	56	
f_{SCM}	CC	P	Self-clocked mode frequency [6,7]		—	1.2	75	MHz
C_{JITTER}	CC	T	CLKOUT period jitter[8,9,10,11]	Peak-to-peak (clock edge to clock edge)	f_{SYS} maximum	–5	5	% f_{CLKOUT}
		T		Long-term jitter (avg. over 2 ms interval)		–6	6	ns
t_{cst}	CC	T	Crystal start-up time [12, 13]		—	—	10	ms
V_{IHEXT}	CC	T	EXTAL input high voltage		Crystal Mode[14], 0.8 ≤ Vxtal ≤ 1.5V[15]	Vxtal + 0.4	—	V
		T			External Reference[14, 16]	V_{RC33}/2 + 0.4	V_{RC33}	

4.13 Platform flash controller electrical characteristics

Table 30. APC, RWSC, WWSC settings vs. frequency of operation[1]

Target Max Frequency (MHz)	APC[2]	RWSC[2]	WWSC
21[3]	000	000	01
41[3]	001	001	01
62[3]	010	010	01
82[3]	011	011	01
All	111	111	111

1 Illegal combinations exist, all entries must be taken from the same row

2 APC must be equal to RWSC

3 Maximum Frequency includes FM modulation

4.14 Flash memory electrical characteristics

Table 31. Program and erase specifications

Symbol		Parameter	Min Value	Typical Value[1]	Initial Max[2]	Max[3]	Unit
$T_{dwprogram}$	P	Double Word (64 bits) Program Time[4]	—	22	50	500	µs
$T_{16kpperase}$	P	16 KB Block Pre-program and Erase Time	—	300	500	5000	ms
$T_{32kpperase}$	P	32 KB Block Pre-program and Erase Time	—	400	600	5000	ms
$T_{64kpperase}$	P	64 KB Block Pre-program and Erase Time	—	600	900	5000	ms
$T_{128kpperase}$	P	128 KB Block Pre-program and Erase Time	—	800	1300	7500	ms

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program & erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

3 This parameter is supplied for reference and is not guaranteed by design and not tested.
4 Delay and rise/fall are measured to 20% or 80% of the respective signal.
5 This parameter is guaranteed by characterization before qualification rather than 100% tested.
6 In high swing mode, high/low swing pad Vol and Voh values are the same as those of the slew controlled output pads
7 Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
8 Output delay is shown in Figure 8. Add a maximum of one system clock to the output delay for delay with respect to system clock.
9 Can be used on the tester.
10 This drive select value is not supported. If selected, it will be approximately equal to 11.
11 Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
12 Selectable high/low swing IO pad with selectable slew in high swing mode only.
13 Fast pads are 3.3 V pads.
14 Stand alone input buffer. Also has weak pull-up/pull-down.

Table 34. Pad AC specifications (3.3 V)[1]

Pad Type		C	Output Delay (ns)[2,3] Low-to-High / High-to-Low		Rise/Fall Edge (ns)[3,4]		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium[5,6,7]	CC	D	5.8/4.4	18/17	2.7/2.1	10/10	50	11[8]
	CC	D	16/13	46/49	11.2/8.6	34/34	200	
	N/A							10[9]
	CC	D	14/16	37/45	6.5/6.7	19/19	50	01
	CC	D	27/27	69/82	15/13	43/43	200	
	CC	D	83/86	200/210	38/38	86/86	50	00
	CC	D	113/109	270/285	53/46	120/120	200	
Slow[7,10]	CC	D	9.2/6.9	27/28	5.5/4.1	20/20	50	11
	CC	D	30/23	81/87	21/16	63/63	200	
	N/A							10[9]
	CC	D	31/31	80/90	15.4/15.4	42/42	50	01
	CC	D	58/52	144/155	32/26	82/85	200	
	CC	D	162/168	415/415	80/82	190/190	50	00
	CC	D	216/205	533/540	106/95	250/250	200	
MultiV[7,11] (High Swing Mode)	CC	D		3.7/3.1		10/10	30	11[8]
	CC	D		46/49		37/37	200	
	N/A							10[9]
	CC	D		32		15/15	50	01
	CC	D		72		46/46	200	
	CC	D		210		100/100	50	00
	CC	D		295		134/134	200	

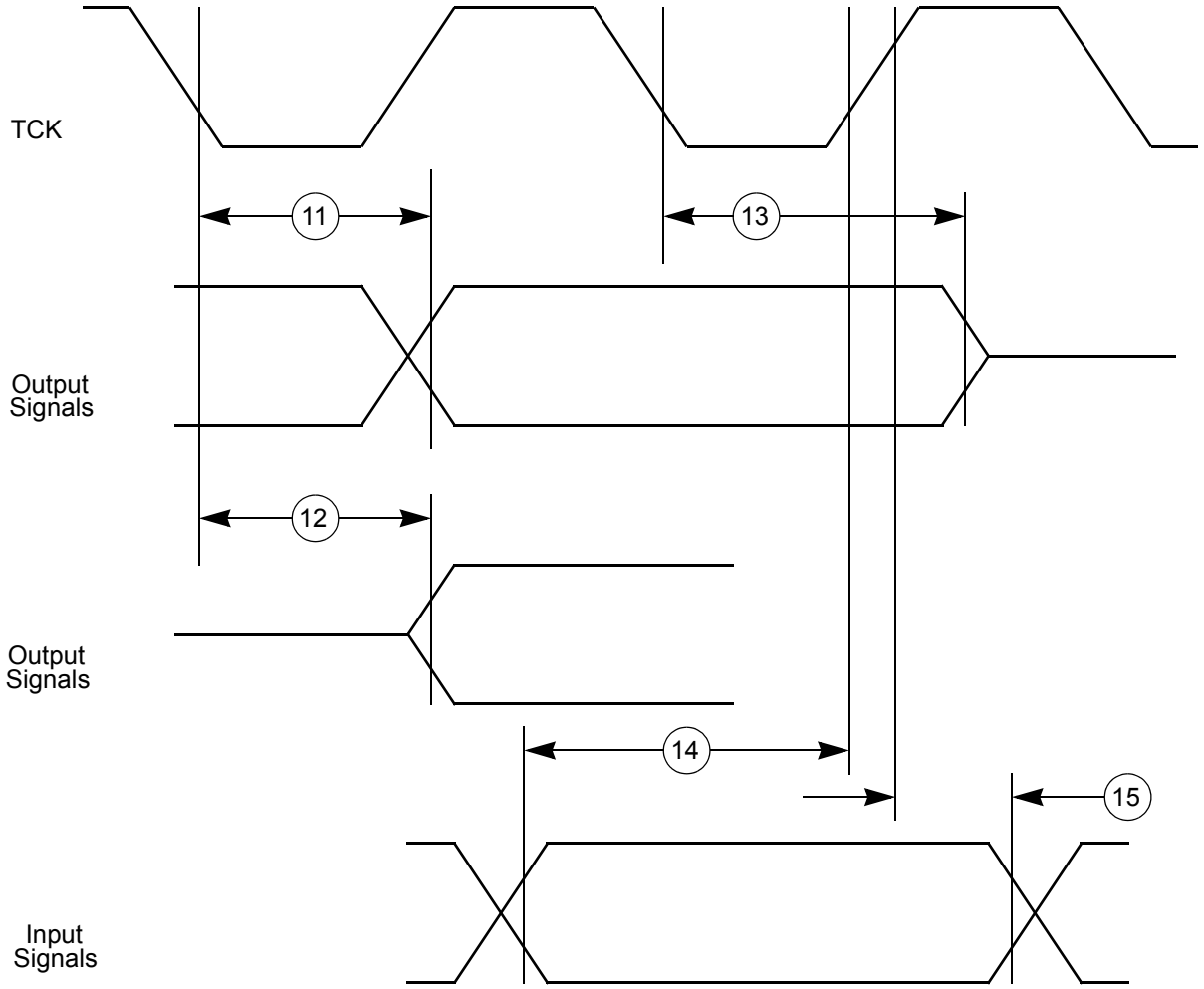


Figure 12. JTAG boundary scan timing

4.16.2 Nexus timing

Table 37. Nexus debug port timing[1]

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
1	t_{MCYC}	CC	D	MCKO Cycle Time	2[2,3]	8	t_{CYC}
1a	t_{MCYC}	CC	D	Absolute Minimum MCKO Cycle Time	100[4]	—	ns
2	t_{MDC}	CC	D	MCKO Duty Cycle	40	60	%
3	t_{MDOV}	CC	D	MCKO Low to MDO Data Valid[5]	– 0.1	0.2	t_{MCYC}
4	t_{MSEOV}	CC	D	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[5]	0.1	0.2	t_{MCYC}
6	t_{EVTOV}	CC	D	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[5]	– 0.1	0.2	t_{MCYC}
7	t_{EVTIPW}	CC	D	$\overline{\text{EVTI}}$ Pulse Width	4.0	—	t_{TCYC}
8	t_{EVTOPW}	CC	D	$\overline{\text{EVTO}}$ Pulse Width	1	—	t_{MCYC}

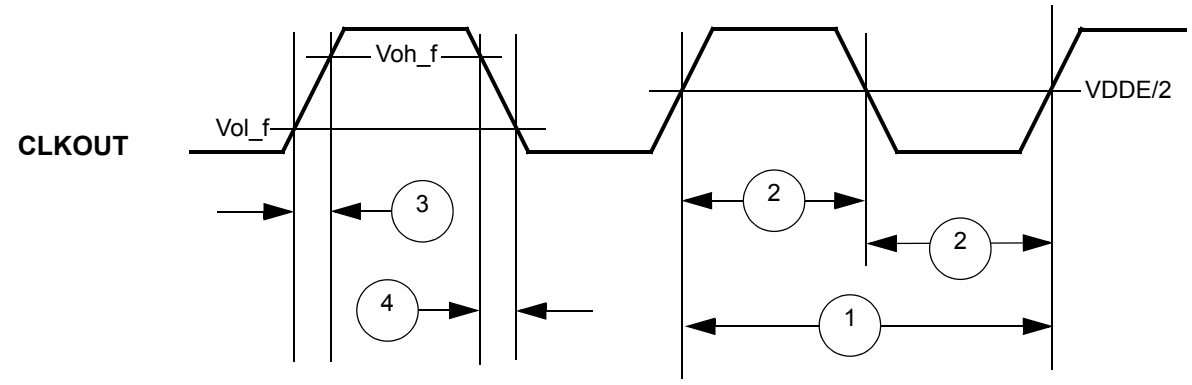


Figure 16. CLKOUT timing

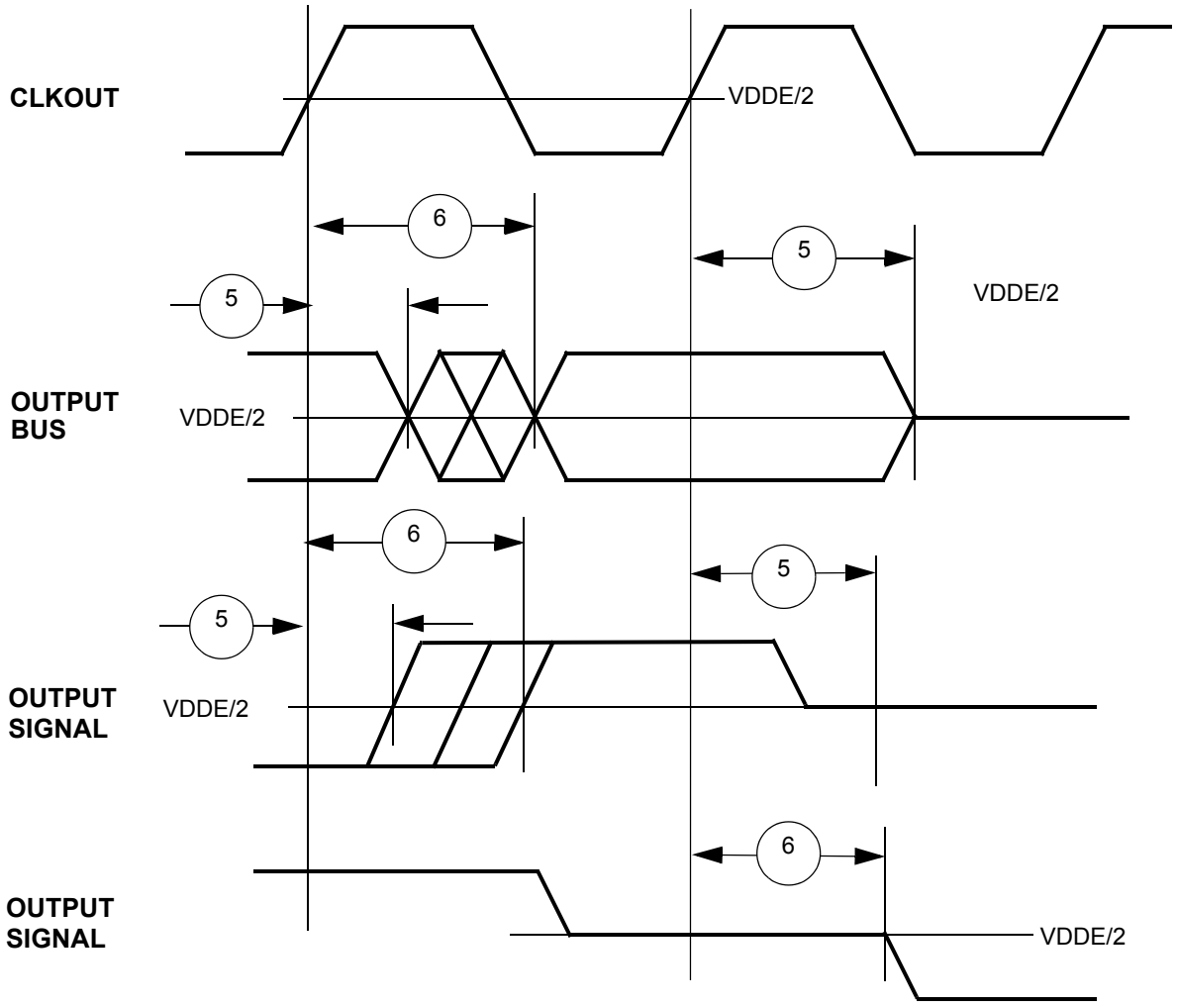
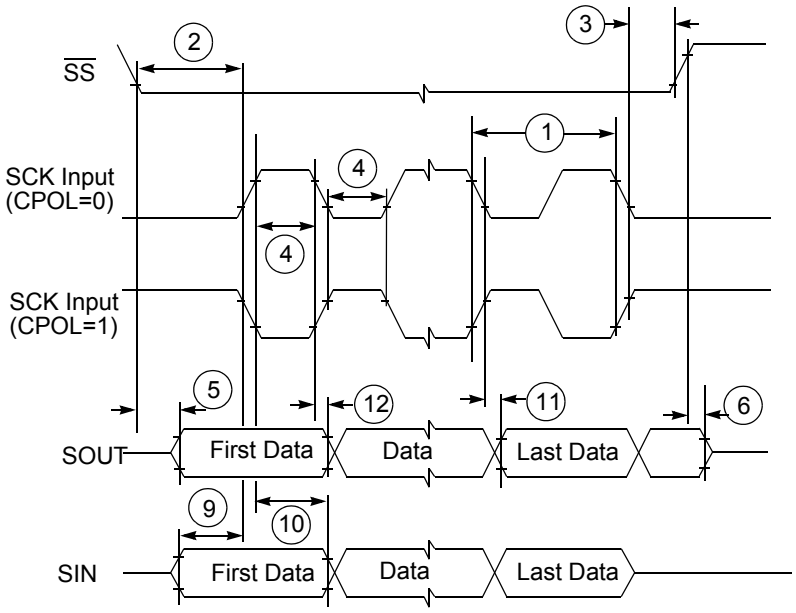
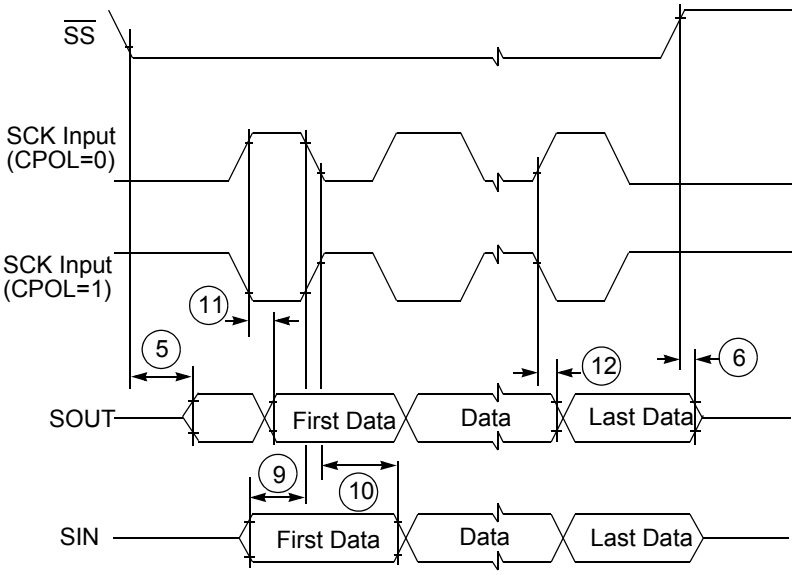


Figure 17. Synchronous output timing



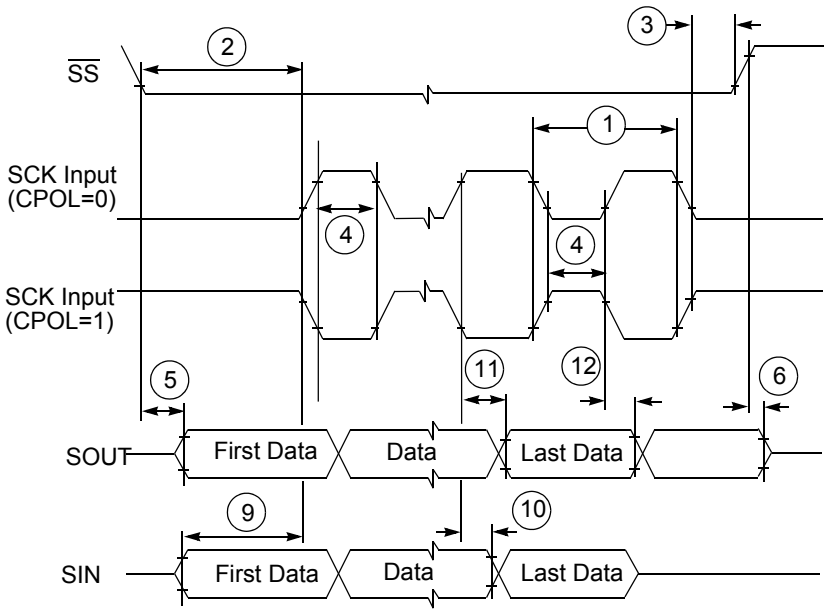
These numbers reference Table 40.

Figure 22. DSPI classic SPI timing – slave, CPHA = 0



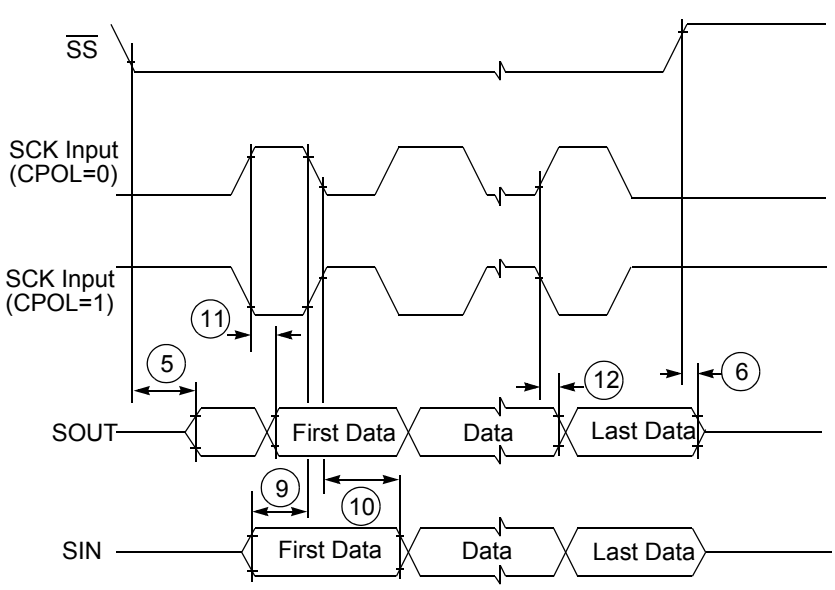
These numbers reference Table 40.

Figure 23. DSPI classic SPI timing – slave, CPHA = 1



These numbers reference Table 40.

Figure 26. DSPI modified transfer format timing – slave, CPHA =0



These numbers reference Table 40.

Figure 27. DSPI modified transfer format timing – slave, CPHA =1

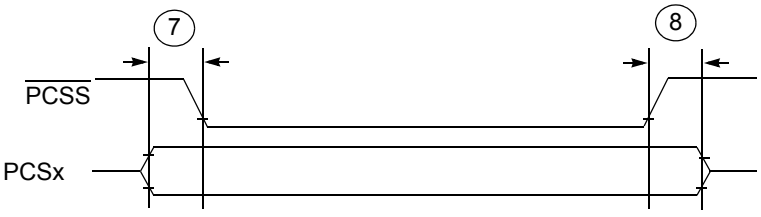


Figure 28. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

NOTES:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THEN 0.08MM. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07MM FOR 0.4MM AND 0.5MM PITCH PACKAGES.

DIM	MIN	NOM	MAX
A	---		1.6
A1	0.05		0.15
A2	1.35	1.4	1.45
b	0.17	0.22	0.27
b1	0.17	0.2	0.23
c	0.09		0.2
c1	0.09		0.16
D		26 BSC	
D1		24 BSC	
e		0.5 BSC	
E		26 BSC	
E1		24 BSC	
L	0.45	0.6	0.75

DIM	MIN	NOM	MAX
L1		1 REF	
R1	0.08		---
R2	0.08		0.2
S		0.2 REF	
θ	0°	3.5°	7°
θ1	0°		---
θ2	11°	12°	13°
θ3	11°	12°	13°

DIM	MIN	NOM	MAX

UNIT	DIMENSION AND TOLERANCES	REFERANCE DOCUMENT
MM	ASME Y14.5M	64-06-280-1392

TITLE:	COMPANY	ASECL
LQFP 176LD 24X24X1.4 PKG 0.5 PITCH POD 2mm FOOTPRINT	SHEET	3

Figure 35. 176 LQFP package mechanical drawing (part 3)

Table 43. Revision history (continued)

Revision	Date	Description of Changes
Rev.4	12/2009	208-pin MAPBGA ballmap for the MPC5633M (1024 KB flash memory) has changed. Power Management Control (PMC) and Power On Reset (POR) electrical specifications updated Temperature sensor data added Specifications now indicate how each controller characteristic parameter is guaranteed. I/O pad current specifications updated I/O Pad VRC33 current specifications updated PAD AC characteristics updated VGA gain specifications added to eQADC electrical characteristics DC electrical specifications updated: • Footnote added to RPUPD100K and RPUPD200K: When the pull-up and pull-down of the same nominal 200 KΩ or 100 KΩ value are both enabled, assuming no interference from other devices, the resulting pad voltage will be 0.5*VDDE ± 2.5% • I_{OL} condition added to V_{OL_LS}. • I_{OH} condition added to V_{OH_LS}. • Minimum V_{OH_LS} is 2.3 V (was 2.7 V). • Separate I_{DDPLL} removed from I_{DD} spec because we can only measure I_{DD} + I_{DDPLL}. I_{DD} increased by 15 mA (to 195 mA) to account for I_{DDPLL}. I_{DD} now documented as I_{DD} + I_{DDPLL}. Footnote added detailing runtime configuration used to measure I_{DD} + I_{DDPLL}. • Specifications for I_{DDSTBY} and $I_{DDSTBY150}$ reformatted to make more clear. • V_{STBY} is now specified by two ranges. The area in between those ranges is indeterminate. LVDS pad specifications updated: • Min value for V_{OD} at SRC=0b01 is 90 mV (was 120); and 160 mV (was 180) at SRC = 0b10 Changes to Signal Properties table: • VDDE7 removed as voltage segment from Calibration bus pins. Calibration bus pins are powered by VDDE12 only. • GPIO[139] and GPIO[87] pins changed to Medium pads • Some signal names have changed on 176-pin QFP package pinout: “CAL_x” signals renamed to “ALT_x”. Changes to Pad Types table: • Column heading changed from “Voltage” to “Supply Voltage” • MultiV pad high swing mode voltage changed to 3.0 V – 5.25 V (was 4.5 V – 5.25 V) • MultiV pad low swing mode voltage changed to 4.5 V – 5.25 V (was 3.0 V – 3.6 V) Signal details table added Power/ground segmentation table added 100-pin package is no longer available

Table 43. Revision history (continued)

Revision	Date	Description of Changes
Rev. 5 (cont.)	04/2010	Changes to flash memory specifications: • T_{BKPRG} 64 KB specification removed (not present in this device) • $T_{64kpperase}$ specification added • Flash module life P/E spec for 32 Kbyte blocks also applies to 64 Kbyte blocks Pad AC specifications (3.3 V) table updated
Rev. 6	04/2010	"Core Voltage Regulator Controller External Components Preferred Configuration" circuit diagram updated. • Clarification added to note: Emitter and collector capacitors (6.8 μF and 10 μF) should be matched (same type) and ESR should be lower than 200 mW. (Added emphasis that only 6.8 μF emitter capacitors need to be matched with collector capacitor. • 220 μF emitter capacitors changed to 220 nF.
Rev. 7	4/2010	No specification or product information changes: • Mechanical outline drawings section renamed to "Packages" and restructured. •
Rev. 8	01/2011	Removed the 208 BGA package from the device-summary table. Revised the "PMC Operating conditions and external regulators supply voltage" table. Revised the "PMC electrical characteristics" table. Revised the pad AC specifications. Revised the "DC electrical specifications" table. Revised the "DSPI LVDS pad specification" table: Revised the "PLLMRFM electrical specifications" table. Change to "Temperature sensor electrical characteristics" table: • Accuracy is guaranteed by production test Revised the "eQADC conversion specifications (operating)" table. Changes to "Calibration bus operation timing" table: • CLKOUT period is guaranteed by production test. All other parameters are guaranteed by design Changes to "Program and erase specifications" table in "Flash memory electrical characteristics" section. • Deleted Bank Program (512KB) (T_{BKPRG}) parameter • TYP P/E values added for 32- and 64 KB blocks and for 128 KB blocks. Changes to Recommended operating characteristics for external power transistor: • VCESAT should be between 200 and 600 mV • VBE should be 0.4V to 1.0V Removed footnote 8 from Vddeh in Maximum ratings. Deleted engineering names for pads in Power UP/DOWN Sequencing Section Changed "sin_c" to DSPI_C_SIN" and "sck_c" to DSPI_C_SCK" on 144 pin LQFP package. Updated the "Electromagnetic Interference Characteristics" table to reflect new parameter levels, test conditions. In the "APC, RWSC, WWSC settings vs. frequency of operation" table, changed 82 MHz entry for WWC from "11" to "01", added an extra row for "All 111 111 11"