Infineon Technologies - XMC1100T016X0016ABXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	11
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-16-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1100t016x0016abxuma1

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1 Summary of Features

The XMC1100 devices are members of the XMC™1000 Family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC1100 series devices are designed for general purpose applications.

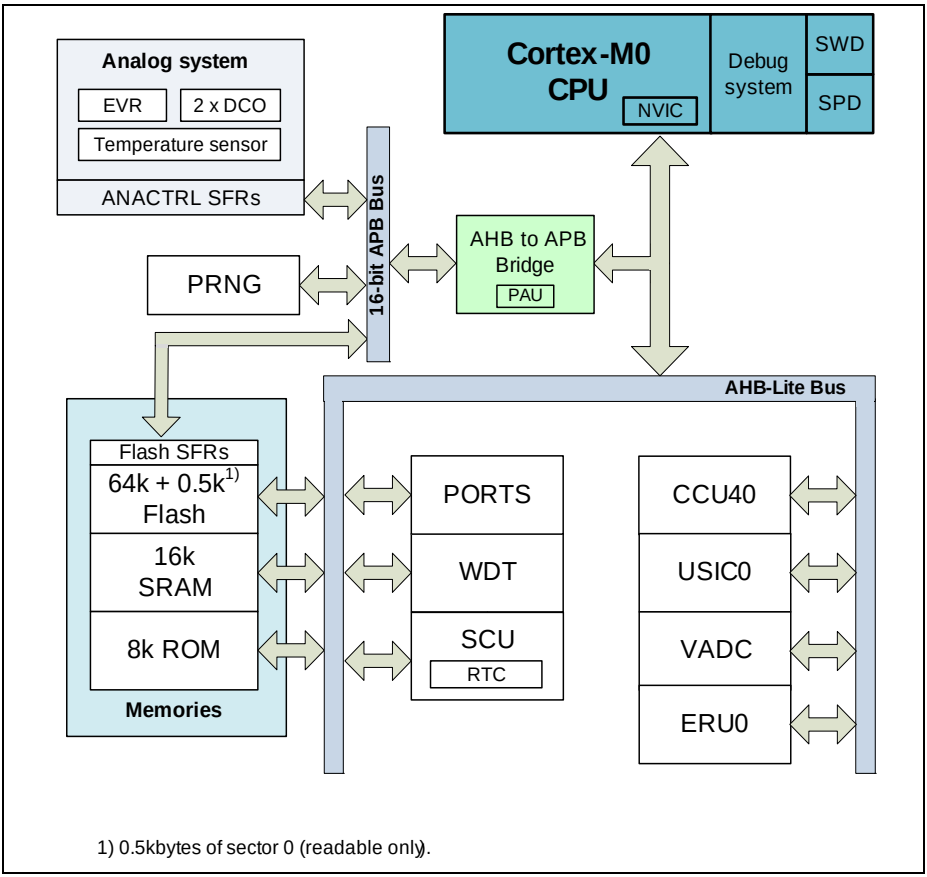


Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High-performance 32-bit ARM Cortex-M0 CPU
  - Most 16-bit Thumb and subset of 32-bit Thumb2 instruction set
  - Single cycle 32-bit hardware multiplier

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

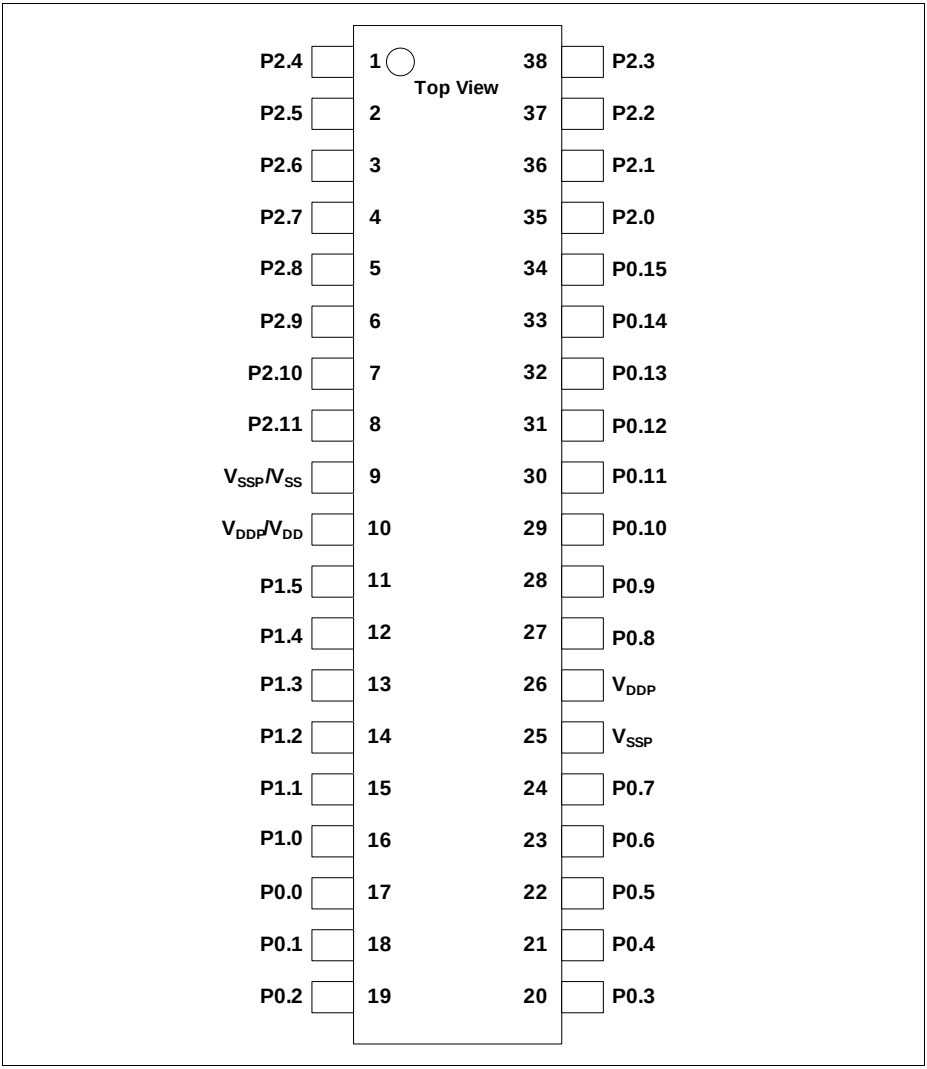


Figure 4 XMC1100 PG-TSSOP-38 Pin Configuration (top view)

Table 9 Port I/O Functions

Function	Outputs							Inputs						
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU0.PDOUT0		ERU0.GOUT0	CCU40.OUT0		USIC0_CH0.SELO0	USIC0_CH1.SELO0	CCU40.IN0C				USIC0_CH0.DX2A	USIC0_CH1.DX2A	
P0.1	ERU0.PDOUT1		ERU0.GOUT1	CCU40.OUT1			SCU.VDROP	CCU40.IN1C						
P0.2	ERU0.PDOUT2		ERU0.GOUT2	CCU40.OUT2		VADC0.EMUX02		CCU40.IN2C						
P0.3	ERU0.PDOUT3		ERU0.GOUT3	CCU40.OUT3		VADC0.EMUX01		CCU40.IN3C						
P0.4				CCU40.OUT1		VADC0.EMUX00	WWDT.SERVICE_OUT							
P0.5				CCU40.OUT0										
P0.6				CCU40.OUT0		USIC0_CH1.MCLKOUT	USIC0_CH1.DOUT0	CCU40.IN0B				USIC0_CH1.DX0C		
P0.7				CCU40.OUT1		USIC0_CH0.SCLKOUT	USIC0_CH1.DOUT0	CCU40.IN1B				USIC0_CH0.DX1C	USIC0_CH1.DX0D	USIC0_CH1.DX1C
P0.8				CCU40.OUT2		USIC0_CH0.SCLKOUT	USIC0_CH1.SCLKOUT	CCU40.IN2B				USIC0_CH0.DX1B	USIC0_CH1.DX1B	
P0.9				CCU40.OUT3		USIC0_CH0.SELO0	USIC0_CH1.SELO0	CCU40.IN3B				USIC0_CH0.DX2B	USIC0_CH1.DX2B	
P0.10						USIC0_CH0.SELO1	USIC0_CH1.SELO1					USIC0_CH0.DX2C	USIC0_CH1.DX2C	
P0.11				USIC0_CH0.MCLKOUT		USIC0_CH0.SELO2	USIC0_CH1.SELO2					USIC0_CH0.DX2D	USIC0_CH1.DX2D	
P0.12						USIC0_CH0.SELO3		CCU40.IN0A	CCU40.IN1A	CCU40.IN2A	CCU40.IN3A	USIC0_CH0.DX2E		
P0.13	WWDT.SERVICE_OUT					USIC0_CH0.SELO4						USIC0_CH0.DX2F		
P0.14						USIC0_CH0.DOUT0	USIC0_CH0.SCLKOUT					USIC0_CH0.DX0A	USIC0_CH0.DX1A	
P0.15						USIC0_CH0.DOUT0	USIC0_CH1.MCLKOUT					USIC0_CH0.DX0B		
P1.0		CCU40.OUT0					USIC0_CH0.DOUT0					USIC0_CH0.DX0C		

3 Electrical Parameter

This section provides the electrical parameter which are implementation-specific for the XMC1100.

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XMC1100 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the XMC1100 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC1100 is designed in.

If a pin current is outside of the **Operating Conditions** but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 12 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV} SR	-5	–	5	mA	
Absolute sum of all input circuit currents during overload condition	I_{OVS} SR	–	–	25	mA	

Figure 9 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

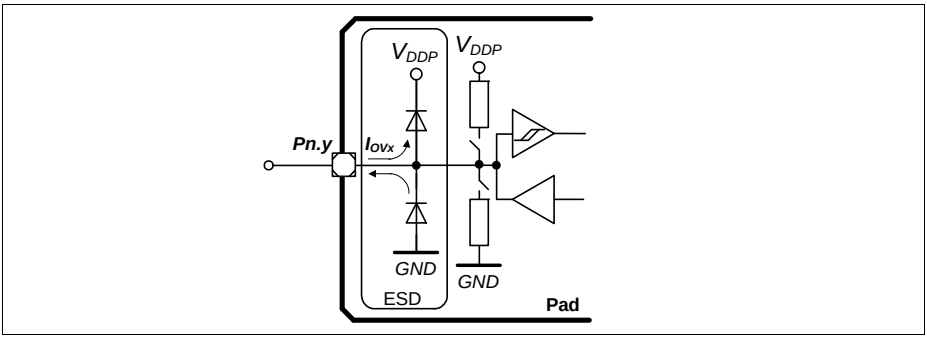


Figure 9 Input Overload Current via ESD structures

Table 13 and **Table 14** list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the **Absolute Maximum Ratings** must not be exceeded during overload.

Table 13 PN-Junction Characterisitics for positive Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 115 °C
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{DDP}$ + 0.5 V	$V_{IN} = V_{DDP}$ + 0.5 V

Table 14 PN-Junction Characterisitics for negative Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 115 °C
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{SS}$ - 0.5 V	$V_{IN} = V_{SS}$ - 0.5 V

3.1.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC1100. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 15 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	85	°C	Temp. Range F
		-40	–	105	°C	Temp. Range X
Digital supply voltage[1)]	V_{DDP} SR	1.8	–	5.5	V	
MCLK Frequency	f_{MCLK} CC	–	–	33.2	MHz	CPU clock
PCLK Frequency	f_{PCLK} CC	–	–	66.4	MHz	Peripherals clock
Short circuit current of digital outputs	I_{SC} SR	-5	–	5	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D} SR	–	–	25	mA	

1) See also the Supply Monitoring thresholds, **Chapter 3.3.2**.

3.2 DC Parameters

3.2.1 Input/Output Characteristics

Table 16 provides the characteristics of the input/output pins of the XMC1100.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Unless otherwise stated, input DC and AC characteristics, including peripheral timings, assume that the input pads operate with the standard hysteresis.

Table 16 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Output low voltage on port pins (with standard pads)	V_{OLP}	CC	–	1.0	V	I_{OL} = 11 mA (5 V) I_{OL} = 7 mA (3.3 V)
			–	0.4	V	I_{OL} = 5 mA (5 V) I_{OL} = 3.5 mA (3.3 V)
Output low voltage on high current pads	V_{OLP1}	CC	–	1.0	V	I_{OL} = 50 mA (5 V) I_{OL} = 25 mA (3.3 V)
			–	0.32	V	I_{OL} = 10 mA (5 V)
			–	0.4	V	I_{OL} = 5 mA (3.3 V)
Output high voltage on port pins (with standard pads)	V_{OHP}	CC	V_{DDP} - 1.0	–	V	I_{OH} = -10 mA (5 V) I_{OH} = -7 mA (3.3 V)
			V_{DDP} - 0.4	–	V	I_{OH} = -4.5 mA (5 V) I_{OH} = -2.5 mA (3.3 V)
Output high voltage on high current pads	V_{OHP1}	CC	V_{DDP} - 0.32	–	V	I_{OH} = -6 mA (5 V)
			V_{DDP} - 1.0	–	V	I_{OH} = -8 mA (3.3 V)
			V_{DDP} - 0.4	–	V	I_{OH} = -4 mA (3.3 V)
Input low voltage on port pins (Standard Hysteresis)	V_{ILPS}	SR	–	0.19 × V_{DDP}	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input high voltage on port pins (Standard Hysteresis)	V_{IHPS}	SR	0.7 × V_{DDP}	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)

8) Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

9) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.

10) However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

3.2.2 Analog to Digital Converters (ADC)

Table 17 shows the Analog to Digital Converter (ADC) characteristics.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 17 ADC Characteristics (Operating Conditions apply)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage range (internal reference)	V_{DD_int} SR	2.0	–	3.0	V	SHSCFG.AREF = 11_B CALCTR.CALGNSTC = $0C_H$
		3.0	–	5.5	V	SHSCFG.AREF = 10_B
Supply voltage range (external reference)	V_{DD_ext} SR	3.0	–	5.5	V	SHSCFG.AREF = 00_B
Analog input voltage range	V_{AIN} SR	V_{SSP} - 0.05	–	V_{DDP} + 0.05	V	
Auxiliary analog reference ground	V_{REFGND} SR	V_{SSP} - 0.05	–	1.0	V	G0CH0
Internal reference voltage (full scale value)	V_{REFINT} CC	5			V	
Switched capacitance of an analog input	C_{AINS} CC	–	1.2	2	pF	GNCTRxz.GAINy = 00_B (unity gain)
		–	1.2	2	pF	GNCTRxz.GAINy = 01_B (gain g1)
		–	4.5	6	pF	GNCTRxz.GAINy = 10_B (gain g2)
		–	4.5	6	pF	GNCTRxz.GAINy = 11_B (gain g3)
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	

Table 17 ADC Characteristics (Operating Conditions apply)[1)] (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain settings	G_{IN} CC		1		–	GNCTRxz.GAINy = 00_B (unity gain)
			3		–	GNCTRxz.GAINy = 01_B (gain g1)
			6		–	GNCTRxz.GAINy = 10_B (gain g2)
			12		–	GNCTRxz.GAINy = 11_B (gain g3)
Sample Time	t_{sample} CC	4	–	–	1 / f_{ADC}	V_{DD} = 5.0 V
		4	–	–	1 / f_{ADC}	V_{DD} = 3.3 V
		30	–	–	1 / f_{ADC}	V_{DD} = 2.0 V
Sigma delta loop hold time	t_{SD_hold} CC	20	–	–	µs	Residual charge stored in an active sigma delta loop remains available
Conversion time in fast compare mode	t_{CF} CC		9		1 / f_{ADC}	[2)]
Conversion time in 12-bit mode	t_{C12} CC		20		1 / f_{ADC}	[2)]
Maximum sample rate in 12-bit mode [3)]	f_{C12} CC	–	–	f_{ADC} / 43.5	–	1 sample pending
		–	–	f_{ADC} / 63.5	–	2 samples pending
Conversion time in 10-bit mode	t_{C10} CC		18		1 / f_{ADC}	[2)]
Maximum sample rate in 10-bit mode [3)]	f_{C10} CC	–	–	f_{ADC} / 41.5	–	1 sample pending
		–	–	f_{ADC} / 59.5	–	2 samples pending
Conversion time in 8-bit mode	t_{C8} CC		16		1 / f_{ADC}	[2)]

Table 17 ADC Characteristics (Operating Conditions apply)[1] (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum sample rate in 8-bit mode [3]	f_{C8} CC	–	–	f_{ADC} / 38.5	–	1 sample pending
		–	–	f_{ADC} / 54.5	–	2 samples pending
RMS noise [4]	EN_{RMS} CC	–	1.5	–	LSB 12	DC input, V_{DD} = 5.0 V, V_{AIN} = 2.5 V, 25°C
DNL error	EA_{DNL} CC	–	±2.0	–	LSB 12	
INL error	EA_{INL} CC	–	±4.0	–	LSB 12	
Gain error with external reference	EA_{GAIN} CC	–	±0.5	–	%	SHSCFG.AREF = 00_B (calibrated)
Gain error with internal reference [5]	EA_{GAIN} CC	–	±3.6	–	%	SHSCFG.AREF = $1X_B$ (calibrated), -40°C - 105°C
		–	±2.0	–	%	SHSCFG.AREF = $1X_B$ (calibrated), 0°C - 85°C
Offset error	EA_{OFF} CC	–	±8.0	–	mV	Calibrated, V_{DD} = 5.0 V

1) The parameters are defined for ADC clock frequency f_{SH} = 32MHz.

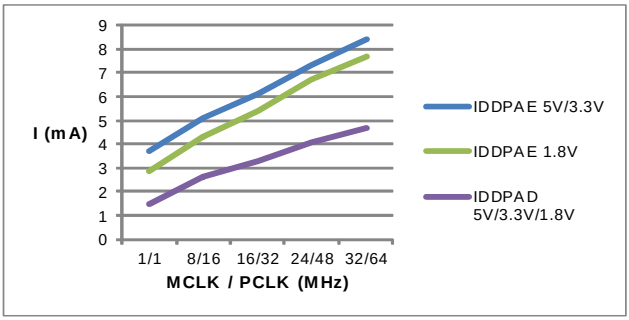
2) No pending samples assumed, excluding sampling time and calibration.

3) Includes synchronization and calibration (average of gain and offset calibration).

4) This parameter can also be defined as an SNR value: SNR[dB] = 20 × log(A_{MAXeff} / N_{RMS}).
With $A_{MAXeff} = 2^N / 2$, SNR[dB] = 20 × log (2048 / N_{RMS}) [N = 12].
N_{RMS} = 1.5 LSB12, therefore, equals SNR = 20 × log (2048 / 1.5) = 62.7 dB.

5) Includes error from the reference voltage.

Figure 11 shows typical graphs for active mode supply current for V_{DDP} = 5V, V_{DDP} = 3.3V, V_{DDP} = 1.8V across different clock frequencies.



Condition:
1. TA = +25° C

Figure 11 Active mode, a) peripherals clocks enabled, b) peripherals clocks disabled: Supply current I_{DDPA} over supply voltage V_{DDP} for different clock frequencies

Figure 17 shows the typical curves for the accuracy of DCO1, with and without calibration based on temperature sensor, respectively.

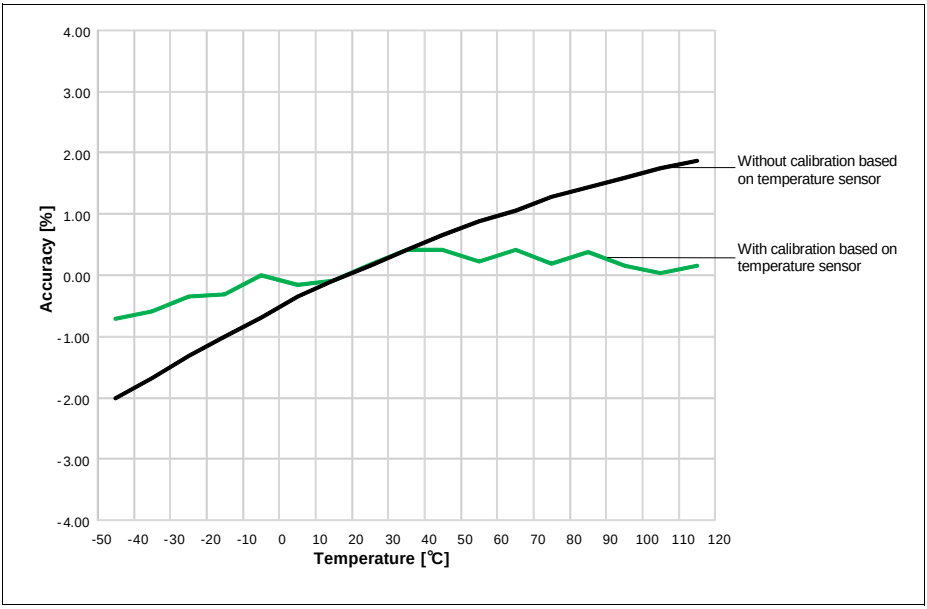


Figure 17 Typical DCO1 accuracy over temperature

Table 24 provides the characteristics of the 32 kHz clock output from digital controlled oscillators, DCO2 in XMC1100.

Table 24 32 kHz DCO2 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	–	32.75	–	kHz	under nominal conditions[1] after trimming
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0 °C to 85 °C)
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

3.3.5 SPD Timing Requirements

The optimum SPD decision time between 0_B and 1_B is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

Table 26 Optimum Number of Sample Clocks for SPD

Sample Freq.	Sampling Factor	Sample Clocks 0_B	Sample Clocks 1_B	Effective Decision Time[1)]	Remark
8 MHz	4	1 to 5	6 to 12	0.69 µs	The other closest option (0.81 µs) for the effective decision time is less robust.

1) Nominal sample frequency period multiplied with 0.5 + (max. number of 0_B sample clocks)

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

Table 28 USIC SSC Slave Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DX1 slave clock period	t_{CLK}	SR	125	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge[1]	t_{10}	SR	10	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1]	t_{11}	SR	10	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1]	t_{12}	SR	10	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1]	t_{13}	SR	10	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	-	–	80	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

Table 30 USIC IIC Fast Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1*C_b	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

4 Package and Reliability

The XMC1100 is a member of the XMC™1000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 33 provides the thermal characteristics of the packages used in XMC1100.

Table 33 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	2.7 × 2.7	mm	PG-VQFN-24-19
		-	3.7 × 3.7	mm	PG-VQFN-40-13
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	104.6	K/W	PG-TSSOP-16-8[1)]
		-	70.3	K/W	PG-TSSOP-38-9[1)]
		-	46.0	K/W	PG-VQFN-24-19[1)]
		-	38.4	K/W	PG-VQFN-40-13[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SSP}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC1100 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115 °C.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

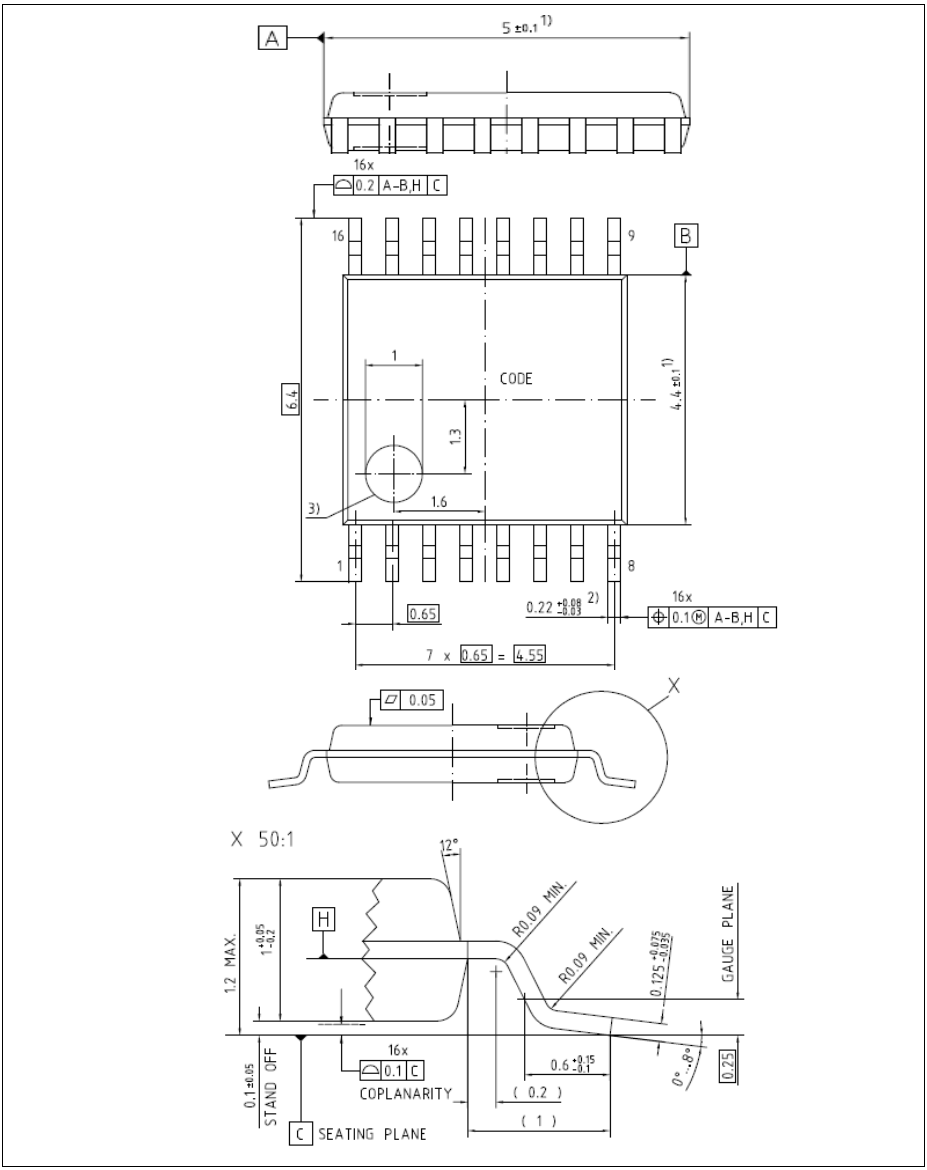


Figure 24 PG-TSSOP-16-8