Infineon Technologies - TC1766192F80HLBDKXUMA1 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	ASC, CANbus, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	81
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	108K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 2x10b, 32x8b/10b/12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	PG-LQFP-176-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1766192f80hlbdkxuma1

2.3 Pin Configuration

Figure 2-3 shows the TC1766 pin configuration.

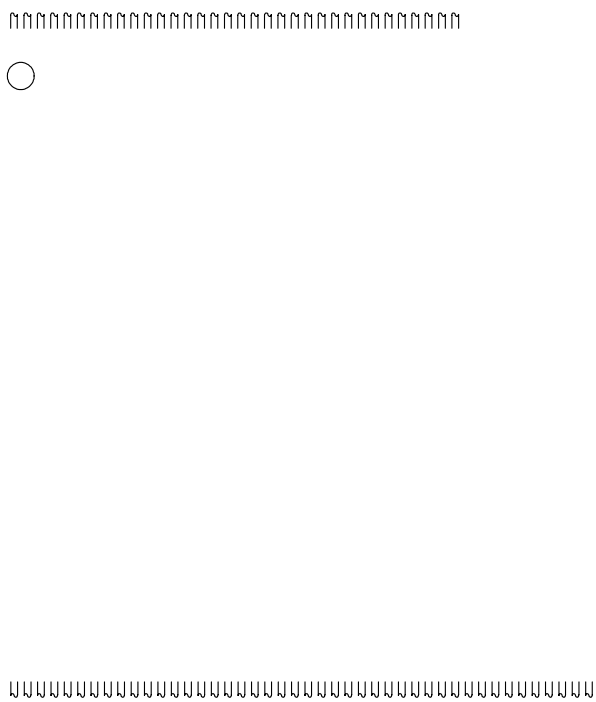

Figure 2-3 TC1766 Pinning for PG-LQFP-176-2 Package

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions	
P2.8	164		A2		SLSO04	SSC0 Slave Select output 4
					SLSO14	SSC1 Slave Select output 4
					EN00	MSC0 enable output 0
P2.9	160		A2		SLSO05	SSC0 Slave Select output 5
					SLSO15	SSC1 Slave Select output 5
					EN01	MSC0 enable output 1
P2.10	161		A2		MRST1A	SSC1 master receive input / slave transmit output A
P2.11	162		A2		SCLK1A	SSC1 clock input/output A
					FCLP0B	MSC0 clock output B
P2.12	163		A2		MTSR1A	SSC1 master transmit out / slave receive input A
					SOP0B	MSC0 serial data output B
P2.13	165		A1		SLSI1	SSC1 slave select input
					SDI0	MSC0 serial data input

4.3.5 Phase Locked Loop (PLL)

Section 4.3.5 provides the characteristics of the PLL parameters and its operation in the TC1766.

Note: All PLL characteristics defined on this and the next page are verified by design characterization.

Table 4-13 PLL Parameters (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit
		Min.	Max.	
Accumulated jitter	D_P	See **Figure 4-12**		–
VCO frequency range	f_{VCO}	400	500	MHz
		500	600	MHz
		600	700	MHz
PLL base frequency[1)]	f_D			

1) The CPU base frequency which is selected after reset is calculated by dividing the limit values by 16 (this is the K factor after reset).

Phase Locked Loop Operation

When PLL operation is enabled and configured, the PLL clock f_{VCO} (and with it the CPU clock f_{CPU}) is constantly adjusted to the selected frequency. The relation between f_{VCO} and f_{SYS} is defined by: $f_{VCO} = K \times f_{CPU}$. The PLL causes a jitter of f_{CPU} and affects the clock outputs TRCLK and SYSCLK (P4.3) which are derived from the PLL clock f_{VCO}.

There are two formulas that define the (absolute) approximate maximum value of jitter D_P in ns dependent on the K-factor, the CPU clock frequency f_{CPU} in MHz, and the number P of consecutive f_{CPU} clock periods.

(4.1)

(4.2)

K : K-Divider Value

P : Number of f_{CPU} periods

D_P : Jitter in ns

f_{CPU} : CPU frequency in MHz

5.3 Flash Memory Parameters

The data retention time of the TC1766's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Table 5-2 Flash Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Program Flash Retention Time, Physical Sector[1)2)]	t_{RET}	20	–	years	Max. 1000 erase/program cycles
Program Flash Retention Time, Logical Sector[1)2)]	t_{RETL}	20	–	years	Max. 50 erase/program cycles
Data Flash Endurance (32 Kbyte)	N_E	15 000	–	–	Max. data retention time 5 years
Data Flash Endurance, EEPROM Emulation (8 × 4 Kbyte)	N_{E8}	120 000	–	–	Max. data retention time 5 years
Programming Time per Page[3)]	t_{PR}	–	5	ms	–
Program Flash Erase Time per 256-Kbyte sector	t_{ERP}	–	5	s	f_{CPU} = 80 MHz
Data Flash Erase Time per 16-Kbyte sector	t_{ERD}	–	0.625	s	f_{CPU} = 80 MHz
Wake-up time	t_{WU}	$4300 \times 1/f_{CPU}$ + 40µs			

1) Storage and inactive time included.

2) At average weighted junction temperature T_J = 100 °C, or
the retention time at average weighted temperature of T_J = 110 °C is minimum 10 years, or
the retention time at average weighted temperature of T_J = 150 °C is minimum 0.7 years.

3) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes additional 5ms.