Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	ASC, CANbus, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	81
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	108K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 2x10b, 32x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	PG-LQFP-176-5
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1766192f80hlbdkxuma2

- – One 2-channel Fast Analog-to-Digital Converter unit (FADC) with concatenated comb filters for hardware data reduction: supporting 10-bit resolution, with minimum conversion time of 262.5ns
- 32 analog input lines for ADC and FADC
- 81 digital general purpose I/O lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 and 2 (CPU, PCP, DMA)
- Dedicated Emulation Device chip for multi-core debugging, tracing, and calibration via USB V1.1 interface available (TC1766ED)
- Power Management System
- Clock Generation Unit with PLL
- Core supply voltage of 1.5 V
- I/O voltage of 3.3 V
- Full automotive temperature range: -40° to +125°C
- PG-LQFP-176-2 package

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions	
P3		I/O		V_{DDP}	**Port 3** Port 3 is a 16-bit bi-directional general-purpose I/O port which can be alternatively used for ASC0/1, SSC0/1 and CAN lines.	
P3.0	136		A2		RXD0A	ASC0 receiver inp./outp. A
P3.1	135		A2		TXD0A	ASC0 transmitter output A
					This pin is sampled at the rising edge of $\overline{\text{PORST}}$. If this pin and the BYPASS input pin are both active, then oscillator bypass mode is entered.	
P3.2	129		A2		SCLK0	SSC0 clock input/output
P3.3	130		A2		MRST0	SSC0 master receive input/ slave transmit output
P3.4	132		A2		MTSR0	SSC0 master transmit output/slave receive input
P3.5	126		A2		SLSO00 SLSO10	SSC0 slave select output 0 SSC1 slave select output 0 [1)]
P3.6	127		A2		SLSO01 SLSO11	SSC0 slave select output 1 SSC1 slave select output 1[1)]
P3.7	131		A2		$\overline{\text{SLSI0}}$ SLSO02 SLSO12	SSC0 slave select input SSC0 slave select output 2 SSC1 slave select output 2
P3.8	128		A2		SLSO06 TXD1A	SSC0 slave select output 6 ASC1 transmitter output A
P3.9	138		A2		RXD1A	ASC1 receiver inp./outp. A
P3.10	137		A1		REQ0	External trigger input 0
P3.11	144		A1		REQ1	External trigger input 1
P3.12	143		A2		RXDCAN0 RXD0B	CAN node 0 receiver input ASC0 receiver inp./outp. B
P3.13	142		A2		TXDCAN0 TXD0B	CAN node 0 transm. output ASC0 transmitter output B
P3.14	134		A2		RXDCAN1 RXD1B	CAN node 1 receiver input ASC1 receiver inp./outp. B
P3.15	133		A2		TXDCAN1 TXD1B	CAN node 1 transm. output ASC1 transmitter output B

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions	
P5		I/O	A2	V_{DDP}	**Port 5** Port 5 is a 16-bit bi-directional general-purpose I/O port. In emulation, it is used as a trace port for OCDS Level 2 debug lines. In normal operation, it is used for GPTA I/O or the MLI0/1 interface.	
P5.0	1				OCDSDBG0 IN40 / OUT40	OCDS L2 Debug Line 0 (Pipeline Status Sig. PS0) line of GPTA
P5.1	2				OCDSDBG1 IN41 / OUT41	OCDS L2 Debug Line 1 (Pipeline Status Sig. PS1) line of GPTA
P5.2	3				OCDSDBG2 IN42 / OUT42	OCDS L2 Debug Line 2 (Pipeline Status Sig. PS2) line of GPTA
P5.3	4				OCDSDBG3 IN43 / OUT43	OCDS L2 Debug Line 3 (Pipeline Status Sig. PS3) line of GPTA
P5.4	5				OCDSDBG4 IN44 / OUT44	OCDS L2 Debug Line 4 (Pipeline Status Sig. PS4) line of GPTA
P5.5	6				OCDSDBG5 IN45 / OUT45	OCDS L2 Debug Line 5 (Break Qualification Line BRK0) line of GPTA
P5.6	7				OCDSDBG6 IN46 / OUT46	OCDS L2 Debug Line 6 (Break Qualification Line BRK1) line of GPTA
P5.7	8				OCDSDBG7 IN47 / OUT47	OCDS L2 Debug Line 7 (Break Qualification Line BRK2) line of GPTA

3 Functional Description

Chapter 3 provides an overview of the TC1766 functional description.

3.1 System Architecture and On-Chip Bus Systems

The TC1766 has two independent on-chip buses (see also TC1766 block diagram on Page 2-6):

- Local Memory Bus (LMB)
- System Peripheral Bus (SPB)

The LMB Bus connects the CPU local resources for data and instruction fetch. The Local Memory Bus interconnects the memory units and functional units, such as CPU and PMU. The main target of the LMB bus is to support devices with fast response times, optimized for speed. This allows the DMI and PMI fast access to local memory and reduces load on the FPI bus. The Tricore system itself is located on LMB bus.

The Local Memory Bus is a synchronous, pipelined, split bus with variable block size transfer support. It supports 8-, 16-, 32- and 64-bit single transactions and variable length 64-bit block transfers.

The SPB Bus is mainly governed by the PCP and is accessible to the CPU via the LMB Bus bridge. The System Peripheral Bus (SPB Bus) in TC1766 is an on-chip FPI Bus. The FPI Bus interconnects the functional units of the TC1766, such as the DMA and on-chip peripheral components. The FPI Bus is designed to be quick to be acquired by on-chip functional units, and quick to transfer data. The low setup overhead of the FPI Bus access protocol guarantees fast FPI Bus acquisition, which is required for time-critical applications.The FPI Bus is designed to sustain high transfer rates. For example, a peak transfer rate of up to 320 Mbyte/s can be achieved with a 80 MHz bus clock and 32-bit data bus. Multiple data transfers per bus arbitration cycle allow the FPI Bus to operate at close to its peak bandwidth.

Both the LMB Bus and the SPB Bus runs at full CPU speed. The maximum CPU speed is 80 MHz.

Additionally, two simplified bus interfaces are connected to and controlled by the DMA Controller:

- DMA Bus
- SMIF Interface

3.6 DMA Controller and Memory Checker

The DMA Controller of the TC1766 transfers data from data source locations to data destination locations without intervention of the CPU or other on-chip devices. One data move operation is controlled by one DMA channel. Eight DMA channels are provided in one DMA Sub-Block. The Bus Switch provides the connection of the DMA Sub-Block to the two FPI Bus interfaces and an MLI bus interface. In the TC1766, the FPI Bus interfaces are connected to the System Peripheral Bus and the DMA Bus. The third specific bus interface provides a connection to Micro Link Interface modules (two MLI modules in the TC1766) and other DMA-related devices (Memory Checker module in the TC1766). Clock control, address decoding, DMA request wiring, and DMA interrupt service request control are implementation-specific and managed outside the DMA controller kernel. Figure 3-2 shows the implementation details and interconnections of the DMA module.

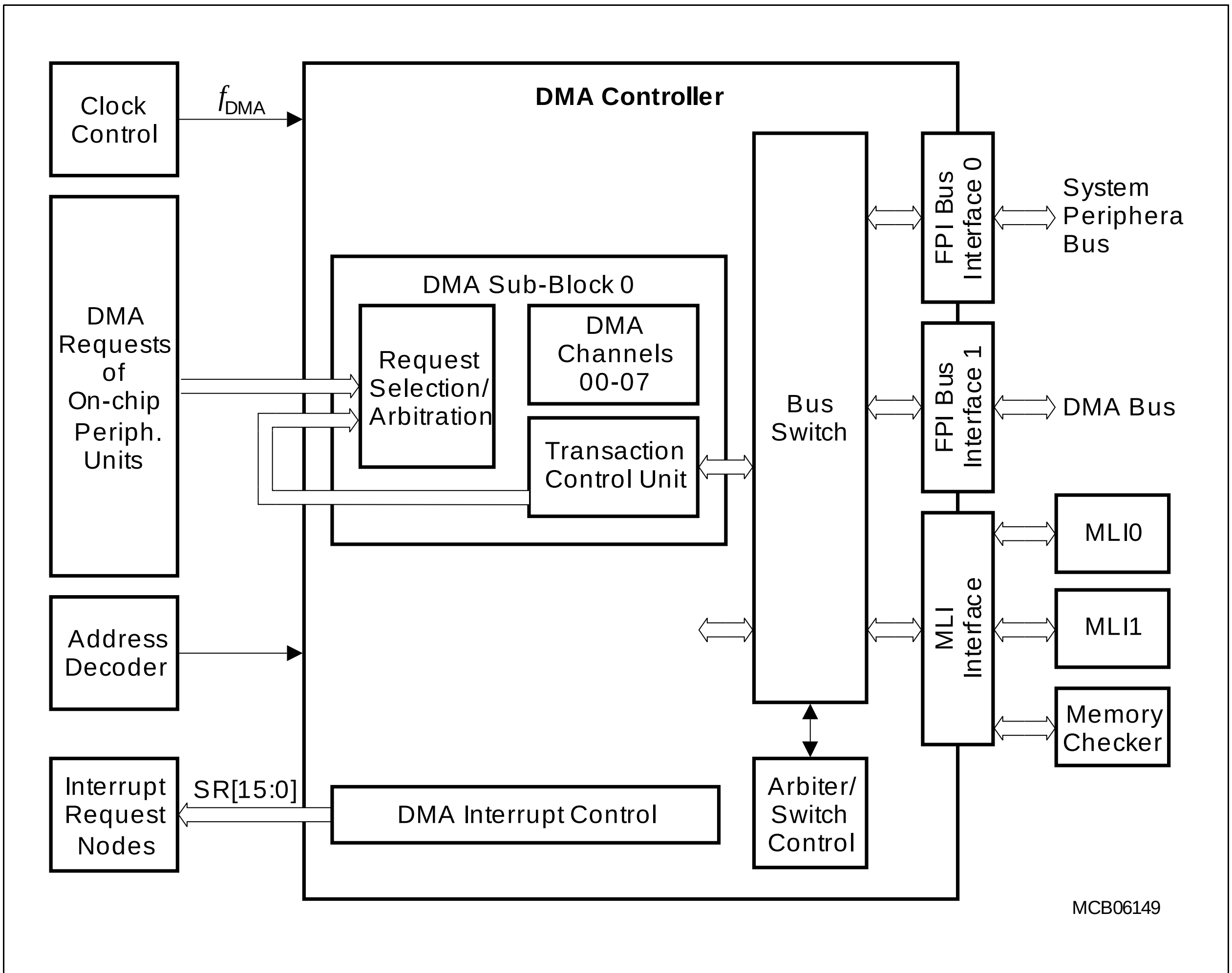

Figure 3-2 DMA Controller Block Diagram

3.8 Asynchronous/Synchronous Serial Interfaces (ASC0, ASC1)

Figure 3-4 shows a global view of the functional blocks and interfaces of the two Asynchronous/Synchronous Serial Interfaces, ASC0 and ASC1.

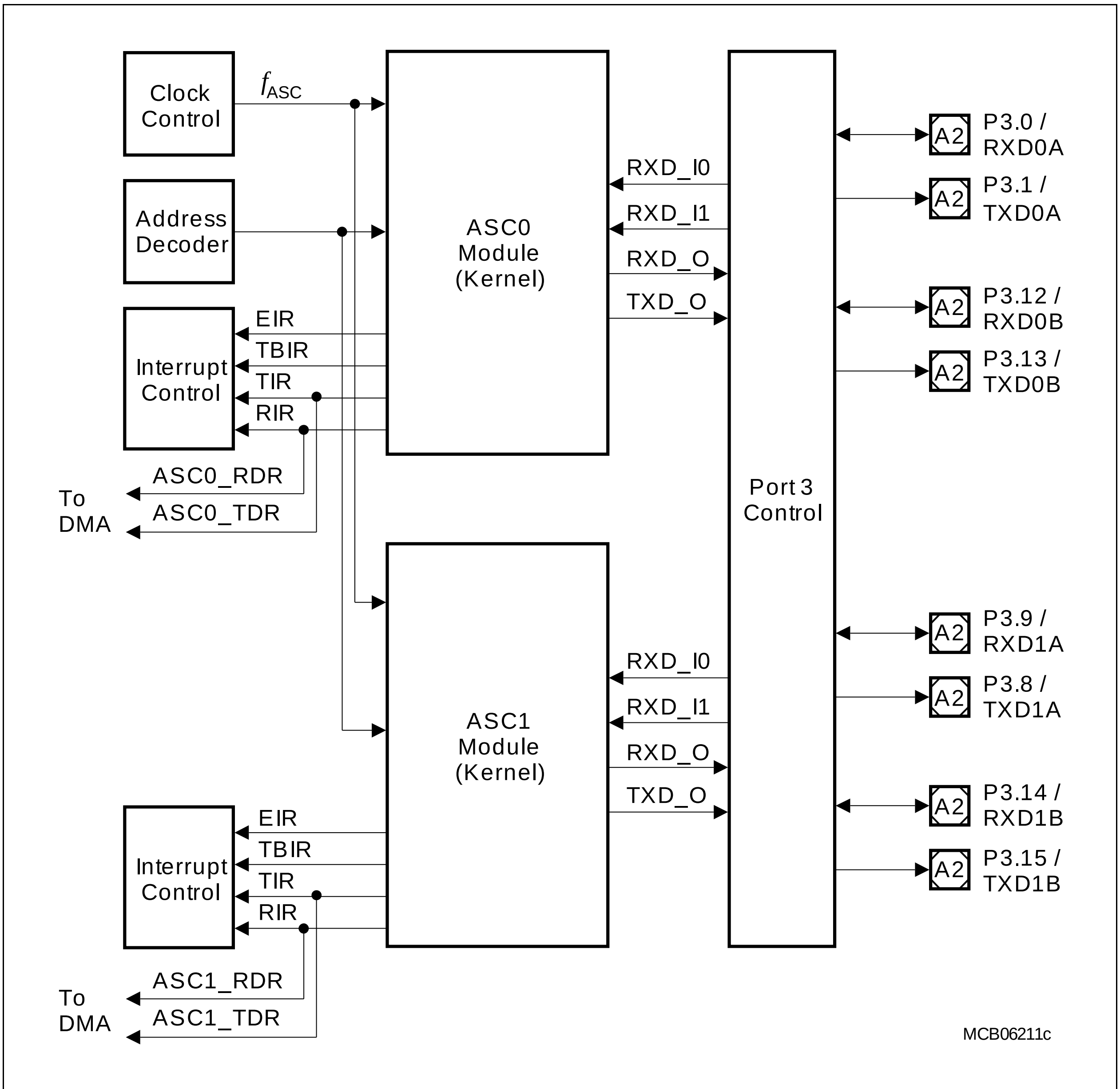

Figure 3-4 Block Diagram of the ASC Interfaces

The ASC provides serial communication between the TC1766 and other microcontrollers, microprocessors, or external peripherals.

The ASC supports full-duplex asynchronous communication and half-duplex synchronous communication. In Synchronous Mode, data is transmitted or received synchronous to a shift clock that is generated by the ASC internally. In Asynchronous Mode, 8-bit or 9-bit data transfer, parity generation, and the number of stop bits can be selected. Parity, framing, and overrun error detection are provided to increase the reliability of data transfers. Transmission and reception of data is double-buffered. For multiprocessor communication, a mechanism is included to distinguish address bytes from data bytes. Testing is supported by a loop-back option. A 13-bit baud rate generator provides the ASC with a separate serial clock signal, which can be accurately adjusted by a prescaler implemented as fractional divider.

Features

- Full-duplex asynchronous operating modes
  - 8-bit or 9-bit data frames, LSB first
  - Parity-bit generation/checking
  - One or two stop bits
  - Baud rate from 5.0 Mbit/s to 1.19 bit/s (@ 80 MHz module clock)
  - Multiprocessor mode for automatic address/data byte detection
  - Loop-back capability
- Half-duplex 8-bit synchronous operating mode
  - Baud rate from 10.0 Mbit/s to 813.8 bit/s (@ 80 MHz module clock)
- Double-buffered transmitter/receiver
- Interrupt generation
  - On a transmit buffer empty condition
  - On a transmit last bit of a frame condition
  - On a receive buffer full condition
  - On an error condition (frame, parity, overrun error)

MultiCAN Features

- CAN functionality conforms to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Two independent CAN nodes
- 64 independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality: message objects can be individually
  – assigned to one of the two CAN nodes
  – configured as transmit or receive object
  – configured as message buffer with FIFO algorithm
  – configured to handle frames with 11-bit or 29-bit identifiers
  – provided with programmable acceptance mask register for filtering
  – monitored via a frame counter
  – configured for Remote Monitoring Mode
- Automatic Gateway Mode support
- 6 individually programmable interrupt nodes
- CAN analyzer mode for bus monitoring

- Duty Cycle Measurement (DCM)
  – Four independent units
  – 0 - 100% margin and time-out handling
  – f_{GPTA} maximum resolution
  – $f_{GPTA}/2$ maximum input signal frequency
- Digital Phase Locked Loop (PLL)
  – One unit
  – Arbitrary multiplication factor between 1 and 65535
  – f_{GPTA} maximum resolution
  – $f_{GPTA}/2$ maximum input signal frequency
- Clock Distribution Unit (CDU)
  – One unit
  – Provides nine clock output signals: f_{GPTA}, divided f_{GPTA} clocks, FPC1/FPC4 outputs, DCM clock, LTC prescaler clock

Signal Generation Unit

- Global Timers (GT)
  – Two independent units
  – Two operating modes (Free-Running Timer and Reload Timer)
  – 24-bit data width
  – f_{GPTA} maximum resolution
  – $f_{GPTA}/2$ maximum input signal frequency
- Global Timer Cell (GTC)
  – 32 units related to the Global Timers
  – Two operating modes (Capture, Compare and Capture after Compare)
  – 24-bit data width
  – f_{GPTA} maximum resolution
  – $f_{GPTA}/2$ maximum input signal frequency
- Local Timer Cell (LTC)
  – 64 independent units
  – Three basic operating modes (Timer, Capture and Compare) for 63 units
  – Special compare modes for one unit
  – 16-bit data width
  – f_{GPTA} maximum resolution
  – $f_{GPTA}/2$ maximum input signal frequency

Interrupt Control Unit

- 111 interrupt sources, generating up to 38 service requests

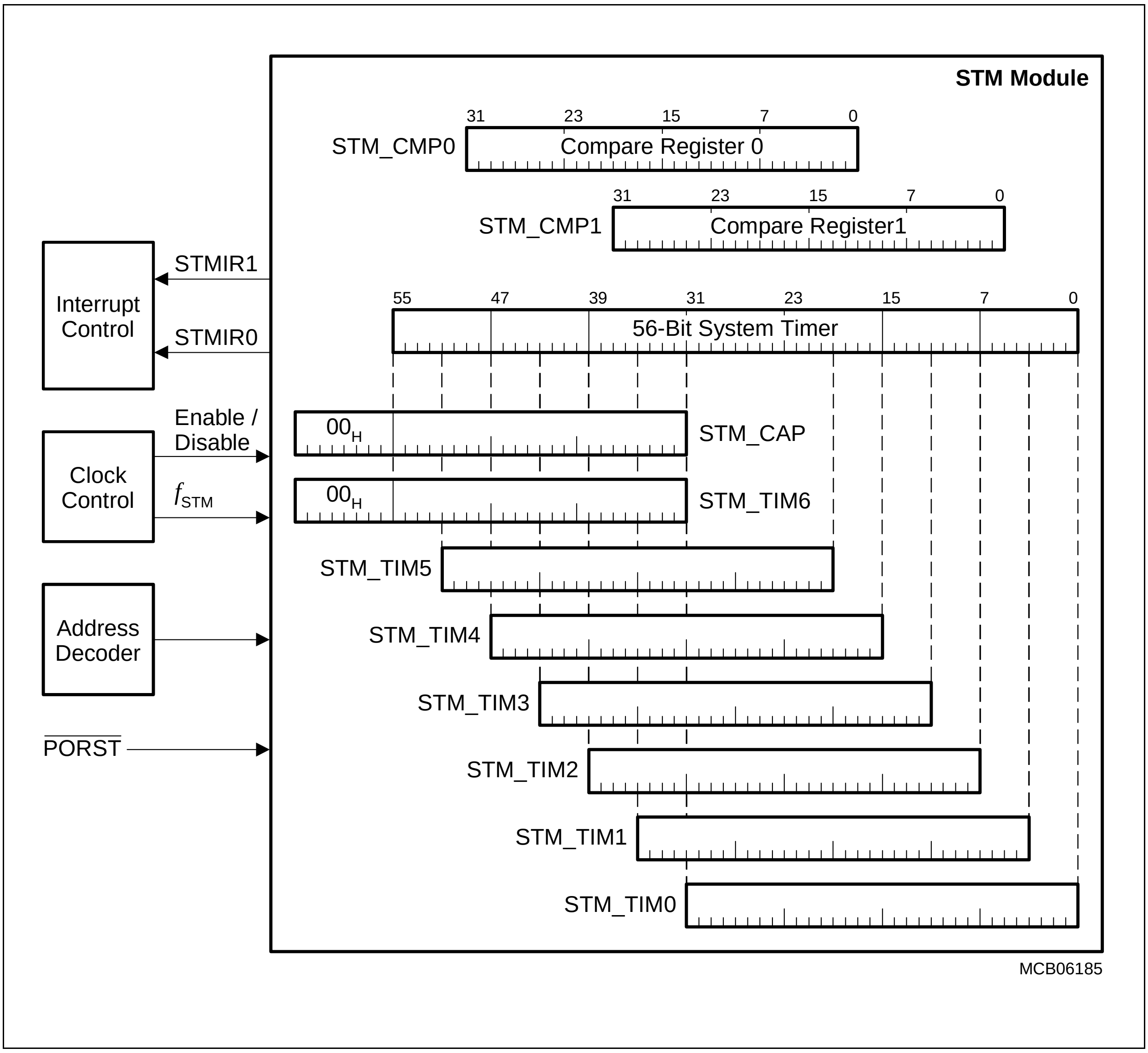

Figure 3-13 General Block Diagram of the STM Module Registers

are derived from f_{VCO} only by the K-Divider. In this mode, the system clock f_{SYS} is equal to f_{CPU}.

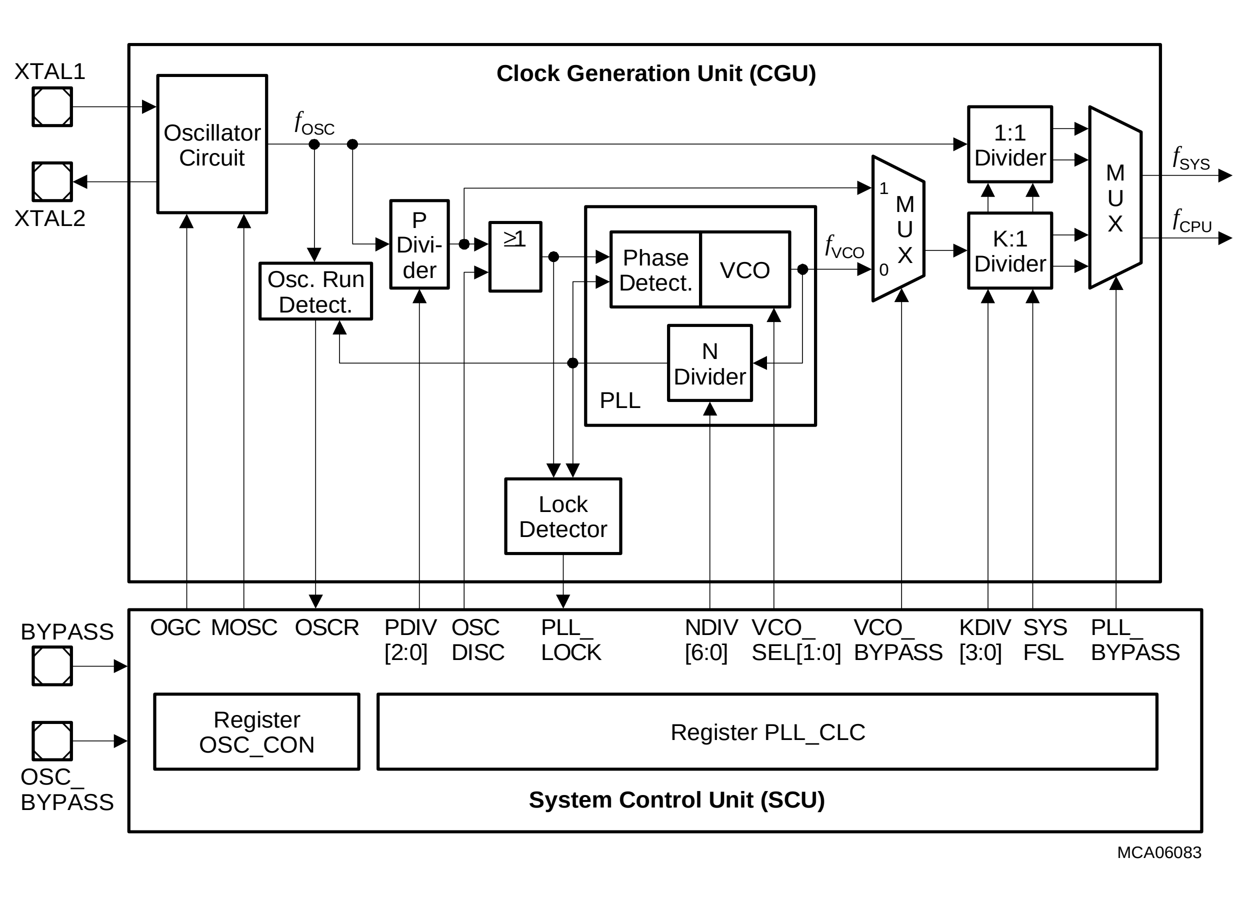

Figure 3-15 Clock Generation Unit

Recommended Oscillator Circuits

The oscillator circuit, a Pierce oscillator, is designed to work with both, an external crystal oscillator or an external stable clock source. It basically consists of an inverting amplifier and a feedback element with XTAL1 as input, and XTAL2 as output.

When using a crystal, a proper external oscillator circuitry must be connected to both pins, XTAL1 and XTAL2. The crystal frequency can be within the range of 4 MHz to 25 MHz. Additionally, it is necessary to have two load capacitances C_{X1} and C_{X2}, and depending on the crystal type, a series resistor R_{X2}, to limit the current. A test resistor R_Q may be temporarily inserted to measure the oscillation allowance (negative resistance) of the oscillator circuitry. R_Q values are typically specified by the crystal vendor. The C_{X1} and C_{X2} values shown in **Figure 3-16** can be used as starting points for the negative resistance evaluation and for non-productive systems. The exact values and related operating range are dependent on the crystal frequency and have to be determined and optimized together with the crystal vendor using the negative resistance method.

4.1.3 Absolute Maximum Ratings

Table 4-2 shows the absolute maximum ratings of the TC1766 parameters.

Table 4-2 Absolute Maximum Rating Parameters

Parameter	Symbol		Limit Values		Unit	Notes
			Min.	Max.		
Ambient temperature	T_A	SR	-40	125	°C	Under bias
Storage temperature	T_{ST}	SR	-65	150	°C	–
Junction temperature	T_J	SR	-40	150	°C	Under bias
Voltage at 1.5 V power supply pins with respect to V_{SS}[1)	V_{DD}	SR	–	2.25	V	–
Voltage at 3.3 V power supply pins with respect to V_{SS}[2)	V_{DDP}	SR	–	3.75	V	–
Voltage on any Class A input pin and dedicated input pins with respect to V_{SS}	V_{IN}	SR	-0.5	V_{DDP} + 0.5 or max. 3.7	V	Whatever is lower
Voltage on any Class D analog input pin with respect to V_{AGND}	V_{AIN}, V_{AREFx}	SR	-0.5	V_{DDM} + 0.5 or max. 3.7	V	Whatever is lower
Voltage on any Class D analog input pin with respect to V_{SSAF}	V_{AINF}, V_{FAREF}	SR	-0.5	V_{DDMF} + 0.5 or max. 3.7	V	Whatever is lower
CPU & LMB Bus Frequency	f_{CPU}	SR	–	80[3)	MHz	–
FPI Bus Frequency	f_{SYS}	SR	–	80[3)	MHz	[4)

1) Applicable for V_{DD}, V_{DDOSC}, V_{DDPLL}, and V_{DDAF}.

2) Applicable for V_{DDP}, V_{DDFL3}, V_{DDM}, and V_{DDMF}.

3) The PLL jitter characteristics add to this value according to the application settings. See the PLL jitter parameters.

4) The ratio between f_{CPU} and f_{SYS} is fixed at 1:1.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions (V_{IN} > related V_{DD} or V_{IN} < V_{SS}) the voltage on the related V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Table 4-4 Pin Groups for Overload/Short-Circuit Current Sum Parameter

Group	Pins
1	TRCLK, P5.[7:0], P0.[7:6], P0.[15:14]
2	P0.[13:12], P0.[5:4], P2.[13:8], SOP0A, SON0, FCLP0A, FCLN0
3	P0.[11:8], P0.[3:0], P3.[13:11]
4	P3[10:0], P3.[15:14]
5	$\overline{\text{HDRST}}$, $\overline{\text{PORST}}$, $\overline{\text{NMI}}$, $\overline{\text{TESTMODE}}$, $\overline{\text{BRKIN}}$, $\overline{\text{BRKOUT}}$, BYPASS, TCK, $\overline{\text{TRST}}$, TDO, TMS, TDI, P1.[7:4]
6	P1.[3:0], P1.[11:8], P4.[3:0]
7	P2.[7:0], P1.[14:12]
8	P5.[15:8]

Table 4-5 Input/Output DC-Characteristics (cont'd)**(Operating Conditions**

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input leakage current Class A2/3/4 pins	I_{OZA24}	CC	–	±3000 ±6000	nA	$((V_{DDP}/2)-1) < V_{IN} <((V_{DDP}/2)+1)$ otherwise[3)]
Input leakage current Class A1 pins	I_{OZA1}	CC	–	±500	nA	$0\ V < V_{IN} < V_{DDP}$
Class C Pads (V_{DDP} = 3.13 to 3.47 V = 3.3V ±5%)						
Output low voltage	V_{OL}	CC	815		mV	Parallel termination 100 Ω ± 1%
Output high voltage	V_{OH}	CC		1545	mV	
Output differential voltage	V_{OD}	CC	150	600	mV	
Output offset voltage	V_{OS}	CC	1075	1325	mV	
Output impedance	R_0	CC	40	140		–
Class D Pads						
see ADC Characteristics			–	–	–	–

1) Not subject to production test, verified by design / characterization.

2) The pads that have spike filter function in the input path: $\overline{\text{PORST}}$, $\overline{\text{HDRST}}$, $\overline{\text{NMI}}$ do not have hysteresis.

3) Only one of these parameters is tested, the other is verified by design characterization

4) Max. resistance between pin and next power supply pin 25 Ω for strong driver mode (verified by design characterization).

5) Function verified by design, value is not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

Table 4-6 ADC Characteristics (cont'd) (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions / Remarks
			Min.	Typ.	Max.		
ON resistance of the transmission gates in the analog voltage path	R_{AIN}	CC	–	1	1.5	kΩ	[9]
ON resistance for the ADC test (pull-down for AIN7)	R_{AIN7T}	CC	200	300	1000	Ω	Test feature available only for AIN7 [9]
Current through resistance for the ADC test (pull-down for AIN7)	I_{AIN7T}	CC	–	15 rms	30 peak	mA	Test feature available only for AIN7 [9]

1) Voltage overshoot to 4 V are permissible, provided the pulse duration is less than 100 μs and the cumulated summary of the pulses does not exceed 1 h.

2) Voltage overshoot to 1.7 V are permissible, provided the pulse duration is less than 100 μs and the cumulated summary of the pulses does not exceed 1 h.

3) A running conversion may become inexact in case of violating the normal operating conditions (voltage overshoot).

4) If the reference voltage V_{AREF} increases or the V_{DDM} decreases, so that V_{AREF} = (V_{DDM} + 0.05 V to V_{DDM} + 0.07 V), then the accuracy of the ADC decreases by 4LSB12.

5) If a reduced reference voltage in a range of $V_{DDM}/2$ to V_{DDM} is used, then the ADC converter errors increase. If the reference voltage is reduced with the factor k (k<1), then TUE, DNL, INL Gain and Offset errors increase with the factor 1/k.
If a reduced reference voltage in a range of 1 V to $V_{DDM}/2$ is used, then there are additional decrease in the ADC speed and accuracy.

6) Current peaks of up to 6 mA with a duration of max. 2 ns may occur

7) TUE is tested at V_{AREF} = 3.3 V, V_{AGND} = 0 V and V_{DDM} = 3.3 V

8) ADC module capability.

9) Not subject to production test, verified by design / characterization.

10) Value under typical application conditions due to integration (switching noise, etc.).

11) The sum of DNL/INL/Gain/Offset errors does not exceed the related TUE total unadjusted error.

12) For 10-bit conversions the DNL/INL/Gain/Offset error values must be multiplied with factor 0.25.
For 8-bit conversions the DNL/INL/Gain/Offset error values must be multiplied with 0.0625.

13) The leakage current definition is a continuous function, as shown in **Figure 4-3**. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function.

14) Only one of these parameters is tested, the other is verified by design characterization.

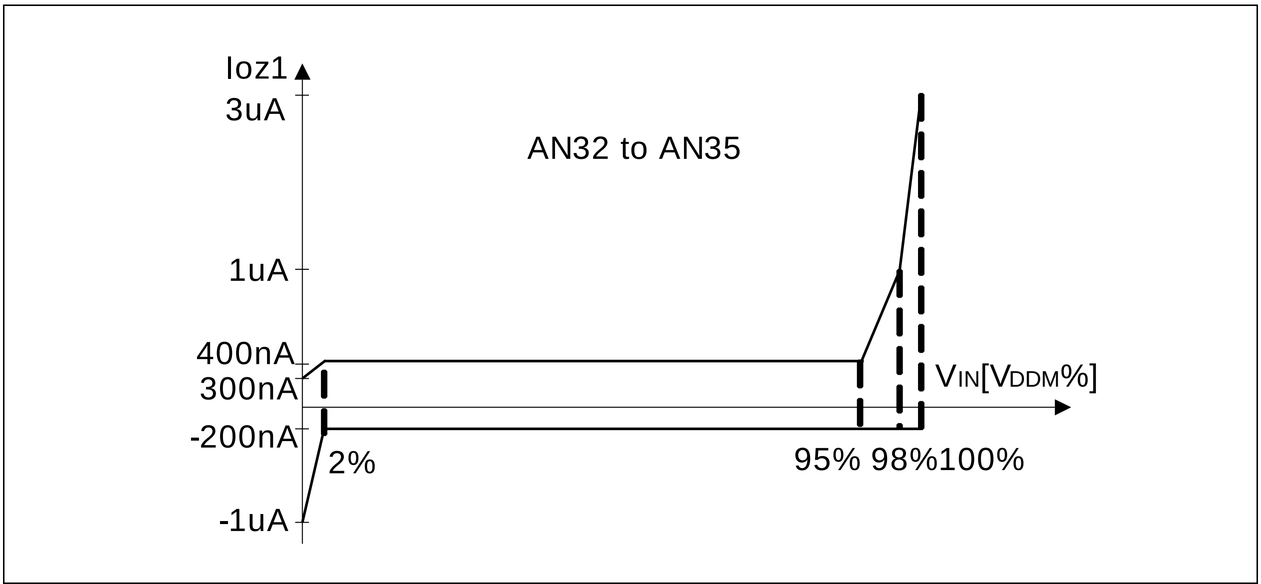

Figure 4-5 Analog Inputs AN32-AN35 Leakage

4.3.2 Output Rise/Fall Times

Table 4-11 provides the characteristics of the output rise/fall times in the TC1766.

Table 4-11 Output Rise/Fall Times (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Class A1 Pads					
Rise/fall times[1)] Class A1 pads	t_{RA1}, t_{FA1}		50 140 18000 150 550 65000	ns	Regular (medium) driver, 50 pF Regular (medium) driver, 150 pF Regular (medium) driver, 20 nF Weak driver, 20 pF Weak driver, 150 pF Weak driver, 20 000 pF
Class A2 Pads					
Rise/fall times [1)] Class A2 pads	t_{FA2}, t_{FA2}		3.3 6 5.5 16 50 140 18000 150 550 65000	ns	Strong driver, sharp edge, 50 pF Strong driver, sharp edge, 100pF Strong driver, med. edge, 50 pF Strong driver, soft edge, 50 pF Medium driver, 50 pF Medium driver, 150 pF Medium driver, 20 000 pF Weak driver, 20 pF Weak driver, 150 pF Weak driver, 20 000 pF
Class A3 Pads					
Rise/fall times [1)] Class A3 pads	t_{FA3}, t_{FA3}		2.5	ns	50 pF
Class A4 Pads					
Rise/fall times [1)] Class A4 pads	t_{FA4}, t_{FA4}		2.0	ns	25 pF
Class C Pads					
Rise/fall times Class C pads	t_{rC}, t_{fC}		2	ns	

1) Not all parameters are subject to production test, but verified by design/characterization and test correlation.

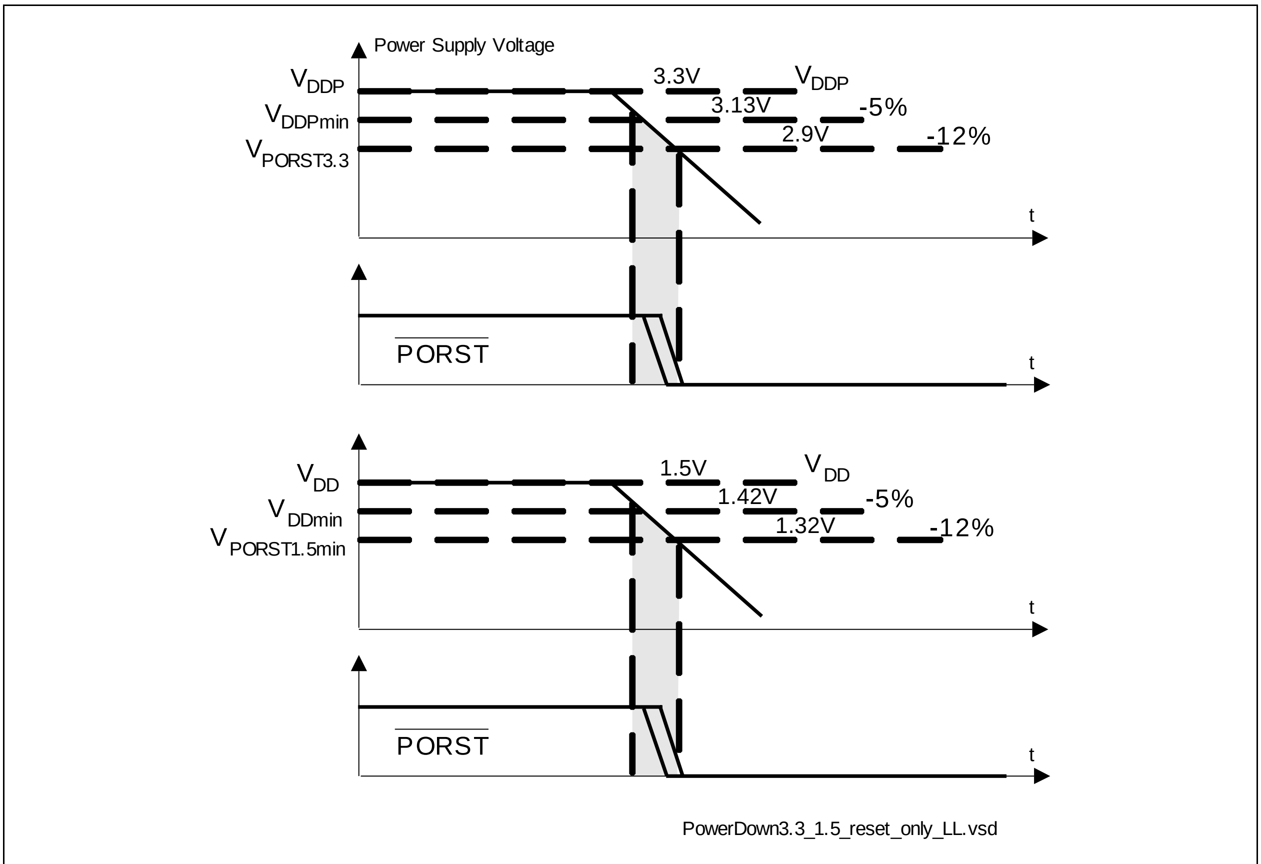

Figure 4-10 Power Down / Power Loss Sequence

4.3.5 Phase Locked Loop (PLL)

Section 4.3.5 provides the characteristics of the PLL parameters and its operation in the TC1766.

Note: All PLL characteristics defined on this and the next page are verified by design characterization.

Table 4-13 PLL Parameters (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit
		Min.	Max.	
Accumulated jitter	D_P	See Figure 4-12		–
VCO frequency range	f_{VCO}	400	500	MHz
		500	600	MHz
		600	700	MHz
PLL base frequency[1)]	$f_{PLLBASE}$	140	320	MHz
		150	400	MHz
		200	480	MHz
PLL lock-in time	t_L	–	200	µs

1) The CPU base frequency which is selected after reset is calculated by dividing the limit values by 16 (this is the K factor after reset).

Phase Locked Loop Operation

When PLL operation is enabled and configured, the PLL clock f_{VCO} (and with it the CPU clock f_{CPU}) is constantly adjusted to the selected frequency. The relation between f_{VCO} and f_{SYS} is defined by: $f_{VCO} = K \times f_{CPU}$. The PLL causes a jitter of f_{CPU} and affects the clock outputs TRCLK and SYSCLK (P4.3) which are derived from the PLL clock f_{VCO}.

There are two formulas that define the (absolute) approximate maximum value of jitter D_P in ns dependent on the K-factor, the CPU clock frequency f_{CPU} in MHz, and the number P of consecutive f_{CPU} clock periods.

$$P \times K < 900 \qquad Dp[ns] = \pm\left(\frac{5 \times P}{fcpu[MHz]} + 0,9\right) \tag{4.1}$$

$$P \times K \geq 900 \qquad Dp[ns] = \pm\left(\frac{4500}{fcpu[MHz] \times K} + 0,9\right) \tag{4.2}$$

K : K-Divider Value

P : Number of f_{CPU} periods

D_P : Jitter in ns

f_{CPU} : CPU frequency in MHz

4.3.7 Timing for JTAG Signals

(Operating Conditions apply, C_L = 50 pF)

Table 4-15 TCK Clock Timing Parameter

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
TCK clock period[1)]	t_{TCK}	SR	25	–	ns
TCK high time	t_1	SR	10	–	ns
TCK low time	t_2	SR	10	–	ns
TCK clock rise time	t_3	SR	–	4	ns
TCK clock fall time	t_4	SR	–	4	ns

1) f_{TCK} should be lower or equal to f_{SYS}

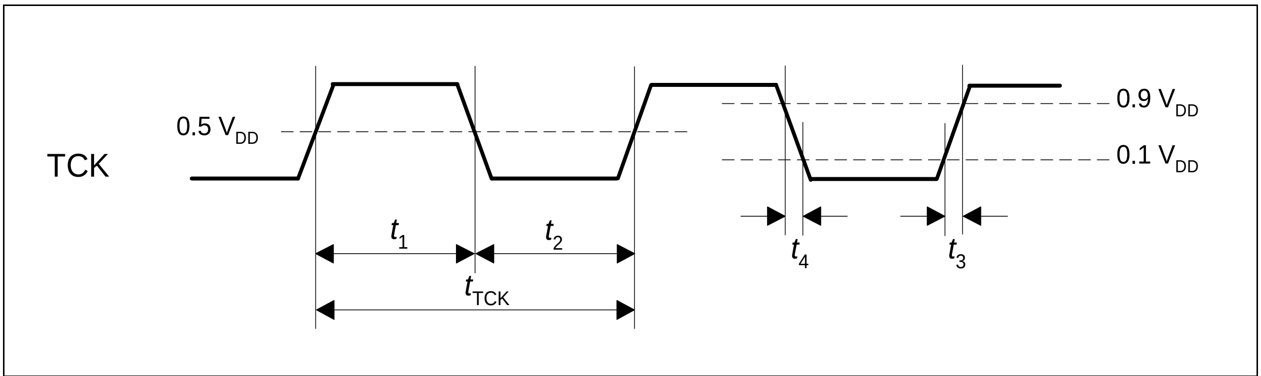

Figure 4-15 TCK Clock Timing