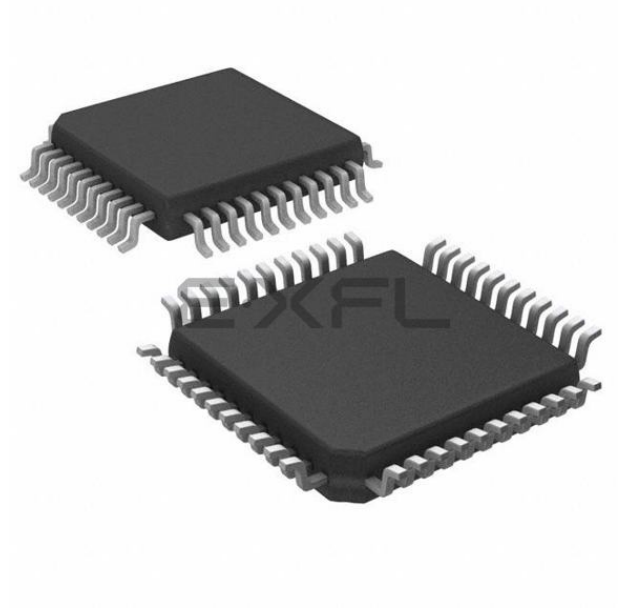

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-VQFP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts80c51rd2-lce

Reset	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to $V_{CC.}$ If the hardware watchdog reaches its time-out, the reset pin becomes an output during the time the internal reset is activated.

	PLCC68	SQUARE VQFP64 1.4
P3.2	40	29
P3.3	41	30
P3.4	42	31
P3.5	43	32
P3.6	45	34
P3.7	47	36
RESET	30	21
ALE/$\overline{PROG}$	68	56
$\overline{PSEN}$	67	55
$\overline{EA}$/VPP	2	58
XTAL1	49	38
XTAL2	48	37
P4.0	20	11
P4.1	24	15
P4.2	26	17
P4.3	44	33
P4.4	46	35
P4.5	50	39
P4.6	53	42
P4.7	57	46
P5.0	60	49
P5.1	62	51
P5.2	63	52
P5.3	7	62
P5.4	8	63
P5.5	10	1
P5.6	13	4
P5.7	16	7

6. TS80C51Rx2 Enhanced Features

In comparison to the original 80C52, the TS80C51Rx2 implements some new features, which are:

- The X2 option.
- The Dual Data Pointer.
- The extended RAM.
- The Programmable Counter Array (PCA).
- The Watchdog.
- The 4 level interrupt priority system.
- The power-off flag.
- The ONCE mode.
- The ALE disabling.
- Some enhanced features are also located in the UART and the timer 2.

6.1. X2 Feature

The TS80C51Rx2 core needs only 6 clock periods per machine cycle. This feature called ”X2” provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

6.1.1. Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 1. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 2. shows the mode switching waveforms.

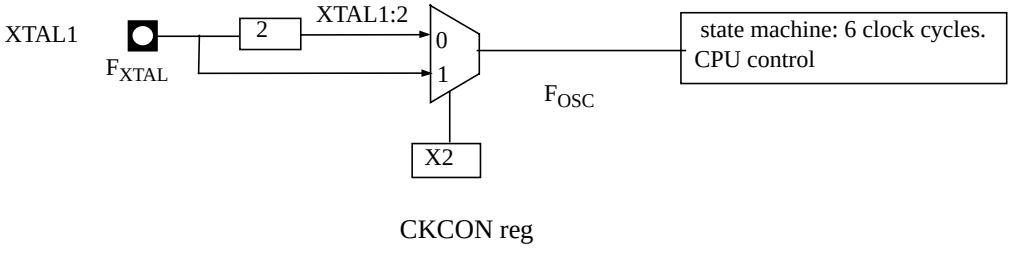


Figure 1. Clock Generation Diagram

ASSEMBLY LANGUAGE

```
; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2              AUXR1 EQU 0A2H
;
0000  909000      MOV  DPTR,#SOURCE     ; address of SOURCE
0003  05A2        INC   AUXR1           ; switch data pointers
0005  90A000      MOV  DPTR,#DEST       ; address of DEST
0008              LOOP:
0008  05A2        INC   AUXR1           ; switch data pointers
000A  E0          MOVX A,@DPTR          ; get a byte from SOURCE
000B  A3          INC   DPTR            ; increment SOURCE address
000C  05A2        INC   AUXR1           ; switch data pointers
000E  F0          MOVX @DPTR,A          ; write the byte to DEST
000F  A3          INC   DPTR            ; increment DEST address
0010  70F6        JNZ   LOOP            ; check for 0 terminator
0012  05A2        INC   AUXR1           ; (optional) restore DPS
```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.

Table 7. T2MOD Register

T2MOD - Timer 2 Mode Control Register (C9h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	DCEN

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	T2OE	**Timer 2 Output Enable bit** Clear to program P1.0/T2 as clock input or I/O port. Set to program P1.0/T2 as clock output.
0	DCEN	**Down Counter Enable bit** Clear to disable timer 2 as up/down counter. Set to enable timer 2 as up/down counter.

Reset Value = XXXX XX00b
Not bit addressable

6.5. Programmable Counter Array PCA

The PCA provides more timing capabilities with less CPU intervention than the standard timer/counters. Its advantages include reduced software overhead and improved accuracy. The PCA consists of a dedicated timer/counter which serves as the time base for an array of five compare/ capture modules. Its clock input can be programmed to count any one of the following signals:

- Oscillator frequency ÷ 12 (÷ 6 in X2 mode)
- Oscillator frequency ÷ 4 (÷ 2 in X2 mode)
- Timer 0 overflow
- External input on ECI (P1.2)

Each compare/capture modules can be programmed in any one of the following modes:

- rising and/or falling edge capture,
- software timer,
- high-speed output, or
- pulse width modulator.

Module 4 can also be programmed as a watchdog timer (See Section "PCA Watchdog Timer", page 33).

When the compare/capture modules are programmed in the capture mode, software timer, or high speed output mode, an interrupt can be generated when the module executes its function. All five modules plus the PCA timer overflow share one interrupt vector.

The PCA timer/counter and compare/capture modules share Port 1 for external I/O. These pins are listed below. If the port is not used for the PCA, it can still be used for standard I/O.

PCA component	External I/O Pin
16-bit Counter	P1.2 / ECI
16-bit Module 0	P1.3 / CEX0
16-bit Module 1	P1.4 / CEX1
16-bit Module 2	P1.5 / CEX2
16-bit Module 3	P1.6 / CEX3
16-bit Module 4	P1.7 / CEX4

The PCA timer is a common time base for all five modules (See Figure 7). The timer count source is determined from the CPS1 and CPS0 bits in the **CMOD SFR** (See Table 8) and can be programmed to run at:

- 1/12 the oscillator frequency. (Or 1/6 in X2 Mode)
- 1/4 the oscillator frequency. (Or 1/2 in X2 Mode)
- The Timer 0 overflow
- The input on the ECI pin (P1.2)

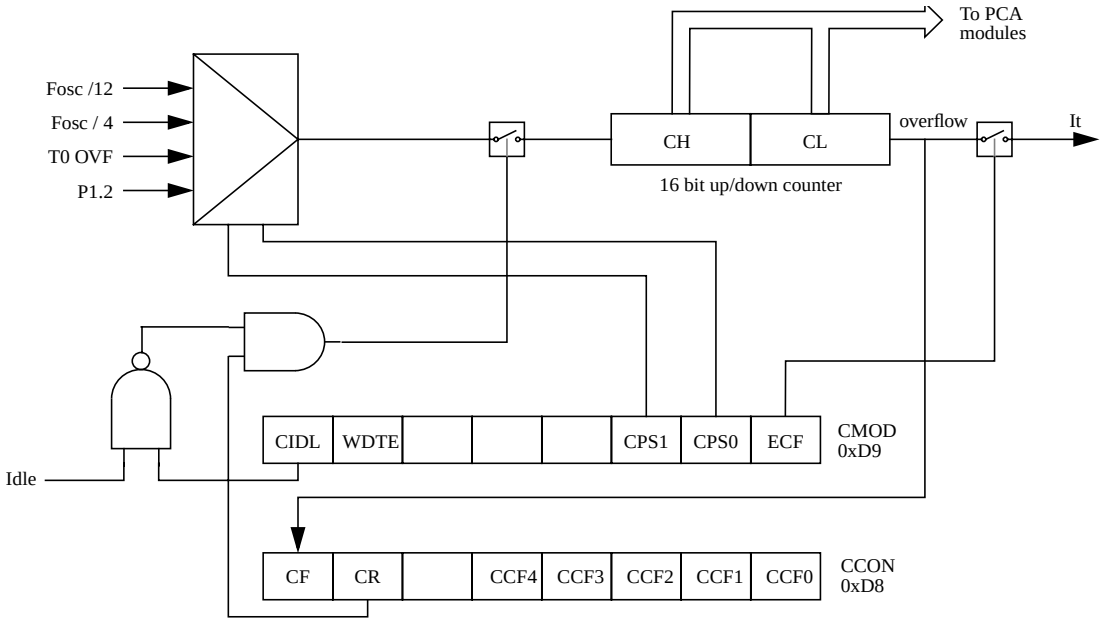


Figure 7. PCA Timer/Counter

Table 8. CMOD: PCA Counter Mode Register

CMOD Address 0D9H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF
Reset value	0	0	X	X	X	0	0	0

Symbol	Function		
CIDL	Counter Idle control: CIDL = 0 programs the PCA Counter to continue functioning during idle Mode. CIDL = 1 programs it to be gated off during idle.		
WDTE	Watchdog Timer Enable: WDTE = 0 disables Watchdog Timer function on PCA Module 4. WDTE = 1 enables it.		
-	Not implemented, reserved for future use.[a]		
CPS1	PCA Count Pulse Select bit 1.		
CPS0	PCA Count Pulse Select bit 0.		
	CPS1	**CPS0**	**Selected PCA input**.[b]
	0	0	Internal clock f_{osc}/12 (Or f_{osc}/6 in X2 Mode).
	0	1	Internal clock f_{osc}/4 (Or f_{osc}/2 in X2 Mode).
	1	0	Timer 0 Overflow
	1	1	External clock at ECI/P1.2 pin (max rate = f_{osc}/ 8)
ECF	PCA Enable Counter Overflow interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function of CF.		

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.
b. f_{osc} = oscillator frequency

The CMOD SFR includes three additional bits associated with the PCA (See Figure 7 and Table 8).

- The CIDL bit which allows the PCA to stop during idle mode.
- The WDTE bit which enables or disables the watchdog function on module 4.

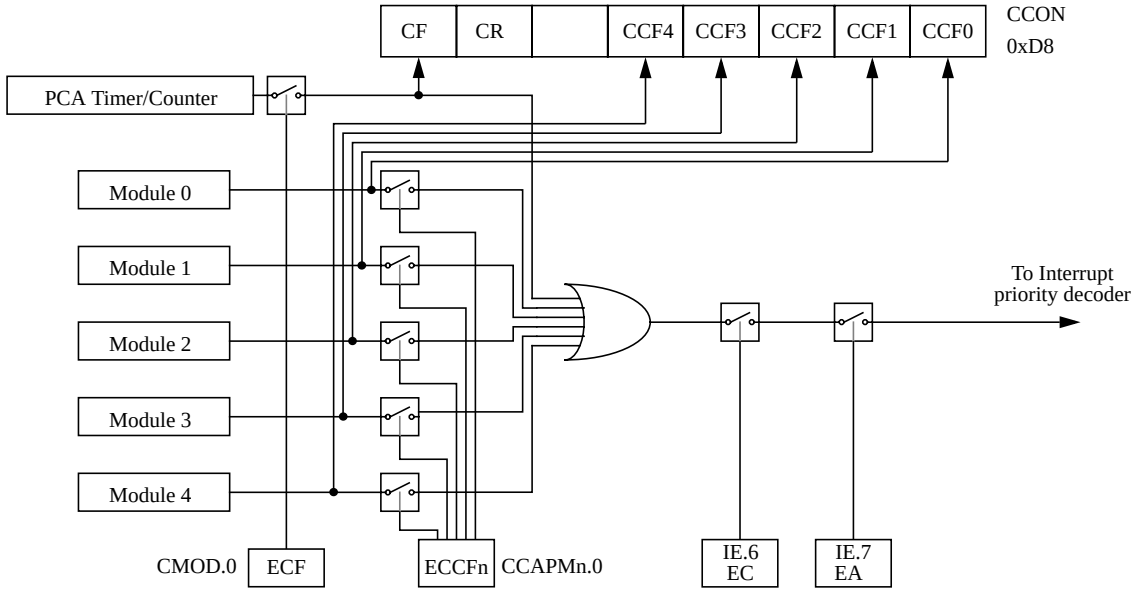


Figure 8. PCA Interrupt System

PCA Modules: each one of the five compare/capture modules has six possible functions. It can perform:

- 16-bit Capture, positive-edge triggered,
- 16-bit Capture, negative-edge triggered,
- 16-bit Capture, both positive and negative-edge triggered,
- 16-bit Software Timer,
- 16-bit High Speed Output,
- 8-bit Pulse Width Modulator.

In addition, module 4 can be used as a Watchdog Timer.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. (See Table 10). The registers contain the bits that control the mode that each module will operate in.

- The ECCF bit (CCAPMn.0 where n=0, 1, 2, 3, or 4 depending on the module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module.
- PWM (CCAPMn.1) enables the pulse width modulation mode.
- The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register.
- The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.
- The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition.
- The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function.

Table 11 shows the CCAPMn settings for the various PCA functions.

.

6.5.3. High Speed Output Mode

In this mode the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set (See Figure 11).

A prior write must be done to CCAPnL and CCAPnH before writing the ECOMn bit.

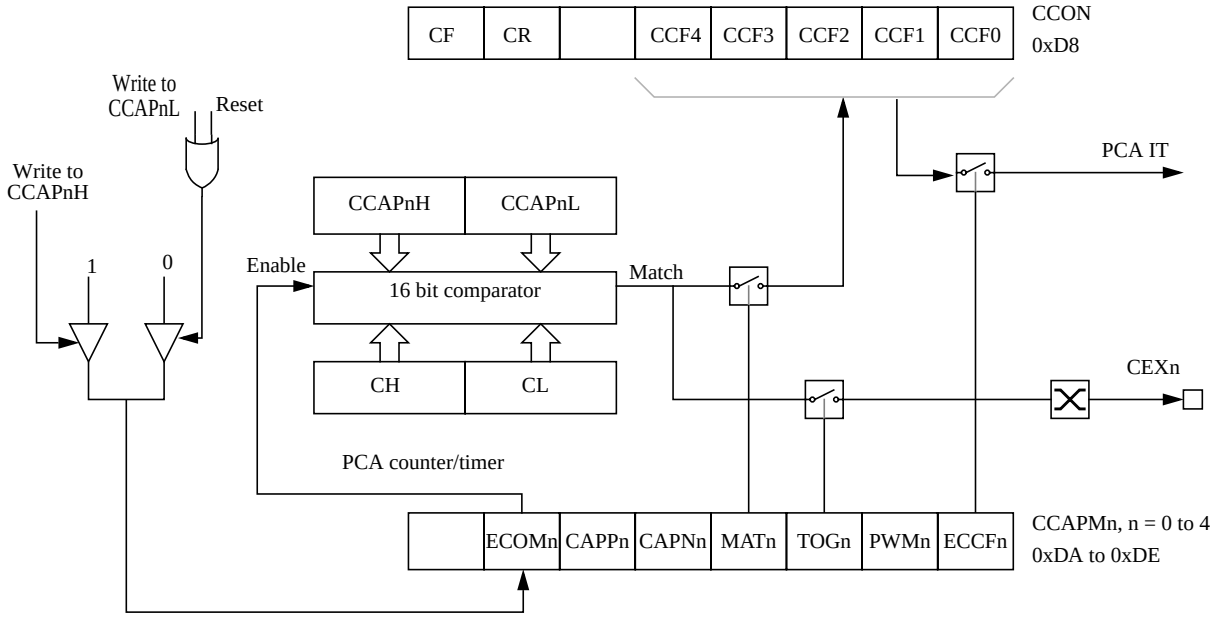


Figure 11. PCA High Speed Output Mode

Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.

Table 16. SCON Register

SCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0
FE/SM0	**SM1**	**SM2**	**REN**	**TB8**	**RB8**	**TI**	**RI**

Bit Number	Bit Mnemonic	Description
7	FE	**Framing Error bit (SMOD0=1)** Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit
	SM0	**Serial port Mode bit 0** Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit
6	SM1	**Serial port Mode bit 1** SM0 SM1 Mode Description Baud Rate 0 0 0 Shift Register F_{XTAL}/12 (/6 in X2 mode) 0 1 1 8-bit UART Variable 1 0 2 9-bit UART F_{XTAL}/64 or F_{XTAL}/32 (/32, /16 in X2 mode) 1 1 3 9-bit UART Variable
5	SM2	**Serial port Mode 2 bit / Multiprocessor Communication Enable bit** Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.
4	REN	**Reception Enable bit** Clear to disable serial reception. Set to enable serial reception.
3	TB8	**Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3.** Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.
2	RB8	**Receiver Bit 8 / Ninth bit received in modes 2 and 3** Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.
1	TI	**Transmit Interrupt flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.
0	RI	**Receive Interrupt flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 14. and Figure 15. in the other modes.

Reset Value = 0000 0000b
Bit addressable

6.7. Interrupt System

The TS80C51Rx2 has a total of 7 interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (timers 0, 1 and 2), the serial port interrupt and the PCA global interrupt. These interrupts are shown in Figure 16.

WARNING: Note that in the first version of RC devices, the PCA interrupt is in the lowest priority. Thus the order in $\overline{INT0}$, TF0, $\overline{INT1}$, TF1, RI or TI, TF2 or EXF2, PCA.

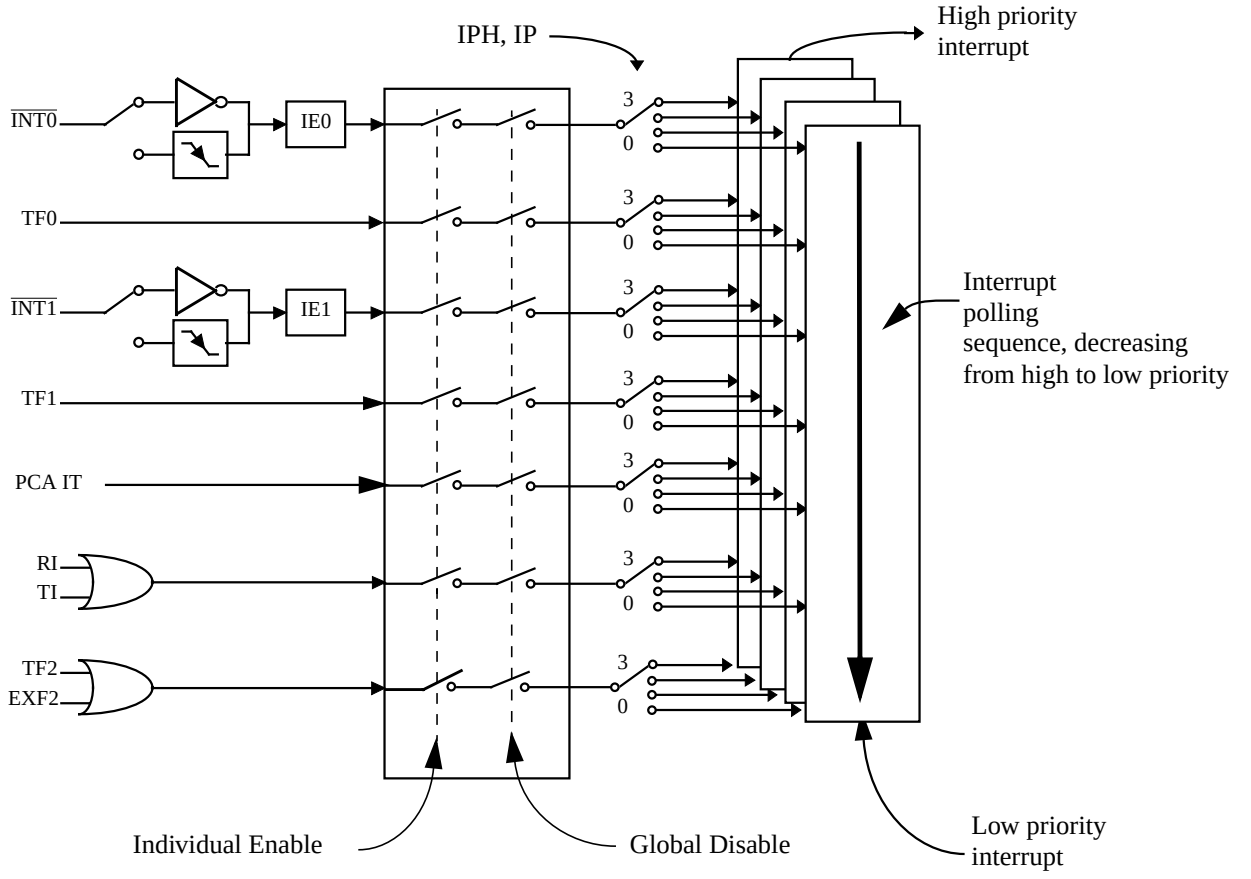


Figure 16. Interrupt Control System

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 19.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 20.) and in the Interrupt Priority High register (See Table 21.). shows the bit values and priority levels associated with each combination.

The PCA interrupt vector is located at address 0033H. All other vector addresses are the same as standard C52 devices.

Table 21. IPH Register

IPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0
-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	PPCH	**PCA interrupt priority bit high.** PPCH PPC Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
5	PT2H	**Timer 2 overflow interrupt Priority High bit** PT2H PT2 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
4	PSH	**Serial port Priority High bit** PSH PS Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
3	PT1H	**Timer 1 overflow interrupt Priority High bit** PT1H PT1 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
2	PX1H	**External interrupt 1 Priority High bit** PX1H PX1 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
1	PT0H	**Timer 0 overflow interrupt Priority High bit** PT0H PT0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
0	PX0H	**External interrupt 0 Priority High bit** PX0H PX0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest

Reset Value = X000 0000b
Not bit addressable

Table 22. The state of ports during idle and power-down mode

Mode	Program Memory	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data*	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data*	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

* Port 0 can force a "zero" level. A "one" will leave port floating.

6.11. ONCE™ Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS80C51Rx2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C51Rx2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and $\overline{PSEN}$ is high.
- Hold ALE low as RST is deactivated.

While the TS80C51Rx2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 26. shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

Table 25. External Pin Status during ONCE Mode

ALE	PSEN	Port 0	Port 1	Port 2	Port 3	XTAL1/2
Weak pull-up	Weak pull-up	Float	Weak pull-up	Weak pull-up	Weak pull-up	Active

7. TS83C51RB2/RC2/RD2 ROM

7.1. ROM Structure

The TS83C51RB2/RC2/RD2 ROM memory is divided in three different arrays:

- the code array: . . . . . 16/32/64 Kbytes.
- the encryption array: . . . . . 64 bytes.
- the signature array:. . . . . 4 bytes.

7.2. ROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

7.2.1. 7.2.1. Encryption Array

Within the ROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

7.2.2. Program Lock Bits

The lock bits when programmed according to Table 28. will provide different level of protection for the on-chip code and data.

Table 28. Program Lock bits

Program Lock Bits				Protection description
Security level	**LB1**	**LB2**	**LB3**	
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	P	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset.
3	U	P	U	Same as level 1+ Verify disable. This security level is only available for 51RDX2 devices.

U: unprogrammed
P: programmed

7.2.3. Signature bytes

The TS83C51RB2/RC2/RD2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 8.3.

7.2.4. Verify Algorithm

Refer to 8.3.4.

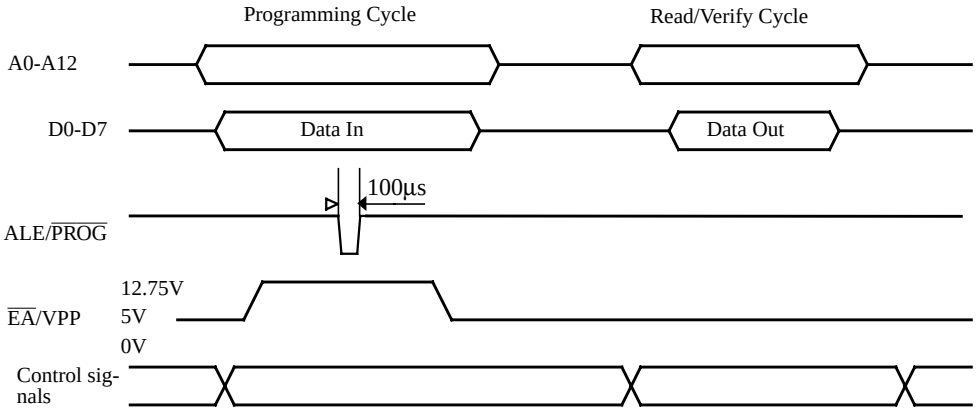


Figure 19. Programming and Verification Signal's Waveform

8.4. EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

8.4.1. Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 µW/cm^2 rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

10.5. AC Parameters

10.5.1. Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example:T_{AVLL} = Time for Address Valid to ALE Low.
T_{LLPL} = Time for ALE Low to $\overline{PSEN}$ Low.

TA = 0 to +70°C (commercial temperature range); V_{SS} = 0 V; V_{CC} = 5 V ± 10%; -M and -V ranges.
TA = -40°C to +85°C (industrial temperature range); V_{SS} = 0 V; V_{CC} = 5 V ± 10%; -M and -V ranges.
TA = 0 to +70°C (commercial temperature range); V_{SS} = 0 V; 2.7 V < V_{CC} < 5.5 V; -L range.
TA = -40°C to +85°C (industrial temperature range); V_{SS} = 0 V; 2.7 V < V_{CC} < 5.5 V; -L range.

Table 34. gives the maximum applicable load capacitance for Port 0, Port 1, 2 and 3, and ALE and $\overline{PSEN}$ signals. Timings will be guaranteed if these capacitances are respected. Higher capacitance values can be used, but timings will then be degraded.

Table 34. Load Capacitance versus speed range, in pF

	-M	-V	-L
Port 0	100	50	100
Port 1, 2, 3	80	50	80
ALE / $\overline{PSEN}$	100	30	100

Table 36., Table 39. and Table 42. give the description of each AC symbols.

Table 37., Table 40. and Table 43. give for each range the AC parameter.

Table 38., Table 41. and Table 44. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

Table 35. Max frequency for derating formula regarding the speed grade

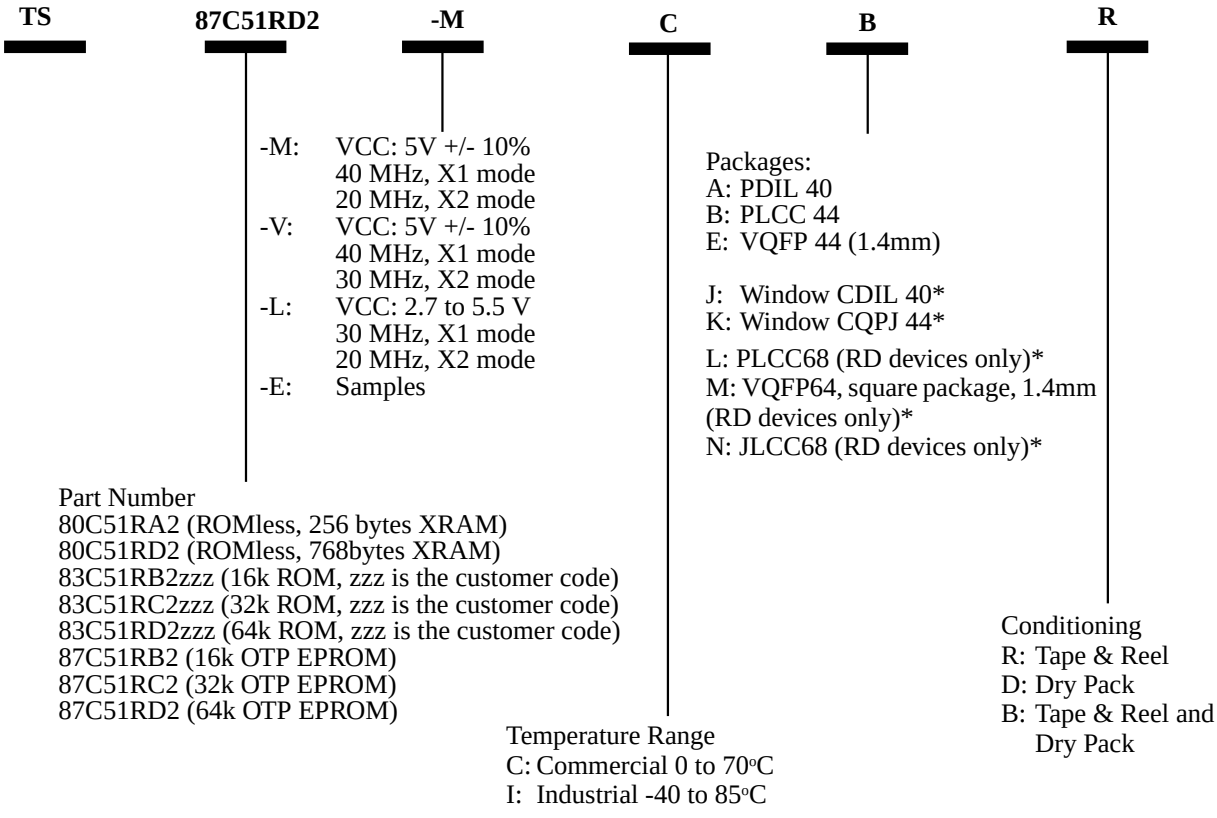
	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	20	40	30	30	20
T (ns)	25	50	25	33.3	33.3	50

Example:
T_{LLIV} in X2 mode for a -V part at 20 MHz (T = $1/20^{E6}$ = 50 ns):
x= 22 (Table 38.)
T= 50ns
T_{LLIV}= 2T - x = 2 x 50 - 22 = 78ns

Table 40. AC Parameters for a Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
T_{RLRH}	130		85		135		125		175		ns
T_{WLWH}	130		85		135		125		175		ns
T_{RLDV}		100		60		102		95		137	ns
T_{RHDX}	0		0		0		0		0		ns
T_{RHDZ}		30		18		35		25		42	ns
T_{LLDV}		160		98		165		155		222	ns
T_{AVDV}		165		100		175		160		235	ns
T_{LLWL}	50	100	30	70	55	95	45	105	70	130	ns
T_{AVWL}	75		47		80		70		103		ns
T_{QVWX}	10		7		15		5		13		ns
T_{QVWH}	160		107		165		155		213		ns
T_{WHQX}	15		9		17		10		18		ns
T_{RLAZ}		0		0		0		0		0	ns
T_{WHLH}	10	40	7	27	15	35	5	45	13	53	ns

11. Ordering Information



(*) Check with Atmel Wireless & Microcontrollers Sales Office for availability. Ceramic packages (J, K, N) are available for proto typing, not for volume production. Ceramic packages are available for OTP only.

Table 47. Maximum Clock Frequency

Code	-M	-V	-L	Unit
Standard Mode, oscillator frequency Standard Mode, internal frequency	40 40	40 40	30 30	MHz
X2 Mode, oscillator frequency X2 Mode, internal equivalent frequency	20 40	30 **60**	20 **40**	MHz

Table 48. Possible Ordering Entries

	TS80C51RA2/RD2 ROMless	TS83C51RB2/RC2/RD2zzz ROM	TS87C51RB2/RC2/RD2 OTP
-MCA	X	X	X
-MCB	X	X	X
-MCE	X	X	X
-MCL	RD2 only	RD2 only	RD2 only
-MCM	RD2 only	RD2 only	RD2 only
-VCA	X	X	X
-VCB	X	X	X
-VCE	X	X	X
-VCL	RD2 only	RD2 only	RD2 only
-VCM	RD2 only	RD2 only	RD2 only
-LCA	X	X	X
-LCB	X	X	X
-LCE	X	X	X
-LCL	RD2 only	RD2 only	RD2 only
-LCM	RD2 only	RD2 only	RD2 only
-MIA	X	X	X
-MIB	X	X	X
-MIE	X	X	X
-MIL	RD2 only	RD2 only	RD2 only
-MIM	RD2 only	RD2 only	RD2 only
-VIA	X	X	X
-VIB	X	X	X
-VIE	X	X	X
-VIL	RD2 only	RD2 only	RD2 only
-VIM	RD2 only	RD2 only	RD2 only
-LIA	X	X	X
-LIB	X	X	X
-LIE	X	X	X
-LIL	RD2 only	RD2 only	RD2 only
-LIM	RD2 only	RD2 only	RD2 only
-EA	X		X
-EB	X		X
-EE	X		X
-EL	RD2 only		RD2 only
-EM	RD2 only		RD2 only
-EJ			RC2 and RD2 only
-EK			RC2 and RD2 only
-EN			RD2 only

- -Ex for samples
- Tape and Reel available for B, E, L and M packages
- Dry pack mandatory for E and M packages