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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMIess
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIL
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts80c51rd2-lia

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



	Pin Number			T					
Mnemonic	DIL	LCC	VQFP 1.4	Туре	Name And Function				
V <sub>SS</sub>	20	22	16	Ι	Ground: 0V reference				
Vss1		1	39	Ι	Optional Ground: Contact the Sales Office for ground connection.				
V <sub>CC</sub>	40	44	38	Ι	<b>Power Supply:</b> This is the power supply voltage for normal, idle and power-down operation				
P0.0-P0.7	39-32	43-36	37-30	I/O	<b>Port 0</b> : Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that hav written to them float and can be used as high impedance inputs. Port 0 pins the polarized to Vcc or Vss in order to prevent any parasitic current consump Port 0 is also the multiplexed low-order address and data bus during access external program and data memory. In this application, it uses strong into pull-up when emitting 1s. Port 0 also inputs the code bytes during EPF programming. External pull-ups are required during program verification du which P0 outputs the code bytes. <b>Port 1:</b> Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 is an 8-bit bidirectional I/O port with internal pull-ups.				
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	<b>Port 1:</b> Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification. Alternate functions for Port 1 include:				
	1	2	40	I/O	T2 (P1.0): Timer/Counter 2 external count input/Clockout				
	2	3	41	I	T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction Control				
	3	4	42	Ι	ECI (P1.2): External Clock for the PCA				
	4	5	43	I/O	CEX0 (P1.3): Capture/Compare External I/O for PCA module 0				
	5	6	44	I/O	CEX1 (P1.4): Capture/Compare External I/O for PCA module 1				
	6	7	45	I/O	CEX0 (P1.5): Capture/Compare External I/O for PCA module 2				
	7	8	46	I/O	CEX0 (P1.6): Capture/Compare External I/O for PCA module 3				
	8	9	47	I/O	CEX0 (P1.7): Capture/Compare External I/O for PCA module 4				
P2.0-P2.7	21-28	24-31	18-25	I/O	<b>Port 2</b> : Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR).In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR. Some Port 2 pins (P2.0 to P2.5) receive the high order address bits during EPROM programming and verification:				
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	<b>Port 3:</b> Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Some Port 3 pins (P3.4 to P3.5) receive the high order address bits during EPROM programming and verification. Port 3 also serves the special features of the 80C51 family, as listed below.				
	10	11	5	I	RXD (P3.0): Serial input port				
	11	13	7	0	TXD (P3.1): Serial output port				
	12	14	8	I	<b>INTO</b> (P3.2): External interrupt 0				
	13	15	9	I	<b>INT1</b> (P3.3): External interrupt 1				
	14	16	10	I	T0 (P3.4): Timer 0 external input				
	15	17	11	I	T1 (P3.5): Timer 1 external input				
	16	18	12	0	WR (P3.6): External data memory write strobe				
	17	19	13	0	RD (P3.7): External data memory read strobe				



## **5.1. Pin Description for 64/68 pin Packages**

Port 4 and Port 5 are 8-bit bidirectional I/O ports with internal pull-ups. Pins that have 1 written to them are pulled high by the internal pull ups and can be used as inputs.

As inputs, pins that are externally pulled low will source current because of the internal pull-ups.

Refer to the previous pin description for other pins.

	PLCC68	SQUARE VQFP64 1.4
VSS	51	9/40
VCC	17	8
P0.0	15	6
P0.1	14	5
P0.2	12	3
P0.3	11	2
P0.4	9	64
P0.5	6	61
P0.6	5	60
P0.7	3	59
P1.0	19	10
P1.1	21	12
P1.2	22	13
P1.3	23	14
P1.4	25	16
P1.5	27	18
P1.6	28	19
P1.7	29	20
P2.0	54	43
P2.1	55	44
P2.2	56	45
P2.3	58	47
P2.4	59	48
P2.5	61	50
P2.6	64	53
P2.7	65	54
P3.0	34	25
P3.1	39	28

Table	2.	64/68	Pin	Packages	Configuration
I GOIC		0.00		I uchages	Comparation



	PLCC68	SQUARE VQFP64 1.4
P3.2	40	29
P3.3	41	30
P3.4	42	31
P3.5	43	32
P3.6	45	34
P3.7	47	36
RESET	30	21
ALE/PROG	68	56
PSEN	67	55
EA/VPP	2	58
XTAL1	49	38
XTAL2	48	37
P4.0	20	11
P4.1	24	15
P4.2	26	17
P4.3	44	33
P4.4	46	35
P4.5	50	39
P4.6	53	42
P4.7	57	46
P5.0	60	49
P5.1	62	51
P5.2	63	52
P5.3	7	62
P5.4	8	63
P5.5	10	1
P5.6	13	4
P5.7	16	7



#### Table 3. CKCON Register

#### CKCON - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0			
-	-	-	-	-	-	-	X2			

Bit Number	Bit Mnemonic	Description
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
3	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
2	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
1	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
0	X2	<b>CPU and peripheral clock bit</b> Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$ ). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$ ).

Reset Value = XXXX XXX0b Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (http://www.atmel-wm.com)



### 6.2. Dual Data Pointer Register Ddptr

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 (See Table 4.) that allows the program code to switch between them (Refer to Figure 3).



Figure 3. Use of Dual Pointer

 Table 4. AUXR1: Auxiliary Register 1

AUXR1 Address 0A2H		-	-	-	-	GF3	-	-	DPS
	Reset value	X	Х	X	Х	0	Х	Х	0

Symbol	Function					
-	Not implemen	Not implemented, reserved for future use. <sup>a</sup>				
DPS	Data Pointer S	Data Pointer Selection.				
	DPS	Operating Mode				
	0	DPTR0 Selected				
	1	DPTR1 Selected				
GF3	This bit is a general purpose user flag <sup>b</sup> .					

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new feature. In that case, the reset value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

b. GF3 will not be available on first version of the RC devices.

### Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.



### ASSEMBLY LANGUAGE

; Block move using dual data pointers ; Destroys DPTR0, DPTR1, A and PSW ; note: DPS exits opposite of entry state ; unless an extra INC AUXR1 is added

00A2	AUXR1 EQU 0A2H	
; 0000 909000 0003 05A2 0005 004000	MOV DPTR,#SOURCE INC AUXR1 MOV DPTR #DEST	; address of SOURCE ; switch data pointers ; address of DEST
0003 90A000 0008 0008 05A2	LOOP: INC AUXR1	; switch data pointers
000A E0	MOVX A, @DPTR	; get a byte from SOURCE
000B A3	INC DPTR	; increment SOURCE address
000C 05A2	INC AUXRI	; switch data pointers
000E F0	MOVX @DPTR,A	; write the byte to DEST
000F A3	INC DPTR	: increment DEST address
0010 70F6	JNZ LOOP	; check for 0 terminator
0012 05A2	INC AUXR1	; (optional) restore DPS

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.



**The CCON SFR** contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (Refer to Table 9).

- Bit CR (CCON.6) must be set by software to run the PCA. The PCA is shut off by clearing this bit.
- Bit CF: The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software.
- Bits 0 through 4 are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software.

CC Addres	CCON Address 0D8H		CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0
	Rese	et value	0	0	X	0	0	0	0	0
Syı	nbol	Function	l							
CF		PCA Count an interrup can only be	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software bu can only be cleared by software.						gs tware but	
CR		PCA Count by software	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.							
-		Not implen	Not implemented, reserved for future use. <sup>a</sup>							
CCF4		PCA Modu cleared by	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.							
CCF3		PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Mus cleared by software.						Must be		
CCF2		PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. M cleared by software.					Must be			
CCF1		PCA Modu cleared by	ile 1 inter software.	rupt flag.	Set by ha	rdware wh	en a matc	h or captı	ire occurs.	Must be
CCF0		PCA Modu cleared by	ile 0 inter software.	rupt flag.	Set by ha	rdware wh	en a matc	h or captu	ire occurs.	Must be

 Table 9. CCON: PCA Counter Control Register

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

The watchdog timer function is implemented in module 4 (See Figure 10).

The PCA interrupt system is shown in Figure 8



Table 12	2. CCAPnH:	PCA Modu	es Capture/C	Compare	Registers	High
----------	------------	----------	--------------	---------	-----------	------

CCAPnH Address n = 0 - 4	CCAP0H=0FAH CCAP1H=0FBH CCAP2H=0FCH CCAP3H=0FDH CCAP3H=0FEH								
		7	6	5	4	3	2	1	0
	Reset value	0	0	0	0	0	0	0	0

#### Table 13. CCAPnL: PCA Modules Capture/Compare Registers Low

CCAPnL Address n = 0 - 4	CCAP0L=0EAH CCAP1L=0EBH CCAP2L=0ECH CCAP3L=0EDH CCAP4L=0EEH								
		7	6	5	4	3	2	1	0
	Reset value	0	0	0	0	0	0	0	0

#### Table 14. CH: PCA Counter High

CH Address 0F9H									
		7	6	5	4	3	2	1	0
	Reset value	0	0	0	0	0	0	0	0

#### Table 15. CL: PCA Counter Low

CL Address 0E9H									
		7	6	5	4	3	2	1	0
	Reset value	0	0	0	0	0	0	0	0



### 6.5.2. 16-bit Software Timer / Compare Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set (See Figure 10).



\* Only for Module 4

#### Figure 10. PCA Compare Mode and PCA Watchdog Timer

Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen. Writing to CCAPnH will set the ECOM bit.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.



## 6.5.4. Pulse Width Modulator Mode

All of the PCA modules can be used as PWM outputs. Figure 12 shows the PWM function. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in the module's CCAPLn SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn. This allows updating the PWM without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.



Figure 12. PCA PWM Mode

## 6.5.5. PCA Watchdog Timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed. Figure 10 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

- 1. periodically change the compare value so it will never match the PCA timer,
- 2. periodically change the PCA timer value so it will never match the compare values, or
- 3. disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for all modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

This watchdog timer won't generate a reset out on the reset pin.



### 6.8. Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirely : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occured during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

## 6.9. Power-Down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 17., PCON register).

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated.  $V_{CC}$  can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before  $V_{CC}$  is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts  $\overline{INT0}$  and  $\overline{INT1}$  are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.

Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 17. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C51Rx2 into power-down mode.



#### Figure 17. Power-Down Exit Waveform

Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content. NOTE: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.



# 6.11. ONCE<sup>TM</sup> Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS80C51Rx2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C51Rx2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and  $\overline{\text{PSEN}}$  is high.
- Hold ALE low as RST is deactivated.

While the TS80C51Rx2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 26. shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

#### Table 25. External Pin Status during ONCE Mode

ALE	PSEN	Port 0	Port 1	Port 2	Port 3	XTAL1/2
Weak pull-up	Weak pull-up	Float	Weak pull-up	Weak pull-up	Weak pull-up	Active





Figure 19. Programming and Verification Signal's Waveform

## 8.4. EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

#### 8.4.1. Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm<sup>2</sup>. Exposing the EPROM to an ultraviolet lamp of 12,000  $\mu$ W/cm<sup>2</sup> rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.



## 10.3. DC Parameters for Standard Voltage

TA = 0°C to +70°C; V<sub>SS</sub> = 0 V; V<sub>CC</sub> = 5 V ± 10%; F = 0 to 40 MHz. TA = -40°C to +85°C; V<sub>SS</sub> = 0 V; V<sub>CC</sub> = 5 V ± 10%; F = 0 to 40 MHz.

#### Table 32. DC Parameters in Standard Voltage

Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
V <sub>IL</sub>	Input Low Voltage	-0.5		0.2 V <sub>CC</sub> - 0.1	V	
V <sub>IH</sub>	Input High Voltage except XTAL1, RST	$0.2 V_{CC} + 0.9$		V <sub>CC</sub> + 0.5	V	
V <sub>IH1</sub>	Input High Voltage, XTAL1, RST	0.7 V <sub>CC</sub>		V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage, ports 1, 2, 3, 4, 5 <sup>(6)</sup>			0.3 0.45 1.0	V V V	$I_{OL} = 100 \ \mu A^{(4)}$ $I_{OL} = 1.6 \ m A^{(4)}$ $I_{OL} = 3.5 \ m A^{(4)}$
V <sub>OL1</sub>	Output Low Voltage, port 0 <sup>(6)</sup>			0.3 0.45 1.0	V V V	$I_{OL} = 200 \ \mu A^{(4)}$ $I_{OL} = 3.2 \ m A^{(4)}$ $I_{OL} = 7.0 \ m A^{(4)}$
V <sub>OL2</sub>	Output Low Voltage, ALE, PSEN			0.3 0.45 1.0	V V V	$\begin{split} I_{OL} &= 100 \; \mu A^{(4)} \\ I_{OL} &= 1.6 \; m A^{(4)} \\ I_{OL} &= 3.5 \; m A^{(4)} \end{split}$
V <sub>OH</sub>	Output High Voltage, ports 1, 2, 3, 4, 5	V <sub>CC</sub> - 0.3 V <sub>CC</sub> - 0.7 V <sub>CC</sub> - 1.5			V V V	$\begin{split} I_{OH} &= -10 \; \mu A \\ I_{OH} &= -30 \; \mu A \\ I_{OH} &= -60 \; \mu A \\ V_{CC} &= 5 \; V \pm 10\% \end{split}$
V <sub>OH1</sub>	Output High Voltage, port 0	V <sub>CC</sub> - 0.3 V <sub>CC</sub> - 0.7 V <sub>CC</sub> - 1.5			V V V	$I_{OH} = -200 \ \mu A$ $I_{OH} = -3.2 \ m A$ $I_{OH} = -7.0 \ m A$ $V_{CC} = 5 \ V \pm 10\%$
V <sub>OH2</sub>	Output High Voltage, ALE, PSEN	V <sub>CC</sub> - 0.3 V <sub>CC</sub> - 0.7 V <sub>CC</sub> - 1.5			V V V	$I_{OH} = -100 \ \mu A$ $I_{OH} = -1.6 \ m A$ $I_{OH} = -3.5 \ m A$ $V_{CC} = 5 \ V \pm 10\%$
R <sub>RST</sub>	RST Pulldown Resistor	50	90 <sup>(5)</sup>	200	kΩ	
I <sub>IL</sub>	Logical 0 Input Current ports 1, 2, 3, 4, 5			-50	μΑ	Vin = 0.45 V
I <sub>LI</sub>	Input Leakage Current			±10	μΑ	0.45 V < Vin < V <sub>CC</sub>
I <sub>TL</sub>	Logical 1 to 0 Transition Current, ports 1, 2, 3, 4, 5			-650	μΑ	Vin = 2.0 V
C <sub>IO</sub>	Capacitance of I/O Buffer			10	pF	$Fc = 1 MHz$ $TA = 25^{\circ}C$
I <sub>PD</sub>	Power Down Current		20 <sup>(5)</sup>	50	μΑ	$2.0 \text{ V} < \text{V}_{\text{CC}} < 5.5 \text{ V}^{(3)}$
I <sub>CC</sub> under RESET	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			1 + 0.4 Freq (MHz) @12MHz 5.8 @16MHz 7.4	mA	$V_{CC} = 5.5 V^{(1)}$



Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
I <sub>CC</sub> operating	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			3 + 0.6 Freq (MHz) @12MHz 10.2 @16MHz 12.6	mA	$V_{CC} = 5.5 V^{(8)}$
I <sub>CC</sub> idle	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			0.25+0.3Freq (MHz) @12MHz 3.9 @16MHz 5.1	mA	$V_{CC} = 5.5 V^{(2)}$

## **10.4. DC Parameters for Low Voltage**

TA = 0°C to +70°C; V<sub>SS</sub> = 0 V; V<sub>CC</sub> = 2.7 V to 5.5 V  $\pm$  10%; F = 0 to 30 MHz. TA = -40°C to +85°C; V<sub>SS</sub> = 0 V; V<sub>CC</sub> = 2.7 V to 5.5 V  $\pm$  10%; F = 0 to 30 MHz.

Table 33	. DC	<b>Parameters</b>	for	Low	Voltage
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Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
V <sub>IL</sub>	Input Low Voltage	-0.5		0.2 V <sub>CC</sub> - 0.1	v	
V <sub>IH</sub>	Input High Voltage except XTAL1, RST	$0.2 V_{CC} + 0.9$		V <sub>CC</sub> + 0.5	v	
V <sub>IH1</sub>	Input High Voltage, XTAL1, RST	0.7 V <sub>CC</sub>		V <sub>CC</sub> + 0.5	v	
V <sub>OL</sub>	Output Low Voltage, ports 1, 2, 3, 4, 5 <sup>(6)</sup>			0.45	v	$I_{OL} = 0.8 \text{ mA}^{(4)}$
V <sub>OL1</sub>	Output Low Voltage, port 0, ALE, PSEN (6)			0.45	v	$I_{OL} = 1.6 \text{ mA}^{(4)}$
V <sub>OH</sub>	Output High Voltage, ports 1, 2, 3, 4, 5	0.9 V <sub>CC</sub>			V	$I_{OH} = -10 \ \mu A$
V <sub>OH1</sub>	Output High Voltage, port 0, ALE, PSEN	0.9 V <sub>CC</sub>			v	$I_{OH} = -40 \ \mu A$
I <sub>IL</sub>	Logical 0 Input Current ports 1, 2, 3, 4, 5			-50	μΑ	Vin = 0.45 V
I <sub>LI</sub>	Input Leakage Current			±10	μΑ	0.45 V < Vin < V <sub>CC</sub>
I <sub>TL</sub>	Logical 1 to 0 Transition Current, ports 1, 2, 3, 4, 5			-650	μΑ	Vin = 2.0 V
R <sub>RST</sub>	RST Pulldown Resistor	50	90 <sup>(5)</sup>	200	kΩ	
CIO	Capacitance of I/O Buffer			10	pF	$    Fc = 1 MHz  TA = 25^{\circ}C $
I <sub>PD</sub>	Power Down Current		20 <sup>(5)</sup>	50	μΑ	$V_{\rm CC} = 2.0 \text{ V to } 5.5 \text{ V}^{(3)}$
			10 <sup>(5)</sup>	30		$V_{\rm CC} = 2.0 \text{ V to } 3.3 \text{ V}^{(3)}$
I <sub>CC</sub> under RESET	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			1 + 0.2 Freq (MHz) @12MHz 3.4 @16MHz 4.2	mA	$V_{CC} = 3.3 V^{(1)}$
I <sub>CC</sub> operating	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			1 + 0.3 Freq (MHz) @12MHz 4.6 @16MHz 5.8	mA	$V_{CC} = 3.3 V^{(8)}$



Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
I <sub>CC</sub> idle	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			0.15 Freq (MHz) + 0.2 @12MHz 2 @16MHz 2.6	mA	$V_{CC} = 3.3 V^{(2)}$

NOTES

1.  $I_{CC}$  under reset is measured with all output pins disconnected; XTAL1 driven with  $T_{CLCH}$ ,  $T_{CHCL} = 5$  ns (see Figure 24.),  $V_{IL} = V_{SS} + 0.5$  V,  $V_{IH} = V_{CC} - 0.5$ V; XTAL2 N.C.;  $\overline{EA} = RST = Port \ 0 = V_{CC}$ .  $I_{CC}$  would be slightly higher if a crystal oscillator used.

2. Idle  $I_{CC}$  is measured with all output pins disconnected; XTAL1 driven with  $T_{CLCH}$ ,  $T_{CHCL} = 5$  ns,  $V_{IL} = V_{SS} + 0.5$  V,  $V_{IH} = V_{CC} - 0.5$  V; XTAL2 N.C; Port  $0 = V_{CC}$ ;  $\overline{EA} = RST = V_{SS}$  (see Figure 22.).

3. Power Down  $I_{CC}$  is measured with all output pins disconnected;  $\overline{EA} = V_{SS}$ , PORT  $0 = V_{CC}$ ; XTAL2 NC.; RST =  $V_{SS}$  (see Figure 23.).

4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the  $V_{OL}s$  of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi  $V_{OL}$  peak 0.6V. A Schmitt Trigger use is not necessary.

5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.

6. Under steady state (non-transient) conditions, I<sub>OL</sub> must be externally limited as follows:

Maximum I<sub>OL</sub> per port pin: 10 mA Maximum I<sub>OL</sub> per 8-bit port:

Port 0: 26 mA

Ports 1, 2, 3 and 4 and 5 when available: 15 mA

Maximum total I<sub>OL</sub> for all output pins: 71 mA

If  $I_{OL}$  exceeds the test condition,  $V_{OL}$  may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions. 7. For other values, please contact your sales office.

8. Operating  $I_{CC}$  is measured with all output pins disconnected; XTAL1 driven with  $T_{CLCH}$ ,  $T_{CHCL} = 5$  ns (see Figure 24.),  $V_{IL} = V_{SS} + 0.5$  V,

 $V_{IH} = V_{CC} - 0.5V$ ; XTAL2 N.C.;  $\overline{EA} = Port 0 = V_{CC}$ ; RST =  $V_{SS}$ . The internal ROM runs the code 80 FE (label: SJMP label).  $I_{CC}$  would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.



All other pins are disconnected.

Figure 20. I<sub>CC</sub> Test Condition, under reset



## **10.5.2. External Program Memory Characteristics**

Table 36. Symbol Description	Table 3	36.	Symbol	Description
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Symbol	Parameter
Т	Oscillator clock period
T <sub>LHLL</sub>	ALE pulse width
T <sub>AVLL</sub>	Address Valid to ALE
T <sub>LLAX</sub>	Address Hold After ALE
T <sub>LLIV</sub>	ALE to Valid Instruction In
T <sub>LLPL</sub>	ALE to PSEN
T <sub>PLPH</sub>	PSEN Pulse Width
T <sub>PLIV</sub>	PSEN to Valid Instruction In
T <sub>PXIX</sub>	Input Instruction Hold After PSEN
T <sub>PXIZ</sub>	Input Instruction FloatAfter PSEN
T <sub>PXAV</sub>	PSEN to Address Valid
T <sub>AVIV</sub>	Address to Valid Instruction In
T <sub>PLAZ</sub>	PSEN Low to Address Float

#### Table 37. AC Parameters for Fix Clock

Speed	-1 40 N	М ЛНz	-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Т	25		33		25		50		33		ns
T <sub>LHLL</sub>	40		25		42		35		52		ns
T <sub>AVLL</sub>	10		4		12		5		13		ns
T <sub>LLAX</sub>	10		4		12		5		13		ns
T <sub>LLIV</sub>		70		45		78		65		98	ns
T <sub>LLPL</sub>	15		9		17		10		18		ns
T <sub>PLPH</sub>	55		35		60		50		75		ns
T <sub>PLIV</sub>		35		25		50		30		55	ns
T <sub>PXIX</sub>	0		0		0		0		0		ns
T <sub>PXIZ</sub>		18		12		20		10		18	ns
T <sub>AVIV</sub>		85		53		95		80		122	ns
T <sub>PLAZ</sub>		10		10		10		10		10	ns



Symbol	Туре	Standard Clock	X2 Clock	-M	-V	-L	Units
T <sub>LHLL</sub>	Min	2 T - x	T - x	10	8	15	ns
T <sub>AVLL</sub>	Min	T - x	0.5 T - x	15	13	20	ns
T <sub>LLAX</sub>	Min	T - x	0.5 T - x	15	13	20	ns
T <sub>LLIV</sub>	Max	4 T - x	2 T - x	30	22	35	ns
T <sub>LLPL</sub>	Min	T - x	0.5 T - x	10	8	15	ns
T <sub>PLPH</sub>	Min	3 T - x	1.5 T - x	20	15	25	ns
T <sub>PLIV</sub>	Max	3 T - x	1.5 T - x	40	25	45	ns
T <sub>PXIX</sub>	Min	x	x	0	0	0	ns
T <sub>PXIZ</sub>	Max	T - x	0.5 T - x	7	5	15	ns
T <sub>AVIV</sub>	Max	5 T - x	2.5 T - x	40	30	45	ns
T <sub>PLAZ</sub>	Max	x	x	10	10	10	ns

 Table 38. AC Parameters for a Variable Clock: derating formula

## 10.5.3. External Program Memory Read Cycle



Figure 25. External Program Memory Read Cycle



Speed	-] 40 M	M MHz	X2 1 30 M 60 MH	V node MHz z equiv.	-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T <sub>RLRH</sub>	130		85		135		125		175		ns
T <sub>WLWH</sub>	130		85		135		125		175		ns
T <sub>RLDV</sub>		100		60		102		95		137	ns
T <sub>RHDX</sub>	0		0		0		0		0		ns
T <sub>RHDZ</sub>		30		18		35		25		42	ns
T <sub>LLDV</sub>		160		98		165		155		222	ns
T <sub>AVDV</sub>		165		100		175		160		235	ns
T <sub>LLWL</sub>	50	100	30	70	55	95	45	105	70	130	ns
T <sub>AVWL</sub>	75		47		80		70		103		ns
T <sub>QVWX</sub>	10		7		15		5		13		ns
T <sub>QVWH</sub>	160		107		165		155		213		ns
T <sub>WHQX</sub>	15		9		17		10		18		ns
T <sub>RLAZ</sub>		0		0		0		0		0	ns
T <sub>WHLH</sub>	10	40	7	27	15	35	5	45	13	53	ns

Table 40. AC Parameters for a Fix Clock



Symbol	Туре	Standard Clock	X2 Clock	-M	-V	-L	Units
T <sub>RLRH</sub>	Min	6 T - x	3 T - x	20	15	25	ns
T <sub>WLWH</sub>	Min	6 T - x	3 T - x	20	15	25	ns
T <sub>RLDV</sub>	Max	5 T - x	2.5 T - x	25	23	30	ns
T <sub>RHDX</sub>	Min	x	X	0	0	0	ns
T <sub>RHDZ</sub>	Max	2 T - x	T - x	20	15	25	ns
T <sub>LLDV</sub>	Max	8 T - x	4T -x	40	35	45	ns
T <sub>AVDV</sub>	Max	9 T - x	4.5 T - x	60	50	65	ns
T <sub>LLWL</sub>	Min	3 T - x	1.5 T - x	25	20	30	ns
T <sub>LLWL</sub>	Max	3 T + x	1.5 T + x	25	20	30	ns
T <sub>AVWL</sub>	Min	4 T - x	2 T - x	25	20	30	ns
T <sub>QVWX</sub>	Min	T - x	0.5 T - x	15	10	20	ns
T <sub>QVWH</sub>	Min	7 T - x	3.5 T - x	15	10	20	ns
T <sub>WHQX</sub>	Min	T - x	0.5 T - x	10	8	15	ns
T <sub>RLAZ</sub>	Max	x	х	0	0	0	ns
T <sub>WHLH</sub>	Min	T - x	0.5 T - x	15	10	20	ns
T <sub>WHLH</sub>	Max	T + x	0.5 T + x	15	10	20	ns

Table 41. AC Parameters	for	a	Variable	<b>Clock:</b>	derating	formula
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## 10.5.5. External Data Memory Write Cycle



Figure 26. External Data Memory Write Cycle