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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/ts80c51rd2-lib">https://www.e-xfl.com/product-detail/microchip-technology/ts80c51rd2-lib</a>

## 6. TS80C51Rx2 Enhanced Features

In comparison to the original 80C52, the TS80C51Rx2 implements some new features, which are:

- The X2 option.
- The Dual Data Pointer.
- The extended RAM.
- The Programmable Counter Array (PCA).
- The Watchdog.
- The 4 level interrupt priority system.
- The power-off flag.
- The ONCE mode.
- The ALE disabling.
- Some enhanced features are also located in the UART and the timer 2.

### 6.1. X2 Feature

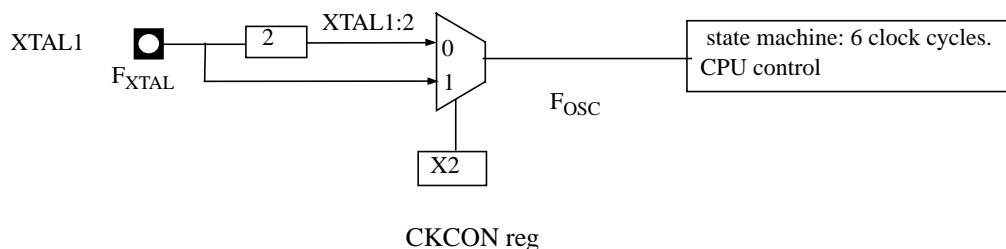
The TS80C51Rx2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

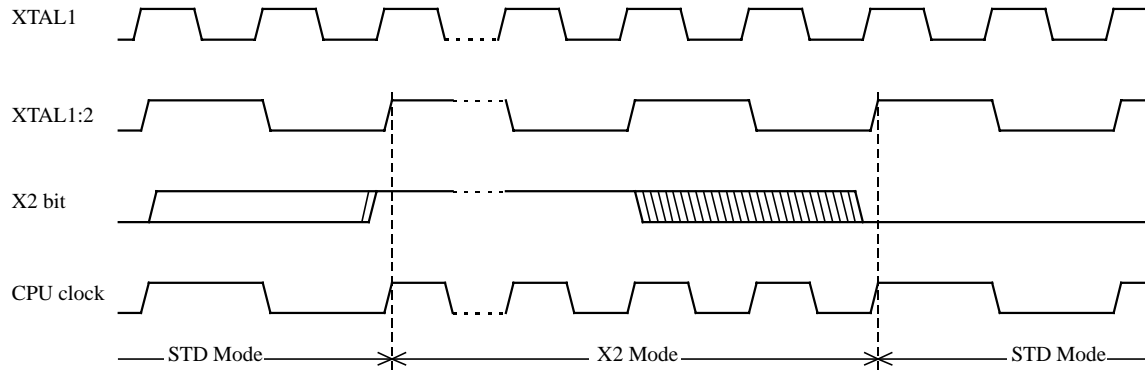
In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

#### 6.1.1. Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 1. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 2. shows the mode switching waveforms.



**Figure 1. Clock Generation Diagram**



**Figure 2. Mode Switching Waveforms**

The X2 bit in the CKCON register (See Table 3.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

#### **CAUTION**

In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers, PCA...) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.

## 6.2. Dual Data Pointer Register Ddptr

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 (See Table 4.) that allows the program code to switch between them (Refer to Figure 3).

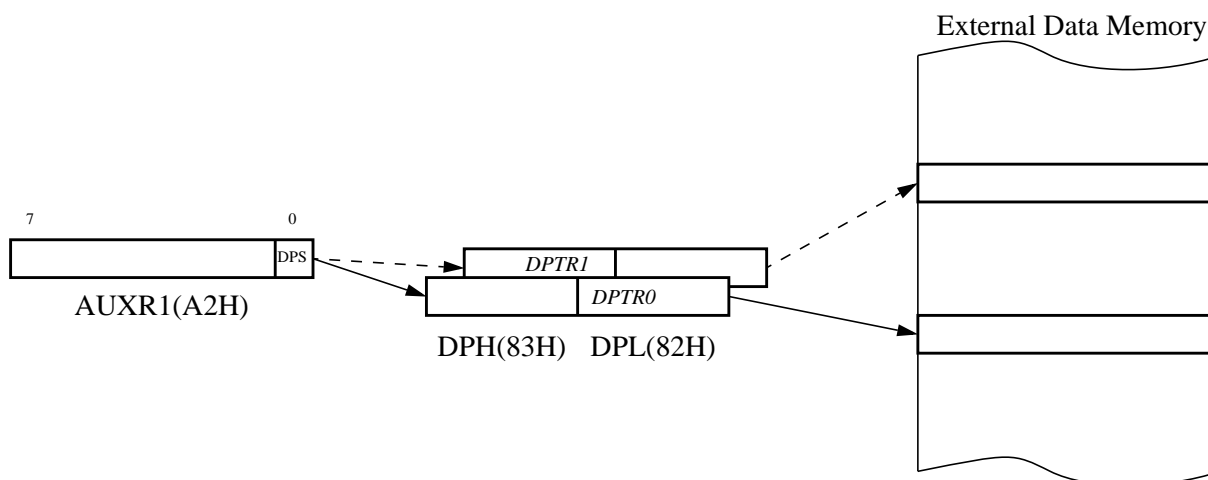


Figure 3. Use of Dual Pointer

Table 4. AUXR1: Auxiliary Register 1

AUXR1 Address 0A2H		-	-	-	-	GF3	-	-	DPS
	Reset value	X	X	X	X	0	X	X	0

Symbol	Function	
-	Not implemented, reserved for future use. <sup>a</sup>	
DPS	Data Pointer Selection.	
	DPS	Operating Mode
	0	DPTR0 Selected
	1	DPTR1 Selected
GF3	This bit is a general purpose user flag <sup>b</sup> .	

- a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new feature. In that case, the reset value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.
- b. GF3 will not be available on first version of the RC devices.

## Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.

**Table 6. T2CON Register**

**T2CON - Timer 2 Control Register (C8h)**

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#

Bit Number	Bit Mnemonic	Description
7	TF2	<b>Timer 2 overflow Flag</b> Must be cleared by software. Set by hardware on timer 2 overflow, if RCLK = 0 and TCLK = 0.
6	EXF2	<b>Timer 2 External Flag</b> Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. When set, causes the CPU to vector to timer 2 interrupt routine when timer 2 interrupt is enabled. Must be cleared by software. EXF2 doesn't cause an interrupt in Up/down counter mode (DCEN = 1)
5	RCLK	<b>Receive Clock bit</b> Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3. Set to use timer 2 overflow as receive clock for serial port in mode 1 or 3.
4	TCLK	<b>Transmit Clock bit</b> Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3. Set to use timer 2 overflow as transmit clock for serial port in mode 1 or 3.
3	EXEN2	<b>Timer 2 External Enable bit</b> Clear to ignore events on T2EX pin for timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port.
2	TR2	<b>Timer 2 Run control bit</b> Clear to turn off timer 2. Set to turn on timer 2.
1	C/T2#	<b>Timer/Counter 2 select bit</b> Clear for timer operation (input from internal clock system: F <sub>OSC</sub> ). Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode.
0	CP/RL2#	<b>Timer 2 Capture/Reload bit</b> If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to auto-reload on timer 2 overflow. Clear to auto-reload on timer 2 overflows or negative transitions on T2EX pin if EXEN2=1. Set to capture on negative transitions on T2EX pin if EXEN2=1.

Reset Value = 0000 0000b

Bit addressable

The **CCON SFR** contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (Refer to Table 9).

- Bit CR (CCON.6) must be set by software to run the PCA. The PCA is shut off by clearing this bit.
- Bit CF: The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software.
- Bits 0 through 4 are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software.

**Table 9. CCON: PCA Counter Control Register**

CCON Address 0D8H		CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0
Reset value		0	0	X	0	0	0	0	0
Symbol	Function								
CF	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.								
CR	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.								
-	Not implemented, reserved for future use. <sup>a</sup>								
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								

- a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

The **watchdog timer** function is implemented in module 4 (See Figure 10).

The **PCA interrupt** system is shown in Figure 8

Table 10. CCAPMn: PCA Modules Compare/Capture Control Registers

CCAPMn Address

n = 0 - 4

CCAPM0=0DAH

CCAPM1=0DBH

CCAPM2=0DCH

CCAPM3=0DDH

CCAPM4=0DEH

	-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn
Reset value	X	0	0	0	0	0	0	0

Symbol	Function
-	Not implemented, reserved for future use. <sup>a</sup>
ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.
CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.
CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.
MATn	Match. When MATn = 1, a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.
TOGn	Toggle. When TOGn = 1, a match of the PCA counter with this module's compare/capture register causes the CEXn pin to toggle.
PWMn	Pulse Width Modulation Mode. PWMn = 1 enables the CEXn pin to be used as a pulse width modulated output.
ECCFn	Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.

- a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

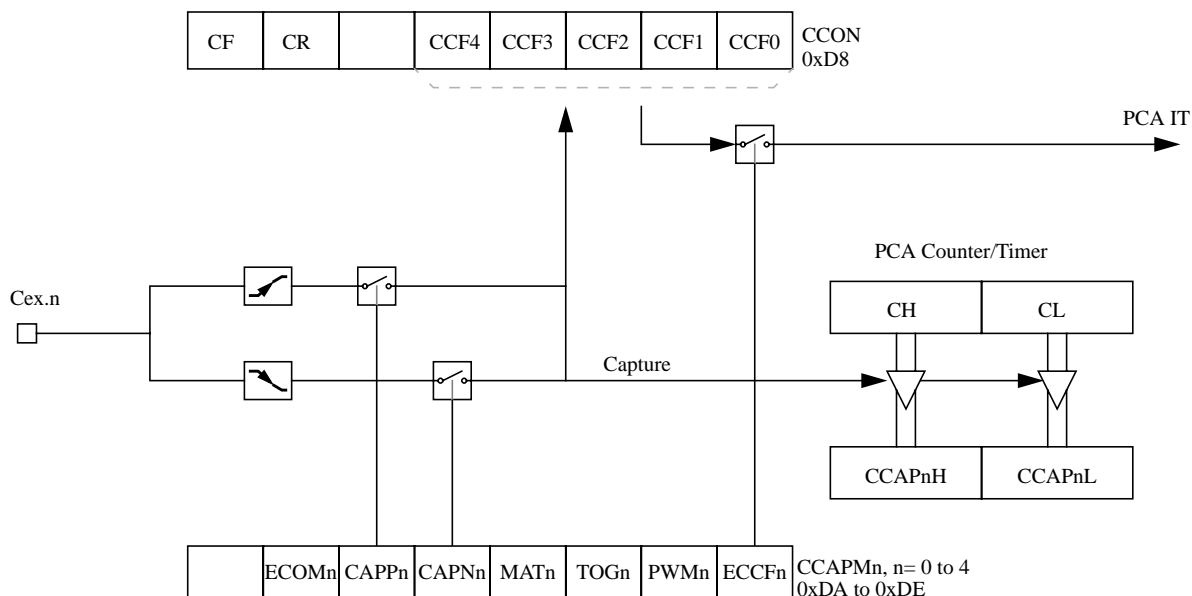
Table 11. PCA Module Modes (CCAPMn Registers)

ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	Module Function
0	0	0	0	0	0	0	No Operation
X	1	0	0	0	0	X	16-bit capture by a positive-edge trigger on CEXn
X	0	1	0	0	0	X	16-bit capture by a negative trigger on CEXn
X	1	1	0	0	0	X	16-bit capture by a transition on CEXn
1	0	0	1	0	0	X	16-bit Software Timer / Compare mode.
1	0	0	1	1	0	X	16-bit High Speed Output
1	0	0	0	0	1	0	8-bit PWM
1	0	0	1	X	0	X	Watchdog Timer (module 4 only)

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output (See Table 12 & Table 13)

### 6.5.1. PCA Capture Mode

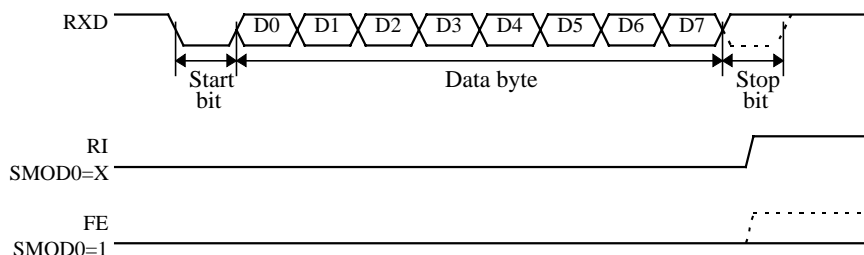
To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated (Refer to Figure 9).



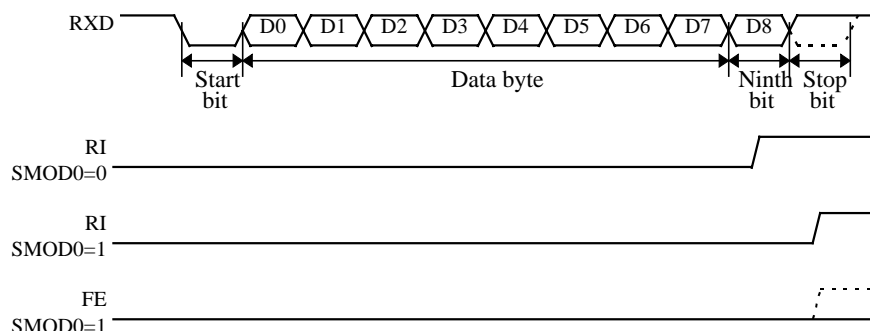
**Figure 9. PCA Capture Mode**



Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 14. and Figure 15.).



**Figure 14. UART Timings in Mode 1**



**Figure 15. UART Timings in Modes 2 and 3**

### 6.6.2. Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

*NOTE: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).*

### 6.6.3. Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed. To address a device by its individual address, the SADEN mask byte must be 1111 1111b.

For example:

SADDR	0101 0110b
SADEN	<u>1111 1100b</u>
Given	0101 01XXb

The following is an example of how to use given addresses to address different slaves:

Slave A:	SADDR	1111 0001b
	SADEN	<u>1111 1010b</u>
	Given	1111 0X0Xb

Slave B:	SADDR	1111 0011b
	SADEN	<u>1111 1001b</u>
	Given	1111 0XX1b

Slave C:	SADDR	1111 0010b
	SADEN	<u>1111 1101b</u>
	Given	1111 00X1b

The SADEN byte is selected so that each slave may be addressed separately.

For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. 1111 0000b).

For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).

To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

### 6.6.4. Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

	SADDR	0101 0110b
	SADEN	1111 1100b
Broadcast = SADDR OR SADEN		1111 111Xb

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

Slave A:	SADDR	1111 0001b
	SADEN	<u>1111 1010b</u>
	Broadcast	1111 1X11b,

Slave B:	SADDR	1111 0011b
	SADEN	<u>1111 1001b</u>
	Broadcast	1111 1X11b,

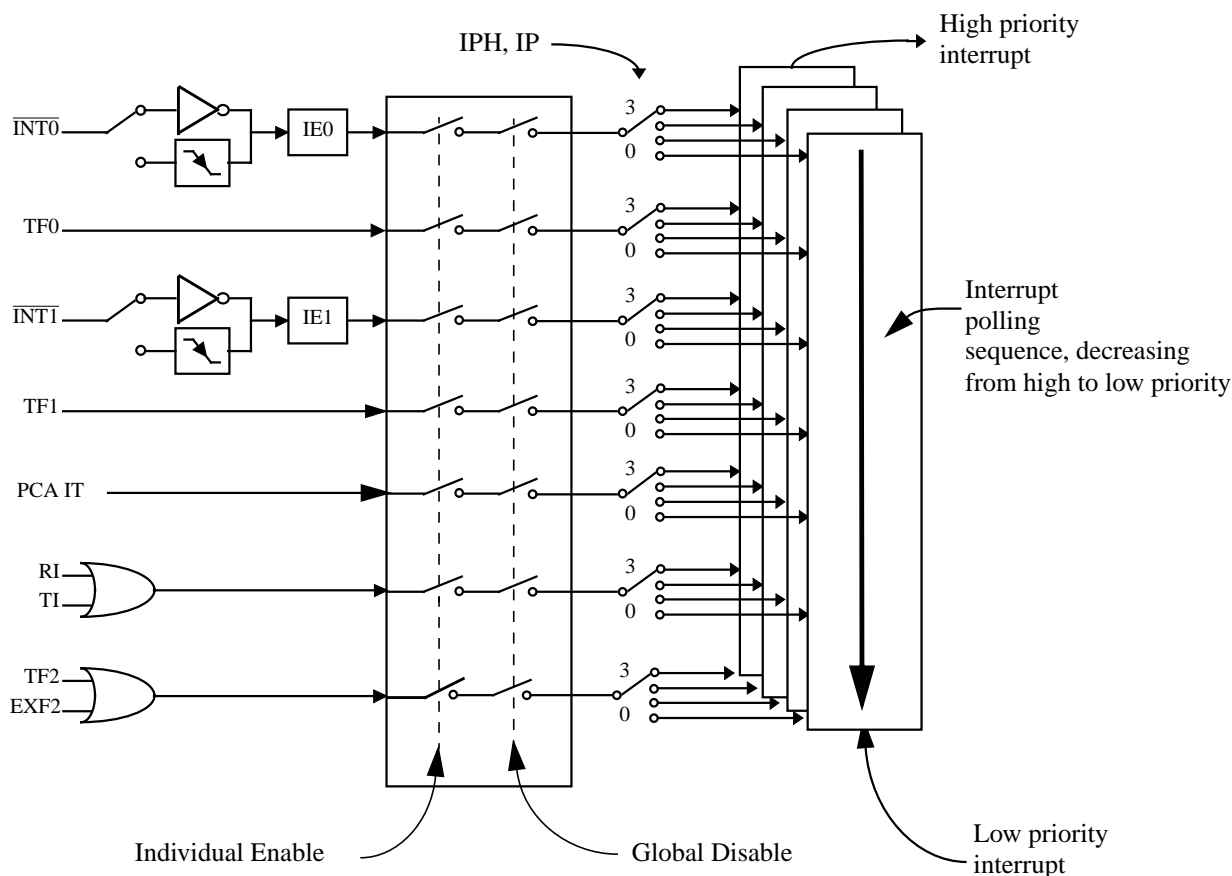
Slave C:	SADDR=	1111 0010b
	SADEN	<u>1111 1101b</u>
	Broadcast	1111 1111b

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send and address FBh.

## 6.7. Interrupt System

The TS80C51Rx2 has a total of 7 interrupt vectors: two external interrupts ( $\overline{\text{INT0}}$  and  $\overline{\text{INT1}}$ ), three timer interrupts (timers 0, 1 and 2), the serial port interrupt and the PCA global interrupt. These interrupts are shown in Figure 16.

**WARNING:** Note that in the first version of RC devices, the PCA interrupt is in the lowest priority. Thus the order in  $\overline{\text{INT0}}$ , TF0,  $\overline{\text{INT1}}$ , TF1, RI or TI, TF2 or EXF2, PCA.



**Figure 16. Interrupt Control System**

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 19.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 20.) and in the Interrupt Priority High register (See Table 21.). shows the bit values and priority levels associated with each combination.

The PCA interrupt vector is located at address 0033H. All other vector addresses are the same as standard C52 devices.

## 6.10. Hardware Watchdog Timer

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer ReSeT (WDTRST) SFR. The WDT is by default disabled from exiting reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST-pin.

### 6.10.1. Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST-pin. The RESET pulse duration is  $96 \times T_{OSC}$ , where  $T_{OSC} = 1/F_{OSC}$ . To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

To have a more powerful WDT, a  $2^7$  counter has been added to extend the Time-out capability, ranking from 16ms to 2s @  $F_{OSC} = 12\text{MHz}$ . To manage this feature, refer to WDTPRG register description, Table 24. (SFR0A7h).

**Table 23. WDTRST Register**

**WDTRST Address (0A6h)**

	7	6	5	4	3	2	1
Reset value	X	X	X	X	X	X	X

Write only, this SFR is used to reset/enable the WDT by writing 01EH then 0E1H in sequence.

## 6.12. Power-Off Flag

The power-off flag allows the user to distinguish between a “cold start” reset and a “warm start” reset.

A cold start reset is the one induced by  $V_{CC}$  switch-on. A warm start reset occurs while  $V_{CC}$  is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 26.). POF is set by hardware when  $V_{CC}$  rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a  $V_{CC}$  range from 4.5V to 5.5V. For lower  $V_{CC}$  value, reading POF bit will return indeterminate value.

**Table 26. PCON Register**

**PCON - Power Control Register (87h)**

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL

Bit Number	Bit Mnemonic	Description
7	SMOD1	<b>Serial port Mode bit 1</b> Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	<b>Serial port Mode bit 0</b> Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	POF	<b>Power-Off Flag</b> Clear to recognize next reset type. Set by hardware when $V_{CC}$ rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	<b>Power-Down mode bit</b> Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	<b>Idle mode bit</b> Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b

Not bit addressable

### 6.13. Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

**Table 27. AUXR Register**

**AUXR - Auxiliary Register (8Eh)**

7	6	5	4	3	2	1	0
-	-	-	-	-	-	EXTRAM	AO

Bit Number	Bit Mnemonic	Description
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
3	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
2	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
1	EXTRAM	<b>EXTRAM bit</b> See Table 5.
0	AO	<b>ALE Output bit</b> Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = XXXX XX00b

Not bit addressable

## 8. TS87C51RB2/RC2/RD2 EPROM

### 8.1. EPROM Structure

The TS87C51RB2/RC2/RD2 EPROM is divided in two different arrays:

- the code array: . . . . . 16/32/64 Kbytes.
- the encryption array: . . . . . 64 bytes.

In addition a third non programmable array is implemented:

- the signature array: . . . . . 4 bytes.

### 8.2. EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

#### 8.2.1. Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

#### 8.2.2. Program Lock Bits

The three lock bits, when programmed according to Table 29.8.2.3. , will provide different level of protection for the on-chip code and data.

**Table 29. Program Lock bits**

Program Lock Bits				Protection description
Security level	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	P	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the EPROM is disabled.
3	U	P	U	Same as 2, also verify is disabled.
4	U	U	P	Same as 3, also external execution is disabled.

U: unprogrammed,

P: programmed

WARNING: Security level 2 and 3 should only be programmed after EPROM and Core verification.

#### 8.2.3. Signature bytes

The TS87C51RB2/RC2/RD2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 8.3.

## 10. Electrical Characteristics

### 10.1. Absolute Maximum Ratings <sup>(1)</sup>

Ambiant Temperature Under Bias:

C = commercial

0°C to 70°C

I = industrial

-40°C to 85°C

Storage Temperature

-65°C to + 150°C

Voltage on  $V_{CC}$  to  $V_{SS}$

-0.5 V to + 7 V

Voltage on  $V_{PP}$  to  $V_{SS}$

-0.5 V to + 13 V

Voltage on Any Pin to  $V_{SS}$

-0.5 V to  $V_{CC} + 0.5$  V

Power Dissipation

1 W<sup>(2)</sup>

#### NOTES

1. Stresses at or above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

### 10.2. Power consumption measurement

Since the introduction of the first C51 devices, every manufacturer made operating  $I_{cc}$  measurements under reset, which made sense for the designs where the CPU was running under reset. In Atmel Wireless & Microcontrollers new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That’s why, while keeping measurements under Reset, Atmel Wireless & Microcontrollers presents a new way to measure the operating  $I_{cc}$ :

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA =  $V_{CC}$ , RST =  $V_{SS}$ , XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating  $I_{cc}$ .



### 10.3. DC Parameters for Standard Voltage

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ;  $V_{SS} = 0\text{ V}$ ;  $V_{CC} = 5\text{ V} \pm 10\%$ ;  $F = 0$  to  $40\text{ MHz}$ .

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ;  $V_{SS} = 0\text{ V}$ ;  $V_{CC} = 5\text{ V} \pm 10\%$ ;  $F = 0$  to  $40\text{ MHz}$ .

**Table 32. DC Parameters in Standard Voltage**

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$V_{IL}$	Input Low Voltage	-0.5		$0.2 V_{CC} - 0.1$	V	
$V_{IH}$	Input High Voltage except XTAL1, RST	$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
$V_{IH1}$	Input High Voltage, XTAL1, RST	$0.7 V_{CC}$		$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage, ports 1, 2, 3, 4, 5 <sup>(6)</sup>			0.3 0.45 1.0	V V V	$I_{OL} = 100\text{ }\mu\text{A}$ <sup>(4)</sup> $I_{OL} = 1.6\text{ mA}$ <sup>(4)</sup> $I_{OL} = 3.5\text{ mA}$ <sup>(4)</sup>
$V_{OL1}$	Output Low Voltage, port 0 <sup>(6)</sup>			0.3 0.45 1.0	V V V	$I_{OL} = 200\text{ }\mu\text{A}$ <sup>(4)</sup> $I_{OL} = 3.2\text{ mA}$ <sup>(4)</sup> $I_{OL} = 7.0\text{ mA}$ <sup>(4)</sup>
$V_{OL2}$	Output Low Voltage, ALE, $\overline{\text{PSEN}}$			0.3 0.45 1.0	V V V	$I_{OL} = 100\text{ }\mu\text{A}$ <sup>(4)</sup> $I_{OL} = 1.6\text{ mA}$ <sup>(4)</sup> $I_{OL} = 3.5\text{ mA}$ <sup>(4)</sup>
$V_{OH}$	Output High Voltage, ports 1, 2, 3, 4, 5	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V V V	$I_{OH} = -10\text{ }\mu\text{A}$ $I_{OH} = -30\text{ }\mu\text{A}$ $I_{OH} = -60\text{ }\mu\text{A}$ $V_{CC} = 5\text{ V} \pm 10\%$
$V_{OH1}$	Output High Voltage, port 0	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V V V	$I_{OH} = -200\text{ }\mu\text{A}$ $I_{OH} = -3.2\text{ mA}$ $I_{OH} = -7.0\text{ mA}$ $V_{CC} = 5\text{ V} \pm 10\%$
$V_{OH2}$	Output High Voltage, ALE, $\overline{\text{PSEN}}$	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V V V	$I_{OH} = -100\text{ }\mu\text{A}$ $I_{OH} = -1.6\text{ mA}$ $I_{OH} = -3.5\text{ mA}$ $V_{CC} = 5\text{ V} \pm 10\%$
$R_{RST}$	RST Pulldown Resistor	50	90 <sup>(5)</sup>	200	k $\Omega$	
$I_{IL}$	Logical 0 Input Current ports 1, 2, 3, 4, 5			-50	$\mu\text{A}$	$V_{in} = 0.45\text{ V}$
$I_{LI}$	Input Leakage Current			$\pm 10$	$\mu\text{A}$	$0.45\text{ V} < V_{in} < V_{CC}$
$I_{TL}$	Logical 1 to 0 Transition Current, ports 1, 2, 3, 4, 5			-650	$\mu\text{A}$	$V_{in} = 2.0\text{ V}$
$C_{IO}$	Capacitance of I/O Buffer			10	pF	$F_c = 1\text{ MHz}$ $T_A = 25^\circ\text{C}$
$I_{PD}$	Power Down Current		20 <sup>(5)</sup>	50	$\mu\text{A}$	$2.0\text{ V} < V_{CC} < 5.5\text{ V}$ <sup>(3)</sup>
$I_{CC}$ under RESET	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			1 + 0.4 Freq (MHz) @12MHz 5.8 @16MHz 7.4	mA	$V_{CC} = 5.5\text{ V}$ <sup>(1)</sup>

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$I_{CC}$ operating	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			3 + 0.6 Freq (MHz) @ 12MHz 10.2 @ 16MHz 12.6	mA	$V_{CC} = 5.5 \text{ V}^{(8)}$
$I_{CC}$ idle	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			0.25+0.3 Freq (MHz) @ 12MHz 3.9 @ 16MHz 5.1	mA	$V_{CC} = 5.5 \text{ V}^{(2)}$

#### 10.4. DC Parameters for Low Voltage

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ;  $V_{SS} = 0 \text{ V}$ ;  $V_{CC} = 2.7 \text{ V}$  to  $5.5 \text{ V} \pm 10\%$ ;  $F = 0$  to  $30 \text{ MHz}$ .

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ;  $V_{SS} = 0 \text{ V}$ ;  $V_{CC} = 2.7 \text{ V}$  to  $5.5 \text{ V} \pm 10\%$ ;  $F = 0$  to  $30 \text{ MHz}$ .

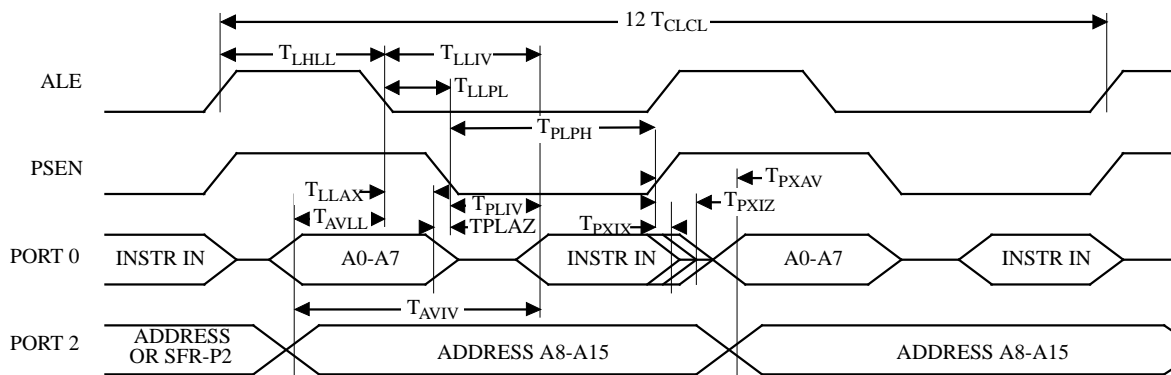
**Table 33. DC Parameters for Low Voltage**

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$V_{IL}$	Input Low Voltage	-0.5		$0.2 V_{CC} - 0.1$	V	
$V_{IH}$	Input High Voltage except XTAL1, RST	$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
$V_{IHI}$	Input High Voltage, XTAL1, RST	$0.7 V_{CC}$		$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage, ports 1, 2, 3, 4, 5 <sup>(6)</sup>			0.45	V	$I_{OL} = 0.8 \text{ mA}^{(4)}$
$V_{OL1}$	Output Low Voltage, port 0, ALE, $\overline{\text{PSEN}}$ <sup>(6)</sup>			0.45	V	$I_{OL} = 1.6 \text{ mA}^{(4)}$
$V_{OH}$	Output High Voltage, ports 1, 2, 3, 4, 5	$0.9 V_{CC}$			V	$I_{OH} = -10 \mu\text{A}$
$V_{OH1}$	Output High Voltage, port 0, ALE, $\overline{\text{PSEN}}$	$0.9 V_{CC}$			V	$I_{OH} = -40 \mu\text{A}$
$I_{IL}$	Logical 0 Input Current ports 1, 2, 3, 4, 5			-50	$\mu\text{A}$	$V_{in} = 0.45 \text{ V}$
$I_{LI}$	Input Leakage Current			$\pm 10$	$\mu\text{A}$	$0.45 \text{ V} < V_{in} < V_{CC}$
$I_{TL}$	Logical 1 to 0 Transition Current, ports 1, 2, 3, 4, 5			-650	$\mu\text{A}$	$V_{in} = 2.0 \text{ V}$
$R_{RST}$	RST Pulldown Resistor	50	90 <sup>(5)</sup>	200	k $\Omega$	
CIO	Capacitance of I/O Buffer			10	pF	$F_c = 1 \text{ MHz}$ $T_A = 25^\circ\text{C}$
$I_{PD}$	Power Down Current		20 <sup>(5)</sup> 10 <sup>(5)</sup>	50 30	$\mu\text{A}$	$V_{CC} = 2.0 \text{ V}$ to $5.5 \text{ V}^{(3)}$ $V_{CC} = 2.0 \text{ V}$ to $3.3 \text{ V}^{(3)}$
$I_{CC}$ under RESET	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			1 + 0.2 Freq (MHz) @ 12MHz 3.4 @ 16MHz 4.2	mA	$V_{CC} = 3.3 \text{ V}^{(1)}$
$I_{CC}$ operating	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			1 + 0.3 Freq (MHz) @ 12MHz 4.6 @ 16MHz 5.8	mA	$V_{CC} = 3.3 \text{ V}^{(8)}$

**Table 38. AC Parameters for a Variable Clock: derating formula**

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
$T_{LHLL}$	Min	$2 T - x$	$T - x$	10	8	15	ns
$T_{AVLL}$	Min	$T - x$	$0.5 T - x$	15	13	20	ns
$T_{LLAX}$	Min	$T - x$	$0.5 T - x$	15	13	20	ns
$T_{LLIV}$	Max	$4 T - x$	$2 T - x$	30	22	35	ns
$T_{LLPL}$	Min	$T - x$	$0.5 T - x$	10	8	15	ns
$T_{PLPH}$	Min	$3 T - x$	$1.5 T - x$	20	15	25	ns
$T_{PLIV}$	Max	$3 T - x$	$1.5 T - x$	40	25	45	ns
$T_{PXIX}$	Min	x	x	0	0	0	ns
$T_{PXIZ}$	Max	$T - x$	$0.5 T - x$	7	5	15	ns
$T_{AVIV}$	Max	$5 T - x$	$2.5 T - x$	40	30	45	ns
$T_{PLAZ}$	Max	x	x	10	10	10	ns

### 10.5.3. External Program Memory Read Cycle



**Figure 25. External Program Memory Read Cycle**

#### 10.5.4. External Data Memory Characteristics

**Table 39. Symbol Description**

Symbol	Parameter
$T_{RLRH}$	$\overline{RD}$ Pulse Width
$T_{WLWH}$	$\overline{WR}$ Pulse Width
$T_{RLDV}$	$\overline{RD}$ to Valid Data In
$T_{RHDX}$	Data Hold After $\overline{RD}$
$T_{RHDZ}$	Data Float After $\overline{RD}$
$T_{LLDV}$	ALE to Valid Data In
$T_{AVDV}$	Address to Valid Data In
$T_{LLWL}$	ALE to $\overline{WR}$ or $\overline{RD}$
$T_{AVWL}$	Address to $\overline{WR}$ or $\overline{RD}$
$T_{QVWX}$	Data Valid to $\overline{WR}$ Transition
$T_{QVWH}$	Data set-up to $\overline{WR}$ High
$T_{WHQX}$	Data Hold After $\overline{WR}$
$T_{RLAZ}$	$\overline{RD}$ Low to Address Float
$T_{WHLH}$	$\overline{RD}$ or $\overline{WR}$ High to ALE high

Table 44. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
$T_{XLXL}$	Min	12 T	6 T				ns
$T_{QVHX}$	Min	10 T - x	5 T - x	50	50	50	ns
$T_{XHQX}$	Min	2 T - x	T - x	20	20	20	ns
$T_{XHDx}$	Min	x	x	0	0	0	ns
$T_{XHDV}$	Max	10 T - x	5 T - x	133	133	133	ns

### 10.5.8. Shift Register Timing Waveforms

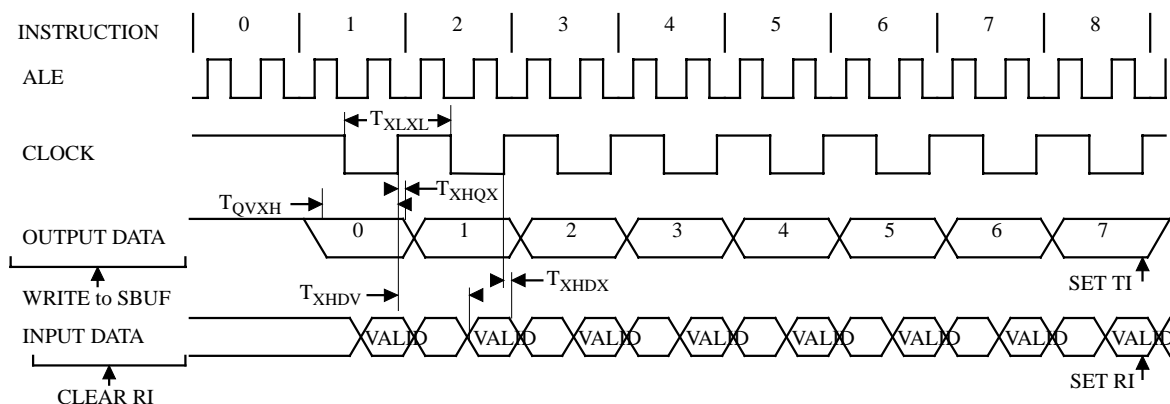


Figure 28. Shift Register Timing Waveforms