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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/30MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	•
Program Memory Type	ROMIess
EEPROM Size	•
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	•
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts80c51rd2-vib

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



	Pin Nu		mber	T	Nome And Eurotian			
Mnemonic	DIL	LCC	VQFP 1.4	Туре	Name And Function			
V _{SS}	20	22	16	Ι	Ground: 0V reference			
Vss1		1	39	Ι	Optional Ground: Contact the Sales Office for ground connection.			
V _{CC}	40	44	38	Ι	Power Supply: This is the power supply voltage for normal, idle and pow down operation			
P0.0-P0.7	39-32	43-36	37-30	I/O	Port 0 : Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have written to them float and can be used as high impedance inputs. Port 0 pins mu be polarized to Vcc or Vss in order to prevent any parasitic current consumptic Port 0 is also the multiplexed low-order address and data bus during access external program and data memory. In this application, it uses strong intern pull-up when emitting 1s. Port 0 also inputs the code bytes during EPRC programming. External pull-ups are required during program verification duri which P0 outputs the code bytes.			
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port pins that have 1s written to them are pulled high by the internal pull-ups ar can be used as inputs. As inputs, Port 1 pins that are externally pulled low wissource current because of the internal pull-ups. Port 1 also receives the low-ord address byte during memory programming and verification. Alternate functions for Port 1 include:			
	1	2	40	I/O	T2 (P1.0): Timer/Counter 2 external count input/Clockout			
	2	3	41	I	T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction Control			
	3	4	42	Ι	ECI (P1.2): External Clock for the PCA			
	4	5	43	I/O	CEX0 (P1.3): Capture/Compare External I/O for PCA module 0			
	5	6	44	I/O	CEX1 (P1.4): Capture/Compare External I/O for PCA module 1			
	6	7	45	I/O	CEX0 (P1.5): Capture/Compare External I/O for PCA module 2			
	7	8	46	I/O	CEX0 (P1.6): Capture/Compare External I/O for PCA module 3			
	8	9	47	I/O	CEX0 (P1.7): Capture/Compare External I/O for PCA module 4			
P2.0-P2.7	21-28	24-31	18-25	I/O	Port 2 : Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR).In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR. Some Port 2 pins (P2.0 to P2.5) receive the high order address bits during EPROM programming and verification:			
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Some Port 3 pins (P3.4 to P3.5) receive the high order address bits during EPROM programming and verification. Port 3 also serves the special features of the 80C51 family, as listed below.			
	10	11	5	I	RXD (P3.0): Serial input port			
	11	13	7	0	TXD (P3.1): Serial output port			
	12	14	8	I	INTO (P3.2): External interrupt 0			
	13	15	9	I	INT1 (P3.3): External interrupt 1			
	14	16	10	I	T0 (P3.4): Timer 0 external input			
	15	17	11	I	T1 (P3.5): Timer 1 external input			
	16	18	12	0	WR (P3.6): External data memory write strobe			
	17	19	13	0	RD (P3.7): External data memory read strobe			



Reset	9	10	4	Ι	Reset: A high on this pin for two machine cycles while the oscillator is running,
					resets the device. An internal diffused resistor to $V_{\mbox{\scriptsize SS}}$ permits a power-on reset
					using only an external capacitor to V_{CC} . If the hardware watchdog reaches its
					time-out, the reset pin becomes an output during the time the internal reset is
					activated.



5.1. Pin Description for 64/68 pin Packages

Port 4 and Port 5 are 8-bit bidirectional I/O ports with internal pull-ups. Pins that have 1 written to them are pulled high by the internal pull ups and can be used as inputs.

As inputs, pins that are externally pulled low will source current because of the internal pull-ups.

Refer to the previous pin description for other pins.

	PLCC68	SQUARE VQFP64 1.4
VSS	51	9/40
VCC	17	8
P0.0	15	6
P0.1	14	5
P0.2	12	3
P0.3	11	2
P0.4	9	64
P0.5	6	61
P0.6	5	60
P0.7	3	59
P1.0	19	10
P1.1	21	12
P1.2	22	13
P1.3	23	14
P1.4	25	16
P1.5	27	18
P1.6	28	19
P1.7	29	20
P2.0	54	43
P2.1	55	44
P2.2	56	45
P2.3	58	47
P2.4	59	48
P2.5	61	50
P2.6	64	53
P2.7	65	54
P3.0	34	25
P3.1	39	28

Table	2.	64/68	Pin	Packages	Configuration
I GOIC		0.00		I uchages	Comparation



Table 3. CKCON Register

CKCON - Clock Control Register (8Fh)

	······································											
7	6	5	4	3	2	1	0					
-	-	-	-	-	-	-	X2					

Bit Number	Bit Mnemonic	Description						
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.						
6	-	eserved The value read from this bit is indeterminate. Do not set this bit.						
5	-	served The value read from this bit is indeterminate. Do not set this bit.						
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.						
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.						
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.						
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.						
0	X2	CPU and peripheral clock bit Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$).						

Reset Value = XXXX XXX0b Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (http://www.atmel-wm.com)





Figure 5. Auto-Reload Mode Up/Down Counter (DCEN = 1)

6.4.2. Programmable Clock-Output

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 6) . The input clock increments TL2 at frequency $F_{OSC}/2$. The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers :

$$Clock - OutFrequency = \frac{F_{osc}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, timer 2 has a programmable frequency range of 61 Hz $(F_{OSC}/2^{16})$ to 4 MHz $(F_{OSC}/4)$. The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear C/T2 bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.
- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or a different one depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.



6.5. Programmable Counter Array PCA

The PCA provides more timing capabilities with less CPU intervention than the standard timer/counters. Its advantages include reduced software overhead and improved accuracy. The PCA consists of a dedicated timer/counter which serves as the time base for an array of five compare/ capture modules. Its clock input can be programmed to count any one of the following signals:

- Oscillator frequency \div 12 (\div 6 in X2 mode)
- Oscillator frequency \div 4 (\div 2 in X2 mode)
- Timer 0 overflow
- External input on ECI (P1.2)

Each compare/capture modules can be programmed in any one of the following modes:

- rising and/or falling edge capture,
- software timer,
- high-speed output, or
- pulse width modulator.

Module 4 can also be programmed as a watchdog timer (See Section "PCA Watchdog Timer", page 33).

When the compare/capture modules are programmed in the capture mode, software timer, or high speed output mode, an interrupt can be generated when the module executes its function. All five modules plus the PCA timer overflow share one interrupt vector.

The PCA timer/counter and compare/capture modules share Port 1 for external I/O. These pins are listed below. If the port is not used for the PCA, it can still be used for standard I/O.

PCA component	External I/O Pin
16-bit Counter	P1.2 / ECI
16-bit Module 0	P1.3 / CEX0
16-bit Module 1	P1.4 / CEX1
16-bit Module 2	P1.5 / CEX2
16-bit Module 3	P1.6 / CEX3
16-bit Module 4	P1.7 / CEX4

The PCA timer is a common time base for all five modules (See Figure 7). The timer count source is determined from the CPS1 and CPS0 bits in the **CMOD SFR** (See Table 8) and can be programmed to run at:

- 1/12 the oscillator frequency. (Or 1/6 in X2 Mode)
- 1/4 the oscillator frequency. (Or 1/2 in X2 Mode)
- The Timer 0 overflow
- The input on the ECI pin (P1.2)





Figure 8. PCA Interrupt System

PCA Modules: each one of the five compare/capture modules has six possible functions. It can perform:

- 16-bit Capture, positive-edge triggered,
- 16-bit Capture, negative-edge triggered,
- 16-bit Capture, both positive and negative-edge triggered,
- 16-bit Software Timer,
- 16-bit High Speed Output,
- 8-bit Pulse Width Modulator.

In addition, module 4 can be used as a Watchdog Timer.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. (See Table 10). The registers contain the bits that control the mode that each module will operate in.

- The ECCF bit (CCAPMn.0 where n=0, 1, 2, 3, or 4 depending on the module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module.
- PWM (CCAPMn.1) enables the pulse width modulation mode.
- The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register.
- The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.
- The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition.
- The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function.

Table 11 shows the CCAPMn settings for the various PCA functions.



6.5.1. PCA Capture Mode

To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated (Refer to Figure 9).



Figure 9. PCA Capture Mode



6.5.4. Pulse Width Modulator Mode

All of the PCA modules can be used as PWM outputs. Figure 12 shows the PWM function. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in the module's CCAPLn SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn. This allows updating the PWM without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.



Figure 12. PCA PWM Mode

6.5.5. PCA Watchdog Timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed. Figure 10 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

- 1. periodically change the compare value so it will never match the PCA timer,
- 2. periodically change the PCA timer value so it will never match the compare values, or
- 3. disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for all modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

This watchdog timer won't generate a reset out on the reset pin.



Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 14. and Figure 15.).







Figure 15. UART Timings in Modes 2 and 3

6.6.2. Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

NOTE: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).



Table 16. SCON Register

SCON - Serial Control Register (98h)

7	6	5	1	0									
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI						
Bit Number	Bit Mnemonic		Description										
7	FE	Framing Error bit Clear to reset the Set by hardware SMOD0 must be	Framing Error bit (SMOD0=1) Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit										
	SM0	Serial port Mode bi Refer to SM1 fo SMOD0 must be	erial port Mode bit 0 Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit										
	6141	Serial port Mode bi SM0 SM	t 1 11 <u>Mode</u>	Description	on Baud Rate	2 2 (/(:= X 2 === 1=)							
6	SMI	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	1 2 3	0Shift Register $F_{XTAL}/12$ (/6 in X2 mode)18-bit UARTVariable29-bit UART $F_{XTAL}/64$ or $F_{XTAL}/32$ (/32, /16 in X2 mode)39-bit UARTVariable									
5	SM2	Serial port Mode 2 bit / Multiprocessor Communication Enable bit Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.											
4	REN	Reception Enable b Clear to disable Set to enable ser	it serial reception. ial reception.										
3	TB8	Transmitter Bit 8 / Clear to transmi Set to transmit a	Ninth bit to trans t a logic 0 in the 9t logic 1 in the 9th b	mit in modes 2 an h bit. bit.	d 3.								
2	RB8	Receiver Bit 8 / Nin Cleared by hard Set by hardware In mode 1, if SM	Receiver Bit 8 / Ninth bit received in modes 2 and 3 Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.										
1	TI	Transmit Interrupt Clear to acknow Set by hardware modes.	flag ledge interrupt. at the end of the 8	th bit time in mode	0 or at the beginn	ing of the stop bit	in the other						
0	RI	Receive Interrupt fl Clear to acknow Set by hardware	ag ledge interrupt. at the end of the 8	th bit time in mode	0, see Figure 14.	and Figure 15. in	the other modes.						

Reset Value = 0000 0000b Bit addressable



Table	22.	The	state	of	ports	during	idle	and	power-down	mode
-------	-----	-----	-------	----	-------	--------	------	-----	------------	------

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data*	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data*	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

* Port 0 can force a "zero" level. A "one" will leave port floating.



6.10. Hardware Watchdog Timer

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer ReSeT (WDTRST) SFR. The WDT is by default disabled from exiting reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST-pin.

6.10.1. Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST-pin. The RESET pulse duration is 96 x T_{OSC} , where $T_{OSC} = 1/F_{OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

To have a more powerful WDT, a 2^7 counter has been added to extend the Time-out capability, ranking from 16ms to 2s @ $F_{OSC} = 12$ MHz. To manage this feature, refer to WDTPRG register description, Table 24. (SFR0A7h).

Table 23. WDTRST Register

WDTRST Address (0A6h)

	7	6	5	4	3	2	1
Reset value	Х	Х	Х	Х	Х	Х	Х

Write only, this SFR is used to reset/enable the WDT by writing 01EH then 0E1H in sequence.





* See Table 31. for proper value on these inputs

Figure 18. Set-Up Modes Configuration

8.3.3. Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the TS87C51RB2/RC2/RD2 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise \overline{EA}/VPP from VCC to VPP (typical 12.75V).
- Step 5: Pulse ALE/PROG once.
- Step 6: Lower \overline{EA}/VPP from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 19.).

8.3.4. Verify algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C51RB2/RC2/RD2.

P 2.7 is used to enable data output.

To verify the TS87C51RB2/RC2/RD2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 19.)

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.



10. Electrical Characteristics

10.1. Absolute Maximum Ratings ⁽¹⁾

Ambiant Temperature Under Bias:	
C = commercial	0°C to 70°C
I = industrial	-40°C to 85°C
Storage Temperature	-65°C to + 150°C
Voltage on V _{CC} to V _{SS}	-0.5 V to + 7 V
Voltage on V _{PP} to V _{SS}	-0.5 V to + 13 V
Voltage on Any Pin to V _{SS}	-0.5 V to V_{CC} + 0.5 V
Power Dissipation	$1 W^{(2)}$

NOTES

1. Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

10.2. Power consumption measurement

Since the introduction of the first C51 devices, every manufacturer made operating Icc measurements under reset, which made sense for the designs were the CPU was running under reset. In Atmel Wireless & Microcontrollers new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That's why, while keeping measurements under Reset, Atmel Wireless & Microcontrollers presents a new way to measure the operating Icc:

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA = Vcc, RST = Vss, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating Icc.



Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
I _{CC} idle	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			0.15 Freq (MHz) + 0.2 @12MHz 2 @16MHz 2.6	mA	$V_{CC} = 3.3 V^{(2)}$

NOTES

1. I_{CC} under reset is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5$ ns (see Figure 24.), $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$ V; XTAL2 N.C.; $\overline{EA} = RST = Port \ 0 = V_{CC}$. I_{CC} would be slightly higher if a crystal oscillator used.

2. Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5$ ns, $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$ V; XTAL2 N.C; Port $0 = V_{CC}$; $\overline{EA} = RST = V_{SS}$ (see Figure 22.).

3. Power Down I_{CC} is measured with all output pins disconnected; $\overline{EA} = V_{SS}$, PORT $0 = V_{CC}$; XTAL2 NC.; RST = V_{SS} (see Figure 23.).

4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the $V_{OL}s$ of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi V_{OL} peak 0.6V. A Schmitt Trigger use is not necessary.

5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.

6. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin: 10 mA Maximum I_{OL} per 8-bit port:

Port 0: 26 mA

Ports 1, 2, 3 and 4 and 5 when available: 15 mA

Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions. 7. For other values, please contact your sales office.

8. Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5$ ns (see Figure 24.), $V_{IL} = V_{SS} + 0.5$ V,

 $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C.; $\overline{EA} = Port 0 = V_{CC}$; RST = V_{SS} . The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.



All other pins are disconnected.

Figure 20. I_{CC} Test Condition, under reset





All other pins are disconnected.





All other pins are disconnected.

Figure 22. I_{CC} Test Condition, Idle Mode



Figure 23. I_{CC} Test Condition, Power-Down Mode



Figure 24. Clock Signal Waveform for $I_{\mbox{\scriptsize CC}}$ Tests in Active and Idle Modes



Symbol	Туре	Standard Clock	X2 Clock	-М	-V	-L	Units
T _{XLXL}	Min	12 T	6 T				ns
T _{QVHX}	Min	10 T - x	5 T - x	50	50	50	ns
T _{XHQX}	Min	2 T - x	T - x	20	20	20	ns
T _{XHDX}	Min	х	Х	0	0	0	ns
T _{XHDV}	Max	10 T - x	5 T- x	133	133	133	ns

Table 44. AC Parameters	for	a	Variable	Clock:	derating	formula
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10.5.8. Shift Register Timing Waveforms



Figure 28. Shift Register Timing Waveforms



10.5.11. External Clock Drive Characteristics (XTAL1)

Table	46.	AC	Parameters
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Symbol	Parameter	Min	Max	Units
T _{CLCL}	Oscillator Period	25		ns
T _{CHCX}	High Time	5		ns
T _{CLCX}	Low Time	5		ns
T _{CLCH}	Rise Time		5	ns
T _{CHCL}	Fall Time		5	ns
T _{CHCX} /T _{CLCX}	Cyclic ratio in X2 mode	40	60	%

10.5.12. External Clock Drive Waveforms



Figure 30. External Clock Drive Waveforms

10.5.13. AC Testing Input/Output Waveforms



Figure 31. AC Testing Input/Output Waveforms

AC inputs during testing are driven at V_{CC} - 0.5 for a logic "1" and 0.45V for a logic "0". Timing measurement are made at V_{IH} min for a logic "1" and V_{IL} max for a logic "0".

10.5.14. Float Waveforms



Figure 32. Float Waveforms



	TS80C51RA2/RD2 ROMless	TS83C51RB2/RC2/RD2zzz ROM	TS87C51RB2/RC2/RD2 OTP
-MCA	Х	Х	X
-MCB	Х	Х	X
-MCE	Х	Х	X
-MCL	RD2 only	RD2 only	RD2 only
-MCM	RD2 only	RD2 only	RD2 only
-VCA	Х	Х	X
-VCB	Х	Х	X
-VCE	Х	Х	X
-VCL	RD2 only	RD2 only	RD2 only
-VCM	RD2 only	RD2 only	RD2 only
-LCA	Х	Х	X
-LCB	Х	Х	X
-LCE	Х	Х	X
-LCL	RD2 only	RD2 only	RD2 only
-LCM	RD2 only	RD2 only	RD2 only
-MIA	Х	Х	X
-MIB	Х	Х	X
-MIE	Х	Х	X
-MIL	RD2 only	RD2 only	RD2 only
-MIM	RD2 only	RD2 only	RD2 only
-VIA	Х	Х	X
-VIB	Х	Х	X
-VIE	Х	Х	X
-VIL	RD2 only	RD2 only	RD2 only
-VIM	RD2 only	RD2 only	RD2 only
-LIA	Х	Х	X
-LIB	Х	Х	X
-LIE	Х	Х	X
-LIL	RD2 only	RD2 only	RD2 only
-LIM	RD2 only	RD2 only	RD2 only
-EA	Х		X
-EB	Х		X
-EE	Х		X
-EL	RD2 only		RD2 only
-EM	RD2 only		RD2 only
-EJ			RC2 and RD2 only
-EK			RC2 and RD2 only
-EN			RD2 only

Table 48. Possible Ordering Entries

• -Ex for samples

- Tape and Reel available for B, E, L and M packages
- Dry pack mandatory for E and M packages