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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/30MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMIess
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-VQFP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts80c51rd2-vie

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



5. Pin Configuration



*NIC: No Internal Connection



Reset	9	10	4	Ι	Reset: A high on this pin for two machine cycles while the oscillator is running,
					resets the device. An internal diffused resistor to $V_{\mbox{\scriptsize SS}}$ permits a power-on reset
					using only an external capacitor to V_{CC} . If the hardware watchdog reaches its
					time-out, the reset pin becomes an output during the time the internal reset is
					activated.



5.1. Pin Description for 64/68 pin Packages

Port 4 and Port 5 are 8-bit bidirectional I/O ports with internal pull-ups. Pins that have 1 written to them are pulled high by the internal pull ups and can be used as inputs.

As inputs, pins that are externally pulled low will source current because of the internal pull-ups.

Refer to the previous pin description for other pins.

	PLCC68	SQUARE VQFP64 1.4
VSS	51	9/40
VCC	17	8
P0.0	15	6
P0.1	14	5
P0.2	12	3
P0.3	11	2
P0.4	9	64
P0.5	6	61
P0.6	5	60
P0.7	3	59
P1.0	19	10
P1.1	21	12
P1.2	22	13
P1.3	23	14
P1.4	25	16
P1.5	27	18
P1.6	28	19
P1.7	29	20
P2.0	54	43
P2.1	55	44
P2.2	56	45
P2.3	58	47
P2.4	59	48
P2.5	61	50
P2.6	64	53
P2.7	65	54
P3.0	34	25
P3.1	39	28

Table	2.	64/68	Pin	Packages	Configuration
I GOIC		0.00		I uchages	Comparation



The CCON SFR contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (Refer to Table 9).

- Bit CR (CCON.6) must be set by software to run the PCA. The PCA is shut off by clearing this bit.
- Bit CF: The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software.
- Bits 0 through 4 are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software.

CC Addres	ON s 0D8H		CF	CR	CCF3	CCF2	CCF1	CCF0		
	Rese	et value	0	0	X	0	0	0	0	0
Syı	nbol	Function								
CF		PCA Count an interrup can only be	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.							
CR		PCA Count by software	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.							be cleared
-		Not implen	nented, res	erved for	future use	a				
CCF4		PCA Modu cleared by	ile 4 inter software.	rupt flag.	Set by ha	rdware wh	en a matc	h or captı	ire occurs.	Must be
CCF3		PCA Modu cleared by	ile 3 inter software.	rupt flag.	Set by ha	rdware wh	en a matc	h or captı	ire occurs.	Must be
CCF2		PCA Modu cleared by	ile 2 inter software.	rupt flag.	Set by ha	rdware wh	en a matc	h or captu	ire occurs.	Must be
CCF1		PCA Modu cleared by	ile 1 inter software.	rupt flag.	Set by ha	rdware wh	en a matc	h or captı	ire occurs.	Must be
CCF0		PCA Modu cleared by	ile 0 inter software.	rupt flag.	Set by ha	rdware wh	en a matc	h or captu	ire occurs.	Must be

 Table 9. CCON: PCA Counter Control Register

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

The watchdog timer function is implemented in module 4 (See Figure 10).

The PCA interrupt system is shown in Figure 8



Table 12	2. CCAPnH:	PCA Modu	es Capture/C	Compare	Registers	High
----------	------------	----------	--------------	---------	-----------	------

CCAPnH Address n = 0 - 4	CCAP0H=0FAH CCAP1H=0FBH CCAP2H=0FCH CCAP3H=0FDH CCAP3H=0FEH								
		7	6	5	4	3	2	1	0
	Reset value	0	0	0	0	0	0	0	0

Table 13. CCAPnL: PCA Modules Capture/Compare Registers Low

CCAPnL Address n = 0 - 4	CCAP0L=0EAH CCAP1L=0EBH CCAP2L=0ECH CCAP3L=0EDH CCAP4L=0EEH								
		7	6	5	4	3	2	1	0
	Reset value	0	0	0	0	0	0	0	0

Table 14. CH: PCA Counter High

CH Address 0F9H									
		7	6	5	4	3	2	1	0
	Reset value	0	0	0	0	0	0	0	0

Table 15. CL: PCA Counter Low

CL Address 0E9H									
		7	6	5	4	3	2	1	0
	Reset value	0	0	0	0	0	0	0	0



6.5.2. 16-bit Software Timer / Compare Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set (See Figure 10).



* Only for Module 4

Figure 10. PCA Compare Mode and PCA Watchdog Timer

Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen. Writing to CCAPnH will set the ECOM bit.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.



6.5.3. High Speed Output Mode

In this mode the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set (See Figure 11).

A prior write must be done to CCAPnL and CCAPnH before writing the ECOMn bit.



Figure 11. PCA High Speed Output Mode

Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.



6.6. TS80C51Rx2 Serial I/O Port

The serial I/O port in the TS80C51Rx2 is compatible with the serial I/O port in the 80C52. It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous

Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

6.6.1. Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 13).



Figure 13. Framing Error Block Diagram

When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 16.) bit is set.



6.6.3. Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed. To address a device by its individual address, the SADEN mask byte must be 1111 1111b. For example:

SADDR	0101 0110b
SADEN	1111 1100b
Given	0101 01XXb

The following is an example of how to use given addresses to address different slaves:

Slave A:	SADDR <u>SADEN</u> Given	1111 0001b <u>1111 1010b</u> 1111 0X0Xb
Slave B:	SADDR <u>SADEN</u> Given	1111 0011b <u>1111 1001b</u> 1111 0XX1b
Slave C:	SADDR <u>SADEN</u> Given	1111 0010b <u>1111 1101b</u> 1111 00X1b

The SADEN byte is selected so that each slave may be addressed separately.

For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. 1111 0000b).

For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).

To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

6.6.4. Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

0101	0110b
1111	1100b
1111	111Xb
	0101 1111 1111

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

Slave A:	SADDR <u>SADEN</u> Broadcast	1111 0001b <u>1111 1010b</u> 1111 1X11b,
Slave B:	SADDR <u>SADEN</u> Broadcast	1111 0011b <u>1111 1001b</u> 1111 1X11B,
Slave C:	SADDR= <u>SADEN</u> Broadcast	1111 0010b <u>1111 1101b</u> 1111 1111b

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send and address FBh.



Table 16. SCON Register

SCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0		
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI		
Bit Number	Bit Mnemonic		Description						
7	FE	Framing Error bit Clear to reset the Set by hardware SMOD0 must be	Framing Error bit (SMOD0=1) Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit						
	SM0	Serial port Mode bi Refer to SM1 fo SMOD0 must be	Serial port Mode bit 0 Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit						
	6141	Serial port Mode bi SM0 SM	tt 1 11 <u>Mode</u>	Description	on Baud Rate	2 2 (/(:= X 2 === 1=)			
6	SMI	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$					2,/16 in X2 mode)		
5	SM2	Serial port Mode 2 bit / Multiprocessor Communication Enable bit Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.							
4	REN	Reception Enable b Clear to disable Set to enable ser	it serial reception. ial reception.						
3	TB8	Transmitter Bit 8 / Clear to transmi Set to transmit a	Ninth bit to trans t a logic 0 in the 9t logic 1 in the 9th b	mit in modes 2 an h bit. bit.	d 3.				
2	RB8	Receiver Bit 8 / Ninth bit received in modes 2 and 3 Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.							
1	TI	Transmit Interrupt flag Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.							
0	RI	Receive Interrupt fl Clear to acknow Set by hardware	ag ledge interrupt. at the end of the 8	th bit time in mode	0, see Figure 14.	and Figure 15. in	the other modes.		

Reset Value = 0000 0000b Bit addressable



6.7. Interrupt System

The TS80C51Rx2 has a total of 7 interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (timers 0, 1 and 2), the serial port interrupt and the PCA global interrupt. These interrupts are shown in Figure 16.

WARNING: Note that in the first version of RC devices, the PCA interrupt is in the lowest priority. Thus the order in INTO, TF0, INT1, TF1, RI or TI, TF2 or EXF2, PCA.



Figure 16. Interrupt Control System

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 19.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 20.) and in the Interrupt Priority High register (See Table 21.). shows the bit values and priority levels associated with each combination.

The PCA interrupt vector is located at address 0033H. All other vector addresses are the same as standard C52 devices.



Table 21. IPH Register

IPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0	
-	РРСН	РТ2Н	PSH	PT1H	PX1H	РТОН	РХОН	
Bit Number	Bit Mnemonic		Description					
7	-	Reserved The value read f	rom this bit is inde	terminate. Do not s	et this bit.			
6	РРСН	PCA interrupt prio <u>PPCH</u> 0 1 1	rity bit high. <u>PPC</u> Prio 0 1 0 1	<u>rity Level</u> Lowest Highest				
5	РТ2Н	Timer 2 overflow in PT2H 0 1 1	terrupt Priority E <u>PT2</u> 0 1 0 1	ligh bit <u>Priority Level</u> Lowest Highest				
4	PSH	Serial port Priority PSH 0 1 1	High bit <u>PS</u> 0 1 0 1	<u>Priority Level</u> Lowest Highest				
3	PT1H	Timer 1 overflow in <u>PT1H</u> 0 0 1 1 1	terrupt Priority E <u>PT1</u> 0 1 0 1 1	ligh bit <u>Priority Level</u> Lowest Highest				
2	PX1H	External interrupt 1 <u>PX1H</u> 0 0 1 1 1	l Priority High bi <u>PX1</u> 0 1 0 1 1	t <u>Priority Level</u> Lowest Highest				
1	РТОН	Timer 0 overflow in <u>PT0H</u> 0 1 1	terrupt Priority E <u>PTO</u> 0 1 0 1 1	ligh bit <u>Priority Level</u> Lowest Highest				
0	РХ0Н	External interrupt (<u>PX0H</u> 0 0 1 1 1) Priority High bi <u>PX0</u> 0 1 0 1	t <u>Priority Level</u> Lowest Highest				

Reset Value = X000 0000b Not bit addressable



6.11. ONCETM Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS80C51Rx2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C51Rx2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and $\overline{\text{PSEN}}$ is high.
- Hold ALE low as RST is deactivated.

While the TS80C51Rx2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 26. shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

Table 25. External Pin Status during ONCE Mode

ALE	PSEN	Port 0	Port 1	Port 2	Port 3	XTAL1/2
Weak pull-up	Weak pull-up	Float	Weak pull-up	Weak pull-up	Weak pull-up	Active



6.13. Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 27. AUXR Register

AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0	
-	-	-	-	-	-	EXTRAM	AO	
Bit Number	Bit Mnemonic	Description						
7	-	Reserved The value read fr	om this bit is inde	terminate. Do not s	set this bit.			
6	-	Reserved The value read fr	om this bit is inde	terminate. Do not s	set this bit.			
5	-	Reserved The value read fr	om this bit is inde	terminate. Do not s	set this bit.			
4	-	Reserved The value read fr	Reserved The value read from this bit is indeterminate. Do not set this bit.					
3	-	Reserved The value read fr	Reserved The value read from this bit is indeterminate. Do not set this bit.					
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.						
1	EXTRAM	EXTRAM bit See Table 5.						
0	AO	ALE Output bit Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.						

Reset Value = XXXX XX00b Not bit addressable



8. TS87C51RB2/RC2/RD2 EPROM

8.1. EPROM Structure

The TS87C51RB2/RC2/RD2 EPROM is divided in two different arrays:

•	the code array:
•	the encryption array:
In	addition a third non programmable array is implemented:
•	the signature array:

8.2. EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

8.2.1. Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

8.2.2. Program Lock Bits

The three lock bits, when programmed according to Table 29.8.2.3., will provide different level of protection for the on-chip code and data.

F	Program Lo	ock Bits		Protection description				
Security level	LB1	LB2	LB3					
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.				
2	Р	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, \overline{EA} is sampled and latched on reset, and further programming of the EPROM is disabled.				
3	U	Р	U	Same as 2, also verify is disabled.				
4	U	U	Р	Same as 3, also external execution is disabled.				

Table 29	. Program	Lock	bits
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U: unprogrammed,

P: programmed

WARNING: Security level 2 and 3 should only be programmed after EPROM and Core verification.

8.2.3. Signature bytes

The TS87C51RB2/RC2/RD2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 8.3.



10.3. DC Parameters for Standard Voltage

TA = 0°C to +70°C; V_{SS} = 0 V; V_{CC} = 5 V ± 10%; F = 0 to 40 MHz. TA = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 5 V ± 10%; F = 0 to 40 MHz.

Table 32. DC Parameters in Standard Voltage

Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
V _{IL}	Input Low Voltage	-0.5		0.2 V _{CC} - 0.1	V	
V _{IH}	Input High Voltage except XTAL1, RST	$0.2 V_{CC} + 0.9$		V _{CC} + 0.5	V	
V _{IH1}	Input High Voltage, XTAL1, RST	0.7 V _{CC}		V _{CC} + 0.5	V	
V _{OL}	Output Low Voltage, ports 1, 2, 3, 4, 5 ⁽⁶⁾			0.3 0.45 1.0	V V V	$I_{OL} = 100 \ \mu A^{(4)}$ $I_{OL} = 1.6 \ m A^{(4)}$ $I_{OL} = 3.5 \ m A^{(4)}$
V _{OL1}	Output Low Voltage, port 0 ⁽⁶⁾			0.3 0.45 1.0	V V V	$I_{OL} = 200 \ \mu A^{(4)}$ $I_{OL} = 3.2 \ m A^{(4)}$ $I_{OL} = 7.0 \ m A^{(4)}$
V _{OL2}	Output Low Voltage, ALE, PSEN			0.3 0.45 1.0	V V V	$\begin{split} I_{OL} &= 100 \; \mu A^{(4)} \\ I_{OL} &= 1.6 \; m A^{(4)} \\ I_{OL} &= 3.5 \; m A^{(4)} \end{split}$
V _{OH}	Output High Voltage, ports 1, 2, 3, 4, 5	V _{CC} - 0.3 V _{CC} - 0.7 V _{CC} - 1.5			V V V	$\begin{split} I_{OH} &= -10 \; \mu A \\ I_{OH} &= -30 \; \mu A \\ I_{OH} &= -60 \; \mu A \\ V_{CC} &= 5 \; V \pm 10\% \end{split}$
V _{OH1}	Output High Voltage, port 0	V _{CC} - 0.3 V _{CC} - 0.7 V _{CC} - 1.5			V V V	$I_{OH} = -200 \ \mu A$ $I_{OH} = -3.2 \ m A$ $I_{OH} = -7.0 \ m A$ $V_{CC} = 5 \ V \pm 10\%$
V _{OH2}	Output High Voltage, ALE, PSEN	V _{CC} - 0.3 V _{CC} - 0.7 V _{CC} - 1.5			V V V	$I_{OH} = -100 \ \mu A$ $I_{OH} = -1.6 \ m A$ $I_{OH} = -3.5 \ m A$ $V_{CC} = 5 \ V \pm 10\%$
R _{RST}	RST Pulldown Resistor	50	90 ⁽⁵⁾	200	kΩ	
I _{IL}	Logical 0 Input Current ports 1, 2, 3, 4, 5			-50	μΑ	Vin = 0.45 V
I _{LI}	Input Leakage Current			±10	μΑ	0.45 V < Vin < V _{CC}
I _{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3, 4, 5			-650	μΑ	Vin = 2.0 V
C _{IO}	Capacitance of I/O Buffer			10	pF	$Fc = 1 MHz$ $TA = 25^{\circ}C$
I _{PD}	Power Down Current		20 ⁽⁵⁾	50	μΑ	$2.0 \text{ V} < \text{V}_{\text{CC}} < 5.5 \text{ V}^{(3)}$
I _{CC} under RESET	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			1 + 0.4 Freq (MHz) @12MHz 5.8 @16MHz 7.4	mA	$V_{CC} = 5.5 V^{(1)}$



Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
I _{CC} idle	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			0.15 Freq (MHz) + 0.2 @12MHz 2 @16MHz 2.6	mA	$V_{CC} = 3.3 V^{(2)}$

NOTES

1. I_{CC} under reset is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5$ ns (see Figure 24.), $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$ V; XTAL2 N.C.; $\overline{EA} = RST = Port \ 0 = V_{CC}$. I_{CC} would be slightly higher if a crystal oscillator used.

2. Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5$ ns, $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$ V; XTAL2 N.C; Port $0 = V_{CC}$; $\overline{EA} = RST = V_{SS}$ (see Figure 22.).

3. Power Down I_{CC} is measured with all output pins disconnected; $\overline{EA} = V_{SS}$, PORT $0 = V_{CC}$; XTAL2 NC.; RST = V_{SS} (see Figure 23.).

4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the $V_{OL}s$ of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi V_{OL} peak 0.6V. A Schmitt Trigger use is not necessary.

5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.

6. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin: 10 mA Maximum I_{OL} per 8-bit port:

Port 0: 26 mA

Ports 1, 2, 3 and 4 and 5 when available: 15 mA

Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions. 7. For other values, please contact your sales office.

8. Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5$ ns (see Figure 24.), $V_{IL} = V_{SS} + 0.5$ V,

 $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C.; $\overline{EA} = Port 0 = V_{CC}$; RST = V_{SS} . The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.



All other pins are disconnected.

Figure 20. I_{CC} Test Condition, under reset



10.5. AC Parameters

10.5.1. Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example: T_{AVLL} = Time for Address Valid to ALE Low. T_{LLPL} = Time for ALE Low to PSEN Low.

TA = 0 to +70°C (commercial temperature range); $V_{SS} = 0$ V; $V_{CC} = 5$ V ± 10%; -M and -V ranges. TA = -40°C to +85°C (industrial temperature range); $V_{SS} = 0$ V; $V_{CC} = 5$ V ± 10%; -M and -V ranges. TA = 0 to +70°C (commercial temperature range); $V_{SS} = 0$ V; 2.7 V < $V_{CC} < 5.5$ V; -L range. TA = -40°C to +85°C (industrial temperature range); $V_{SS} = 0$ V; 2.7 V < $V_{CC} < 5.5$ V; -L range.

Table 34. gives the maximum applicable load capacitance for Port 0, Port 1, 2 and 3, and ALE and $\overline{\text{PSEN}}$ signals. Timings will be guaranteed if these capacitances are respected. Higher capacitance values can be used, but timings will then be degraded.

	-M	-V	-L
Port 0	100	50	100
Port 1, 2, 3	80	50	80
ALE / PSEN	100	30	100

Table 3	4. L	load	Capacitance	versus	speed	range,	in	pF
								- E

Table 36., Table 39. and Table 42. give the description of each AC symbols.

Table 37., Table 40. and Table 43. give for each range the AC parameter.

Table 38., Table 41. and Table 44. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

Table 35. Max frequency for derating formula regarding the speed grade

	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	20	40	30	30	20
T (ns)	25	50	25	33.3	33.3	50

Example:

 T_{LLIV} in X2 mode for a -V part at 20 MHz (T = $1/20^{E6}$ = 50 ns):

x= 22 (Table 38.)

T=50ns

 T_{LLIV} = 2T - x = 2 x 50 - 22 = 78ns



SpeedM 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T _{RLRH}	130		85		135		125		175		ns
T _{WLWH}	130		85		135		125		175		ns
T _{RLDV}		100		60		102		95		137	ns
T _{RHDX}	0		0		0		0		0		ns
T _{RHDZ}		30		18		35		25		42	ns
T _{LLDV}		160		98		165		155		222	ns
T _{AVDV}		165		100		175		160		235	ns
T _{LLWL}	50	100	30	70	55	95	45	105	70	130	ns
T _{AVWL}	75		47		80		70		103		ns
T _{QVWX}	10		7		15		5		13		ns
T _{QVWH}	160		107		165		155		213		ns
T _{WHQX}	15		9		17		10		18		ns
T _{RLAZ}		0		0		0		0		0	ns
T _{WHLH}	10	40	7	27	15	35	5	45	13	53	ns

Table 40. AC Parameters for a Fix Clock



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \ge \pm 20$ mA.

10.5.15. Clock Waveforms

Valid in normal clock mode. In X2 mode XTAL2 signal must be changed to XTAL2 divided by two.



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though ($T_A=25^{\circ}C$ fully loaded) RD and WR propagation delays are approximately 50ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.