



Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-VQFP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c51rb2-lce

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



# 4. SFR Mapping

The Special Function Registers (SFRs) of the TS80C51Rx2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3, P4, P5
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- HDW Watchdog Timer Reset: WDTRST, WDTPRG
- PCA registers: CL, CH, CCAPiL, CCAPiH, CCON, CMOD, CCAPMi
- Interrupt system registers: IE, IP, IPH
- Others: AUXR, CKCON

#### Table 1. All SFRs with their address and their reset value

	Bit addressable	Non Bit addressable							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h		CH 0000 0000	CCAP0H XXXX XXXX	CCAP1H XXXX XXXX	CCAPL2H XXXX XXXX	CCAPL3H XXXX XXXX	CCAPL4H XXXX XXXX		F
F0h	B 0000 0000								F
E8h	P5 bit addressable 1111 1111	CL 0000 0000	CCAP0L XXXX XXXX	CCAP1L XXXX XXXX	CCAPL2L XXXX XXXX	CCAPL3L XXXX XXXX	CCAPL4L XXXX XXXX		E
E0h	ACC 0000 0000								E
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		D
D0h	PSW 0000 0000								D
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			C
C0h	P4 bit addressable 1111 1111							P5 byte addressable 1111 1111	C
B8h	IP X000 000	SADEN 0000 0000							B
B0h	P3 1111 1111							IPH X000 0000	В
A8h	IE 0000 0000	SADDR 0000 0000							A
A0h	P2 1111 1111		AUXR1 XXXX0XX0				WDTRST XXXX XXXX	WDTPRG XXXX X000	A
98h	SCON 0000 0000	SBUF XXXX XXXX							91
90h	P1 1111 1111								9
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXXXX00	CKCON XXXX XXX0	81
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	8
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

reserved



	Pin Number		T		
Mnemonic	DIL	LCC	VQFP 1.4	Туре	Name And Function
V <sub>SS</sub>	20	22	16	Ι	Ground: 0V reference
Vss1		1	39	Ι	Optional Ground: Contact the Sales Office for ground connection.
V <sub>CC</sub>	40	44	38	Ι	<b>Power Supply:</b> This is the power supply voltage for normal, idle and power-down operation
P0.0-P0.7	39-32	43-36	37-30	I/O	<b>Port 0</b> : Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to Vcc or Vss in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes.
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	<b>Port 1:</b> Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification. Alternate functions for Port 1 include:
	1	2	40	I/O	T2 (P1.0): Timer/Counter 2 external count input/Clockout
	2	3	41	I	T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction Control
	3	4	42	Ι	ECI (P1.2): External Clock for the PCA
	4	5	43	I/O	CEX0 (P1.3): Capture/Compare External I/O for PCA module 0
	5	6	44	I/O	CEX1 (P1.4): Capture/Compare External I/O for PCA module 1
	6	7	45	I/O	CEX0 (P1.5): Capture/Compare External I/O for PCA module 2
	7	8	46	I/O	CEX0 (P1.6): Capture/Compare External I/O for PCA module 3
	8	9	47	I/O	CEX0 (P1.7): Capture/Compare External I/O for PCA module 4
P2.0-P2.7	21-28	24-31	18-25	I/O	<b>Port 2</b> : Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR).In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR. Some Port 2 pins (P2.0 to P2.5) receive the high order address bits during EPROM programming and verification:
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	<b>Port 3:</b> Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Some Port 3 pins (P3.4 to P3.5) receive the high order address bits during EPROM programming and verification. Port 3 also serves the special features of the 80C51 family, as listed below.
	10	11	5	I	RXD (P3.0): Serial input port
	11	13	7	0	TXD (P3.1): Serial output port
	12	14	8	I	<b>INTO</b> (P3.2): External interrupt 0
	13	15	9	I	<b>INT1</b> (P3.3): External interrupt 1
	14	16	10	I	T0 (P3.4): Timer 0 external input
	15	17	11	I	T1 (P3.5): Timer 1 external input
	16	18	12	0	WR (P3.6): External data memory write strobe
	17	19	13	0	RD (P3.7): External data memory read strobe



## **5.1. Pin Description for 64/68 pin Packages**

Port 4 and Port 5 are 8-bit bidirectional I/O ports with internal pull-ups. Pins that have 1 written to them are pulled high by the internal pull ups and can be used as inputs.

As inputs, pins that are externally pulled low will source current because of the internal pull-ups.

Refer to the previous pin description for other pins.

	PLCC68	SQUARE VQFP64 1.4
VSS	51	9/40
VCC	17	8
P0.0	15	6
P0.1	14	5
P0.2	12	3
P0.3	11	2
P0.4	9	64
P0.5	6	61
P0.6	5	60
P0.7	3	59
P1.0	19	10
P1.1	21	12
P1.2	22	13
P1.3	23	14
P1.4	25	16
P1.5	27	18
P1.6	28	19
P1.7	29	20
P2.0	54	43
P2.1	55	44
P2.2	56	45
P2.3	58	47
P2.4	59	48
P2.5	61	50
P2.6	64	53
P2.7	65	54
P3.0	34	25
P3.1	39	28

Table	2.	64/68	Pin	Packages	Configuration
I GOIC		0.00		I uchages	Comparation







The X2 bit in the CKCON register (See Table 3.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

#### CAUTION

In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers, PCA...) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.





Figure 4. Internal and External Data Memory Address

AUXR ress 08EH		-	-	-	-	-	-	EXTRA M	AO
Reset	value	X	Х	Х	Х	Х	Х	0	0
Symbol		Function							
-	Not imp	Not implemented, reserved for future use. <sup>a</sup>							
AO	Disable/I	Disable/Enable ALE							
	AO	Op	erating M	ode					
	0	ALI X2	E is emitte mode is u	ed at a cor sed)	istant rate	of 1/6 the	oscillator	frequency (or	r 1/3 if
	1	AL	E is active	only duri	ng a MOV	X or MO	VC instruc	tion	
EXTRAM	Internal/I	External R	AM (00H-	FFH) acce	ess using N	AOVX @	Ri/ @ DP	TR	
	EXTR	AM Op	Operating Mode						
	0	Inte	rnal XRA	M access	using MOV	/X @ Ri/	@ DPTR		
	1	Ext	ernal data	memory a	ccess				

 Table 5. Auxiliary Register AUXR

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.



## 6.5. Programmable Counter Array PCA

The PCA provides more timing capabilities with less CPU intervention than the standard timer/counters. Its advantages include reduced software overhead and improved accuracy. The PCA consists of a dedicated timer/counter which serves as the time base for an array of five compare/ capture modules. Its clock input can be programmed to count any one of the following signals:

- Oscillator frequency  $\div$  12 ( $\div$  6 in X2 mode)
- Oscillator frequency  $\div$  4 ( $\div$  2 in X2 mode)
- Timer 0 overflow
- External input on ECI (P1.2)

Each compare/capture modules can be programmed in any one of the following modes:

- rising and/or falling edge capture,
- software timer,
- high-speed output, or
- pulse width modulator.

Module 4 can also be programmed as a watchdog timer (See Section "PCA Watchdog Timer", page 33).

When the compare/capture modules are programmed in the capture mode, software timer, or high speed output mode, an interrupt can be generated when the module executes its function. All five modules plus the PCA timer overflow share one interrupt vector.

The PCA timer/counter and compare/capture modules share Port 1 for external I/O. These pins are listed below. If the port is not used for the PCA, it can still be used for standard I/O.

PCA component	External I/O Pin
16-bit Counter	P1.2 / ECI
16-bit Module 0	P1.3 / CEX0
16-bit Module 1	P1.4 / CEX1
16-bit Module 2	P1.5 / CEX2
16-bit Module 3	P1.6 / CEX3
16-bit Module 4	P1.7 / CEX4

**The PCA timer** is a common time base for all five modules (See Figure 7). The timer count source is determined from the CPS1 and CPS0 bits in the **CMOD SFR** (See Table 8) and can be programmed to run at:

- 1/12 the oscillator frequency. (Or 1/6 in X2 Mode)
- 1/4 the oscillator frequency. (Or 1/2 in X2 Mode)
- The Timer 0 overflow
- The input on the ECI pin (P1.2)



## 6.5.1. PCA Capture Mode

To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated (Refer to Figure 9).



Figure 9. PCA Capture Mode



## 6.5.4. Pulse Width Modulator Mode

All of the PCA modules can be used as PWM outputs. Figure 12 shows the PWM function. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in the module's CCAPLn SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn. This allows updating the PWM without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.



Figure 12. PCA PWM Mode

## 6.5.5. PCA Watchdog Timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed. Figure 10 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

- 1. periodically change the compare value so it will never match the PCA timer,
- 2. periodically change the PCA timer value so it will never match the compare values, or
- 3. disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for all modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

This watchdog timer won't generate a reset out on the reset pin.



## 6.6. TS80C51Rx2 Serial I/O Port

The serial I/O port in the TS80C51Rx2 is compatible with the serial I/O port in the 80C52. It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous

Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

### 6.6.1. Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 13).



### Figure 13. Framing Error Block Diagram

When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 16.) bit is set.



Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 14. and Figure 15.).







Figure 15. UART Timings in Modes 2 and 3

### 6.6.2. Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

NOTE: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).



## Table 16. SCON Register

#### SCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0				
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI				
Bit Number	Bit Mnemonic		Description								
7	FE	Framing Error bit Clear to reset the Set by hardware SMOD0 must be	<ul> <li>'aming Error bit (SMOD0=1)</li> <li>Clear to reset the error state, not cleared by a valid stop bit.</li> <li>Set by hardware when an invalid stop bit is detected.</li> <li>SMOD0 must be set to enable access to the FE bit</li> </ul>								
	SM0	Serial port Mode bi Refer to SM1 fo SMOD0 must be	rial port Mode bit 0 Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit								
	6141	Serial port Mode bi SM0 SM	t 1 11 <u>Mode</u>	Description	on Baud Rate	2 2 (/( := <b>X</b> 2 === 1=)					
6	SMI	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	1 2 3	8-bit UAI 9-bit UAI 9-bit UAI	RT F <sub>XTAL</sub> /I RT Variable RT F <sub>XTAL</sub> /6 RT Variable	2 (/6 in X2 mode) 4 or F <sub>XTAL</sub> /32 (/32	2,/16 in X2 mode)				
5	SM2	Serial port Mod Clear to disable Set to enable mu be cleared in mo	Serial port Mode 2 bit / Multiprocessor Communication Enable bit Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.								
4	REN	Reception Enable b Clear to disable Set to enable ser	it serial reception. ial reception.								
3	TB8	Transmitter Bit 8 / Clear to transmi Set to transmit a	Ninth bit to trans t a logic 0 in the 9t logic 1 in the 9th b	<b>mit in modes 2 an</b> h bit. bit.	d 3.						
2	RB8	Receiver Bit 8 / Nin Cleared by hard Set by hardware In mode 1, if SM	th bit received in a ware if 9th bit received if 9th bit received $12 = 0$ , RB8 is the particular to the second s	modes 2 and 3 ived is a logic 0. is a logic 1. received stop bit. In	n mode 0 RB8 is n	ot used.					
1	TI	Transmit Interrupt Clear to acknow Set by hardware modes.	flag ledge interrupt. at the end of the 8	th bit time in mode	0 or at the beginn	ing of the stop bit	in the other				
0	RI	Receive Interrupt fl Clear to acknow Set by hardware	<b>ag</b> ledge interrupt. at the end of the 8	th bit time in mode	0, see Figure 14.	and Figure 15. in	the other modes.				

Reset Value = 0000 0000b Bit addressable



#### Table 18. Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

#### Table 19. IE Register

#### IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	EC	ET2	ES	ET1	EX1	ЕТО	EX0

Bit Number	Bit Mnemonic	Description
7	EA	Enable All interrupt bit Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.
6	EC	PCA interrupt enable bit Clear to disable . Set to enable.
5	ET2	Timer 2 overflow interrupt Enable bit Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	Serial port Enable bit Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	Timer 1 overflow interrupt Enable bit         Clear to disable timer 1 overflow interrupt.         Set to enable timer 1 overflow interrupt.
2	EX1	External interrupt 1 Enable bit Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	Timer 0 overflow interrupt Enable bit         Clear to disable timer 0 overflow interrupt.         Set to enable timer 0 overflow interrupt.
0	EX0	External interrupt 0 Enable bit Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0000 0000b Bit addressable



#### Table 20. IP Register

#### **IP - Interrupt Priority Register (B8h)**

7	6	5	4	3	2	1	0
-	PPC	PT2	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	PPC	PCA interrupt priority bit Refer to PPCH for priority level.
5	PT2	Timer 2 overflow interrupt Priority bit Refer to PT2H for priority level.
4	PS	Serial port Priority bit Refer to PSH for priority level.
3	PT1	Timer 1 overflow interrupt Priority bit Refer to PT1H for priority level.
2	PX1	External interrupt 1 Priority bit Refer to PX1H for priority level.
1	PT0	Timer 0 overflow interrupt Priority bit Refer to PT0H for priority level.
0	PX0	External interrupt 0 Priority bit Refer to PX0H for priority level.

Reset Value = X000 0000b Bit addressable



### 6.10. Hardware Watchdog Timer

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer ReSeT (WDTRST) SFR. The WDT is by default disabled from exiting reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST-pin.

### 6.10.1. Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST-pin. The RESET pulse duration is 96 x  $T_{OSC}$ , where  $T_{OSC} = 1/F_{OSC}$ . To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

To have a more powerful WDT, a  $2^7$  counter has been added to extend the Time-out capability, ranking from 16ms to 2s @  $F_{OSC} = 12$ MHz. To manage this feature, refer to WDTPRG register description, Table 24. (SFR0A7h).

#### Table 23. WDTRST Register

#### WDTRST Address (0A6h)

	7	6	5	4	3	2	1
Reset value	Х	Х	Х	Х	Х	Х	Х

Write only, this SFR is used to reset/enable the WDT by writing 01EH then 0E1H in sequence.



#### Table 24. WDTPRG Register

7	6		5	4	3	2	1	0	
T4	Т3	T2         T1         T0         S2         S1				S1	<b>S0</b>		
Bit Number	Bit Mnemonic		Description						
7	T4								
6	T3								
5	T2	Reserve Do 1	d not try to set	or clear this bit.					
4	T1								
3	TO								
2	S2	WDT Ti	WDT Time-out select bit 2						
1	S1	WDT Ti	WDT Time-out select bit 1						
0	SO	WDT Ti	WDT Time-out select bit 0						
			<u>S1</u> 0 1 1 0 0 1 1	$\begin{array}{c cccc} \underline{S0} & \underline{Selecter} \\ 0 & (2^{14} - 1) \\ 1 & (2^{15} - 1) \\ 0 & (2^{16} - 1) \\ 1 & (2^{17} - 1) \\ 0 & (2^{18} - 1) \\ 1 & (2^{19} - 1) \\ 0 & (2^{20} - 1) \\ 1 & (2^{21} - 1) \end{array}$	1 Time-out 9 machine cycles, 10 9 machine cycles, 32 9 machine cycles, 63 9 machine cycles, 12 9 machine cycles, 20 9 machine cycles, 55 9 machine cycles, 1 9 machine cycles, 1 9 machine cycles, 2	5.3 ms @ 12 MHz 2.7 ms @ 12 MHz 5.5 ms @ 12 MHz 31 ms @ 12 MHz 62 ms @ 12 MHz 42 ms @ 12 MHz 05 s @ 12 MHz 09 s @ 12 MHz			

Reset value XXXX X000

### 6.10.2. WDT during Power Down and Idle

In Power Down mode the oscillator stops, which means the WDT also stops. While in Power Down mode the user does not need to service the WDT. There are 2 methods of exiting Power Down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power Down mode. When Power Down is exited with hardware reset, servicing the WDT should occur as it normally should whenever the TS80C51Rx2 is reset. Exiting Power Down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service routine.

To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is best to reset the WDT just before entering powerdown.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting the TS80C51Rx2 while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

## WDTPRG Address (0A7h)



## 6.12. Power-Off Flag

The power-off flag allows the user to distinguish between a "cold start" reset and a "warm start" reset.

A cold start reset is the one induced by  $V_{CC}$  switch-on. A warm start reset occurs while  $V_{CC}$  is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 26.). POF is set by hardware when  $V_{CC}$  rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a Vcc range from 4.5V to 5.5V. For lower Vcc value, reading POF bit will return indeterminate value.

#### Table 26. PCON Register

#### PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0	
SMOD1	SMOD	-	POF	GF1	GF0	PD	IDL	
Bit Number	Bit Mnemonic			Descrip	tion			
7	SMOD1	Serial port Mode bit Set to select dou	Serial port Mode bit 1 Set to select double baud rate in mode 1, 2 or 3.					
6	SMOD0	Serial port Mode bit Clear to select SI Set to to select F	erial port Mode bit 0 Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.					
5	-	<b>Reserved</b> The value read fr	Reserved The value read from this bit is indeterminate. Do not set this bit.					
4	POF	Power-Off Flag Clear to recognize next reset type. Set by hardware when V <sub>CC</sub> rises from 0 to its nominal voltage. Can also be set by software.						
3	GF1	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.						
2	GF0	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.						
1	PD	Power-Down mode I Cleared by hardw Set to enter powe	Power-Down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.					
0	IDL	Idle mode bit Clear by hardware when interrupt or reset occurs. Set to enter idle mode.						

Reset Value = 00X1 0000b Not bit addressable



## 8. TS87C51RB2/RC2/RD2 EPROM

## 8.1. EPROM Structure

The TS87C51RB2/RC2/RD2 EPROM is divided in two different arrays:

•	the code array:
•	the encryption array:
In	addition a third non programmable array is implemented:
•	the signature array:

## 8.2. EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

### 8.2.1. Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

### 8.2.2. Program Lock Bits

The three lock bits, when programmed according to Table 29.8.2.3., will provide different level of protection for the on-chip code and data.

F	Program Lo	ock Bits		Protection description		
Security level	LB1	LB2	LB3			
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.		
2	Р	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the EPROM is disabled.		
3	U	Р	U	Same as 2, also verify is disabled.		
4	U	U	Р	Same as 3, also external execution is disabled.		

Table 29	. Program	Lock	bits
----------	-----------	------	------

U: unprogrammed,

P: programmed

WARNING: Security level 2 and 3 should only be programmed after EPROM and Core verification.

### 8.2.3. Signature bytes

The TS87C51RB2/RC2/RD2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 8.3.





\* See Table 31. for proper value on these inputs

Figure 18. Set-Up Modes Configuration

### 8.3.3. Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the TS87C51RB2/RC2/RD2 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise  $\overline{EA}/VPP$  from VCC to VPP (typical 12.75V).
- Step 5: Pulse ALE/PROG once.
- Step 6: Lower  $\overline{EA}/VPP$  from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 19.).

### 8.3.4. Verify algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C51RB2/RC2/RD2.

P 2.7 is used to enable data output.

To verify the TS87C51RB2/RC2/RD2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 19.)

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.



## 10.3. DC Parameters for Standard Voltage

TA = 0°C to +70°C; V<sub>SS</sub> = 0 V; V<sub>CC</sub> = 5 V ± 10%; F = 0 to 40 MHz. TA = -40°C to +85°C; V<sub>SS</sub> = 0 V; V<sub>CC</sub> = 5 V ± 10%; F = 0 to 40 MHz.

#### Table 32. DC Parameters in Standard Voltage

Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
V <sub>IL</sub>	Input Low Voltage	-0.5		0.2 V <sub>CC</sub> - 0.1	V	
V <sub>IH</sub>	Input High Voltage except XTAL1, RST	$0.2 V_{CC} + 0.9$		V <sub>CC</sub> + 0.5	v	
V <sub>IH1</sub>	Input High Voltage, XTAL1, RST	0.7 V <sub>CC</sub>		V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage, ports 1, 2, 3, 4, 5 <sup>(6)</sup>			0.3 0.45 1.0	V V V	$I_{OL} = 100 \ \mu A^{(4)}$ $I_{OL} = 1.6 \ m A^{(4)}$ $I_{OL} = 3.5 \ m A^{(4)}$
V <sub>OL1</sub>	Output Low Voltage, port 0 <sup>(6)</sup>			0.3 0.45 1.0	V V V	$I_{OL} = 200 \ \mu A^{(4)}$ $I_{OL} = 3.2 \ m A^{(4)}$ $I_{OL} = 7.0 \ m A^{(4)}$
V <sub>OL2</sub>	Output Low Voltage, ALE, PSEN			0.3 0.45 1.0	V V V	$\begin{split} I_{OL} &= 100 \; \mu A^{(4)} \\ I_{OL} &= 1.6 \; m A^{(4)} \\ I_{OL} &= 3.5 \; m A^{(4)} \end{split}$
V <sub>OH</sub>	Output High Voltage, ports 1, 2, 3, 4, 5	V <sub>CC</sub> - 0.3 V <sub>CC</sub> - 0.7 V <sub>CC</sub> - 1.5			V V V	$\begin{split} I_{OH} &= -10 \; \mu A \\ I_{OH} &= -30 \; \mu A \\ I_{OH} &= -60 \; \mu A \\ V_{CC} &= 5 \; V \pm 10\% \end{split}$
V <sub>OH1</sub>	Output High Voltage, port 0	V <sub>CC</sub> - 0.3 V <sub>CC</sub> - 0.7 V <sub>CC</sub> - 1.5			V V V	$I_{OH} = -200 \ \mu A$ $I_{OH} = -3.2 \ m A$ $I_{OH} = -7.0 \ m A$ $V_{CC} = 5 \ V \pm 10\%$
V <sub>OH2</sub>	Output High Voltage, ALE, PSEN	V <sub>CC</sub> - 0.3 V <sub>CC</sub> - 0.7 V <sub>CC</sub> - 1.5			V V V	$I_{OH} = -100 \ \mu A$ $I_{OH} = -1.6 \ m A$ $I_{OH} = -3.5 \ m A$ $V_{CC} = 5 \ V \pm 10\%$
R <sub>RST</sub>	RST Pulldown Resistor	50	90 <sup>(5)</sup>	200	kΩ	
I <sub>IL</sub>	Logical 0 Input Current ports 1, 2, 3, 4, 5			-50	μΑ	Vin = 0.45 V
I <sub>LI</sub>	Input Leakage Current			±10	μΑ	0.45 V < Vin < V <sub>CC</sub>
I <sub>TL</sub>	Logical 1 to 0 Transition Current, ports 1, 2, 3, 4, 5			-650	μA	Vin = 2.0 V
C <sub>IO</sub>	Capacitance of I/O Buffer			10	pF	$Fc = 1 MHz$ $TA = 25^{\circ}C$
I <sub>PD</sub>	Power Down Current		20 (5)	50	μΑ	$2.0 \ V < V_{CC} < 5.5 \ V^{(3)}$
I <sub>CC</sub> under RESET	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			1 + 0.4 Freq (MHz) @12MHz 5.8 @16MHz 7.4	mA	$V_{CC} = 5.5 V^{(1)}$



## **10.5.4. External Data Memory Characteristics**

Table 57. Symbol Description						
Symbol	Parameter					
T <sub>RLRH</sub>	RD Pulse Width					
T <sub>WLWH</sub>	WR Pulse Width					
T <sub>RLDV</sub>	RD to Valid Data In					
T <sub>RHDX</sub>	Data Hold After RD					
T <sub>RHDZ</sub>	Data Float After RD					
T <sub>LLDV</sub>	ALE to Valid Data In					
T <sub>AVDV</sub>	Address to Valid Data In					
T <sub>LLWL</sub>	ALE to WR or RD					
T <sub>AVWL</sub>	Address to WR or RD					
T <sub>QVWX</sub>	Data Valid to WR Transition					
T <sub>QVWH</sub>	Data set-up to WR High					
T <sub>WHQX</sub>	Data Hold After WR					
T <sub>RLAZ</sub>	RD Low to Address Float					
T <sub>WHLH</sub>	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE high					

### Table 39. Symbol Description