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Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIL
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c51rb2-mca

5.1. Pin Description for 64/68 pin Packages

Port 4 and Port 5 are 8-bit bidirectional I/O ports with internal pull-ups. Pins that have 1 written to them are pulled high by the internal pull ups and can be used as inputs.

As inputs, pins that are externally pulled low will source current because of the internal pull-ups.

Refer to the previous pin description for other pins.

Table 2. 64/68 Pin Packages Configuration

	PLCC68	SQUARE VQFP64 1.4
VSS	51	9/40
VCC	17	8
P0.0	15	6
P0.1	14	5
P0.2	12	3
P0.3	11	2
P0.4	9	64
P0.5	6	61
P0.6	5	60
P0.7	3	59
P1.0	19	10
P1.1	21	12
P1.2	22	13
P1.3	23	14
P1.4	25	16
P1.5	27	18
P1.6	28	19
P1.7	29	20
P2.0	54	43
P2.1	55	44
P2.2	56	45
P2.3	58	47
P2.4	59	48
P2.5	61	50
P2.6	64	53
P2.7	65	54
P3.0	34	25
P3.1	39	28

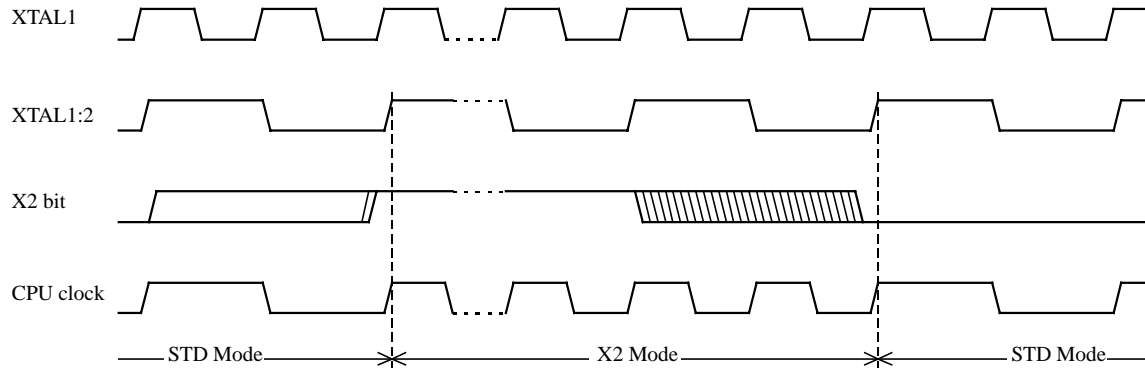


Figure 2. Mode Switching Waveforms

The X2 bit in the CKCON register (See Table 3.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

CAUTION

In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers, PCA...) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.

Table 3. CKCON Register

CKCON - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	X2

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	X2	CPU and peripheral clock bit Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$).

Reset Value = XXXX XXX0b

Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (<http://www.atmel-wm.com>)

ASSEMBLY LANGUAGE

```

; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2          AUXR1 EQU 0A2H
;
0000 909000    MOV DPTR,#SOURCE      ; address of SOURCE
0003 05A2      INC  AUXR1             ; switch data pointers
0005 90A000    MOV DPTR,#DEST        ; address of DEST
0008          LOOP:
0008 05A2      INC  AUXR1             ; switch data pointers
000A E0        MOVX A,@DPTR          ; get a byte from SOURCE
000B A3        INC  DPTR             ; increment SOURCE address
000C 05A2      INC  AUXR1             ; switch data pointers
000E F0        MOVX @DPTR,A          ; write the byte to DEST
000F A3        INC  DPTR             ; increment DEST address
0010 70F6      JNZ  LOOP             ; check for 0 terminator
0012 05A2      INC  AUXR1             ; (optional) restore DPS

```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.

6.3. Expanded RAM (XRAM)

The TS80C51Rx2 provide additional Bytes of random access memory (RAM) space for increased data parameter handling and high level language usage.

RA2, RB2 and RC2 devices have 256 bytes of expanded RAM, from 00H to FFH in external data space; RD2 devices have 768 bytes of expanded RAM, from 00H to 2FFH in external data space.

The TS80C51Rx2 has internal data memory that is mapped into four separate segments.

The four segments are:

- 1. The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
- 2. The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
- 3. The Special Function Registers, SFRs, (addresses 80H to FFH) are directly addressable only.
- 4. The expanded RAM bytes are indirectly accessed by MOVX instructions, and with the EXTRAM bit cleared in the AUXR register. (See Table 5.)

The Lower 128 bytes can be accessed by either direct or indirect addressing. The Upper 128 bytes can be accessed by indirect addressing only. The Upper 128 bytes occupy the same address space as the SFR. That means they have the same address, but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 bytes of data RAM or to SFR space by the addressing mode used in the instruction.

- Instructions that use direct addressing access SFR space. **For example: MOV 0A0H, # data** ,accesses the SFR at location 0A0H (which is P2).
- Instructions that use indirect addressing access the Upper 128 bytes of data RAM. **For example: MOV @R0, # data** where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).
- The 256 or 768 XRAM bytes can be accessed by indirect addressing, with EXTRAM bit cleared and MOVX instructions. This part of memory which is physically located on-chip, logically occupies the first 256 or 768 bytes of external data memory.
- With EXTRAM = 0, the XRAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. **An access to XRAM will not affect ports P0, P2, P3.6 (\overline{WR}) and P3.7 (\overline{RD}).** **For example, with EXTRAM = 0, MOVX @R0, # data** where R0 contains 0A0H, accesses the XRAM at address 0A0H rather than external memory. An access to external data memory locations higher than FFH (i.e. 0100H to FFFFH) (higher than 2FFH (i.e. 0300H to FFFFH for RD devices) will be performed with the MOVX DPTR instructions in the same way as in the standard 80C51, so with P0 and P2 as data/address busses, and P3.6 and P3.7 as write and read timing signals. Refer to Figure . For RD devices, accesses to expanded RAM from 100H to 2FFH can only be done thanks to the use of DPTR.
- With EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 80C51. MOVX @ Ri will provide an eight-bit address multiplexed with data on Port0 and any output port pins can be used to output higher order address bits. This is to provide the external paging capability. MOVX @DPTR will generate a sixteen-bit address. Port2 outputs the high-order eight address bits (the contents of DPH) while Port0 multiplexes the low-order eight address bits (DPL) with data. MOVX @ Ri and MOVX @DPTR will generate either read or write signals on P3.6 (\overline{WR}) and P3.7 (\overline{RD}).

The stack pointer (SP) may be located anywhere in the 256 bytes RAM (lower and upper RAM) internal data memory. The stack may not be located in the XRAM.

6.5. Programmable Counter Array PCA

The PCA provides more timing capabilities with less CPU intervention than the standard timer/counters. Its advantages include reduced software overhead and improved accuracy. The PCA consists of a dedicated timer/counter which serves as the time base for an array of five compare/ capture modules. Its clock input can be programmed to count any one of the following signals:

- Oscillator frequency $\div 12$ ($\div 6$ in X2 mode)
- Oscillator frequency $\div 4$ ($\div 2$ in X2 mode)
- Timer 0 overflow
- External input on ECI (P1.2)

Each compare/capture modules can be programmed in any one of the following modes:

- rising and/or falling edge capture,
- software timer,
- high-speed output, or
- pulse width modulator.

Module 4 can also be programmed as a watchdog timer (See Section "PCA Watchdog Timer", page 33).

When the compare/capture modules are programmed in the capture mode, software timer, or high speed output mode, an interrupt can be generated when the module executes its function. All five modules plus the PCA timer overflow share one interrupt vector.

The PCA timer/counter and compare/capture modules share Port 1 for external I/O. These pins are listed below. If the port is not used for the PCA, it can still be used for standard I/O.

PCA component	External I/O Pin
16-bit Counter	P1.2 / ECI
16-bit Module 0	P1.3 / CEX0
16-bit Module 1	P1.4 / CEX1
16-bit Module 2	P1.5 / CEX2
16-bit Module 3	P1.6 / CEX3
16-bit Module 4	P1.7 / CEX4

The PCA timer is a common time base for all five modules (See Figure 7). The timer count source is determined from the CPS1 and CPS0 bits in the **CMOD SFR** (See Table 8) and can be programmed to run at:

- 1/12 the oscillator frequency. (Or 1/6 in X2 Mode)
- 1/4 the oscillator frequency. (Or 1/2 in X2 Mode)
- The Timer 0 overflow
- The input on the ECI pin (P1.2)

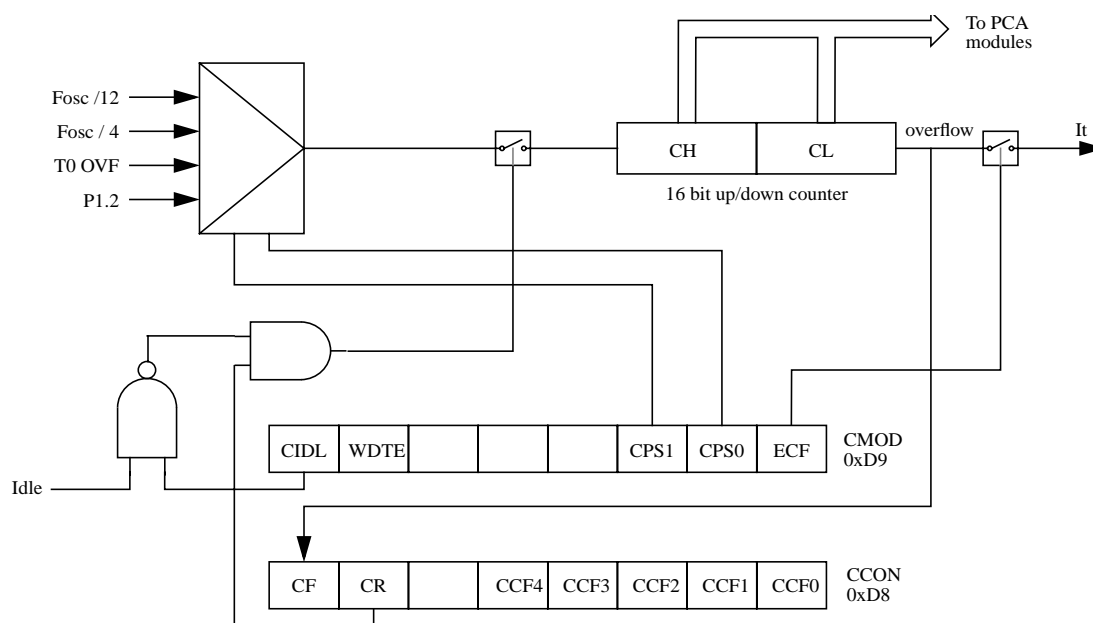


Figure 7. PCA Timer/Counter

Table 8. CMOD: PCA Counter Mode Register

CMOD Address 0D9H		CIDL	WDTE	-	-	-	CPS1	CPS0	ECF
Reset value		0	0	X	X	X	0	0	0

Symbol	Function		
CIDL	Counter Idle control: CIDL = 0 programs the PCA Counter to continue functioning during idle Mode. CIDL = 1 programs it to be gated off during idle.		
WDTE	Watchdog Timer Enable: WDTE = 0 disables Watchdog Timer function on PCA Module 4. WDTE = 1 enables it.		
-	Not implemented, reserved for future use. ^a		
CPS1	PCA Count Pulse Select bit 1.		
CPS0	PCA Count Pulse Select bit 0.		
	CPS1	CPS0	Selected PCA input. ^b
	0	0	Internal clock $f_{osc}/12$ (Or $f_{osc}/6$ in X2 Mode).
	0	1	Internal clock $f_{osc}/4$ (Or $f_{osc}/2$ in X2 Mode).
	1	0	Timer 0 Overflow
	1	1	External clock at ECI/P1.2 pin (max rate = $f_{osc}/8$)
ECF	PCA Enable Counter Overflow interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function of CF.		

- a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.
- b. f_{osc} = oscillator frequency

The CMOD SFR includes three additional bits associated with the PCA (See Figure 7 and Table 8).

- The CIDL bit which allows the PCA to stop during idle mode.
- The WDTE bit which enables or disables the watchdog function on module 4.

The **CCON SFR** contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (Refer to Table 9).

- Bit CR (CCON.6) must be set by software to run the PCA. The PCA is shut off by clearing this bit.
- Bit CF: The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software.
- Bits 0 through 4 are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software.

Table 9. CCON: PCA Counter Control Register

CCON Address 0D8H		CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0
Reset value		0	0	X	0	0	0	0	0
Symbol	Function								
CF	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.								
CR	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.								
-	Not implemented, reserved for future use. ^a								
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								

- a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

The **watchdog timer** function is implemented in module 4 (See Figure 10).

The **PCA interrupt** system is shown in Figure 8

6.5.3. High Speed Output Mode

In this mode the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set (See Figure 11).

A prior write must be done to CCAPnL and CCAPnH before writing the ECOMn bit.

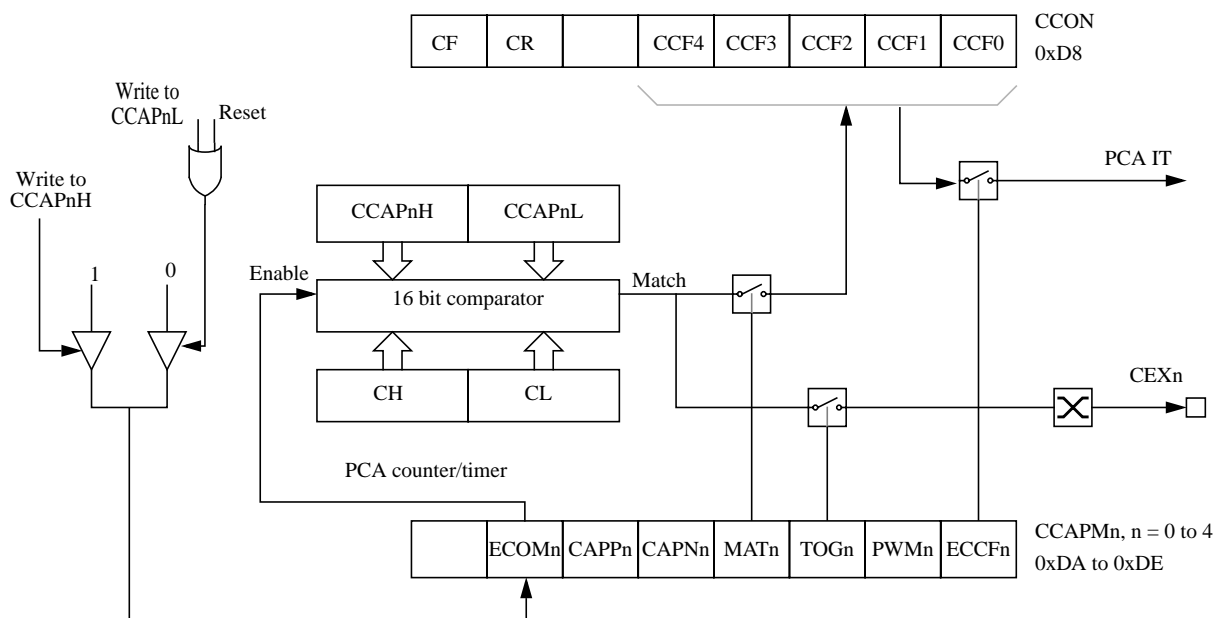


Figure 11. PCA High Speed Output Mode

Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.

6.6. TS80C51Rx2 Serial I/O Port

The serial I/O port in the TS80C51Rx2 is compatible with the serial I/O port in the 80C52.

It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

6.6.1. Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 13).

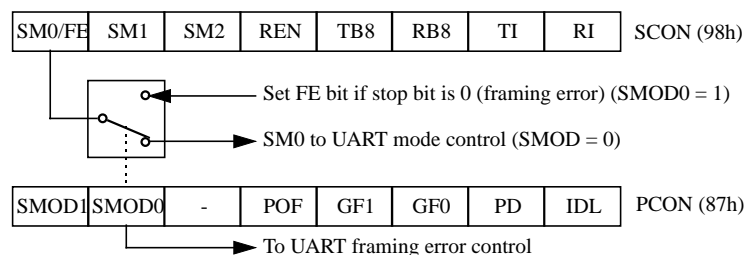


Figure 13. Framing Error Block Diagram

When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 16.) bit is set.

6.7. Interrupt System

The TS80C51Rx2 has a total of 7 interrupt vectors: two external interrupts ($\overline{\text{INT0}}$ and $\overline{\text{INT1}}$), three timer interrupts (timers 0, 1 and 2), the serial port interrupt and the PCA global interrupt. These interrupts are shown in Figure 16.

WARNING: Note that in the first version of RC devices, the PCA interrupt is in the lowest priority. Thus the order in $\overline{\text{INT0}}$, TF0, $\overline{\text{INT1}}$, TF1, RI or TI, TF2 or EXF2, PCA.

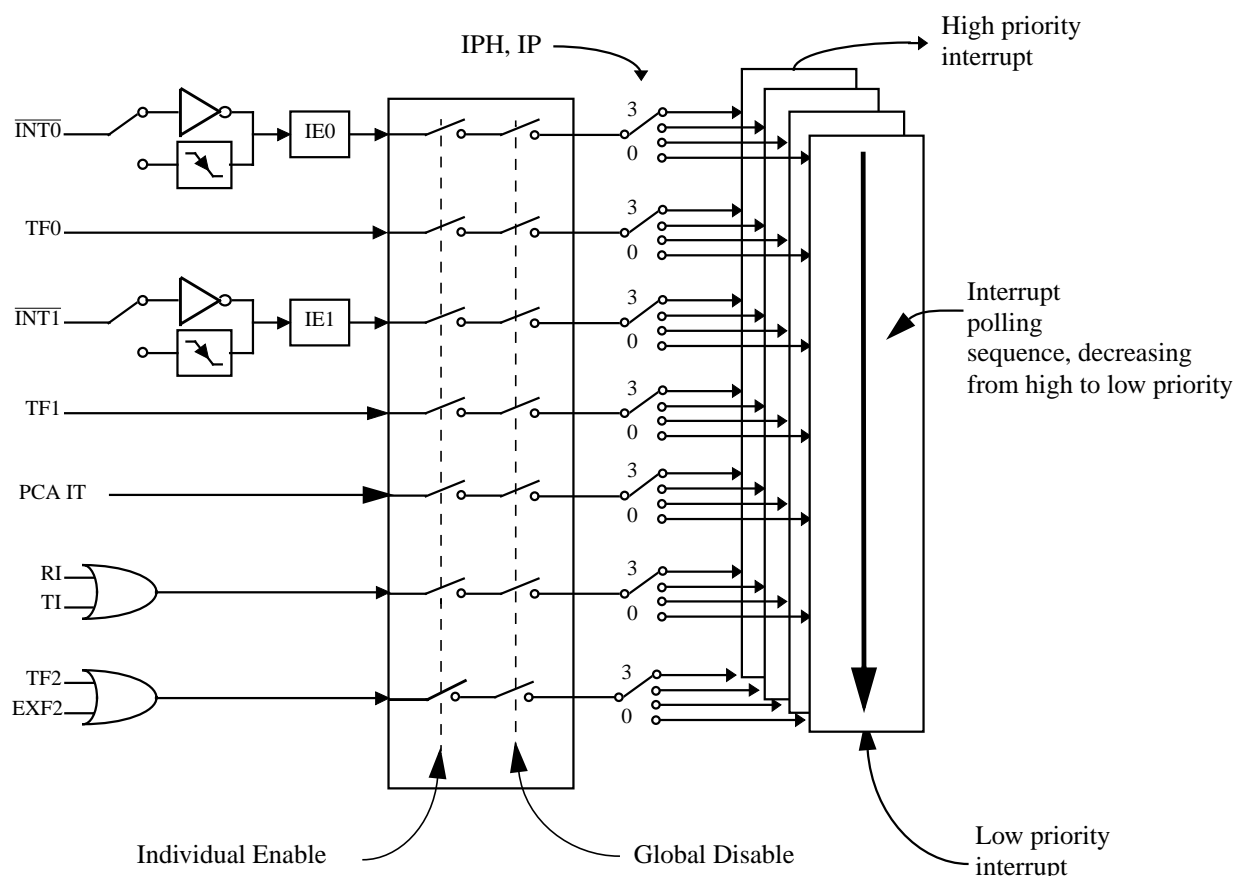


Figure 16. Interrupt Control System

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 19.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 20.) and in the Interrupt Priority High register (See Table 21.). shows the bit values and priority levels associated with each combination.

The PCA interrupt vector is located at address 0033H. All other vector addresses are the same as standard C52 devices.

6.10. Hardware Watchdog Timer

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer ReSeT (WDTRST) SFR. The WDT is by default disabled from exiting reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST-pin.

6.10.1. Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST-pin. The RESET pulse duration is $96 \times T_{OSC}$, where $T_{OSC} = 1/F_{OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

To have a more powerful WDT, a 2^7 counter has been added to extend the Time-out capability, ranking from 16ms to 2s @ $F_{OSC} = 12\text{MHz}$. To manage this feature, refer to WDTPRG register description, Table 24. (SFR0A7h).

Table 23. WDTRST Register

WDTRST Address (0A6h)

	7	6	5	4	3	2	1
Reset value	X	X	X	X	X	X	X

Write only, this SFR is used to reset/enable the WDT by writing 01EH then 0E1H in sequence.

Table 24. WDTPRG Register

WDTPRG Address (0A7h)

7	6	5	4	3	2	1	0
T4	T3	T2	T1	T0	S2	S1	S0

Bit Number	Bit Mnemonic	Description																																				
7	T4	Reserved Do not try to set or clear this bit.																																				
6	T3																																					
5	T2																																					
4	T1																																					
3	T0																																					
2	S2	WDT Time-out select bit 2																																				
1	S1	WDT Time-out select bit 1																																				
0	S0	WDT Time-out select bit 0																																				
		<table><tr><th>S2</th><th>S1</th><th>S0</th><th>Selected Time-out</th></tr><tr><td>0</td><td>0</td><td>0</td><td>(2¹⁴ - 1) machine cycles, 16.3 ms @ 12 MHz</td></tr><tr><td>0</td><td>0</td><td>1</td><td>(2¹⁵ - 1) machine cycles, 32.7 ms @ 12 MHz</td></tr><tr><td>0</td><td>1</td><td>0</td><td>(2¹⁶ - 1) machine cycles, 65.5 ms @ 12 MHz</td></tr><tr><td>0</td><td>1</td><td>1</td><td>(2¹⁷ - 1) machine cycles, 131 ms @ 12 MHz</td></tr><tr><td>1</td><td>0</td><td>0</td><td>(2¹⁸ - 1) machine cycles, 262 ms @ 12 MHz</td></tr><tr><td>1</td><td>0</td><td>1</td><td>(2¹⁹ - 1) machine cycles, 542 ms @ 12 MHz</td></tr><tr><td>1</td><td>1</td><td>0</td><td>(2²⁰ - 1) machine cycles, 1.05 s @ 12 MHz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>(2²¹ - 1) machine cycles, 2.09 s @ 12 MHz</td></tr></table>	S2	S1	S0	Selected Time-out	0	0	0	(2 ¹⁴ - 1) machine cycles, 16.3 ms @ 12 MHz	0	0	1	(2 ¹⁵ - 1) machine cycles, 32.7 ms @ 12 MHz	0	1	0	(2 ¹⁶ - 1) machine cycles, 65.5 ms @ 12 MHz	0	1	1	(2 ¹⁷ - 1) machine cycles, 131 ms @ 12 MHz	1	0	0	(2 ¹⁸ - 1) machine cycles, 262 ms @ 12 MHz	1	0	1	(2 ¹⁹ - 1) machine cycles, 542 ms @ 12 MHz	1	1	0	(2 ²⁰ - 1) machine cycles, 1.05 s @ 12 MHz	1	1	1	(2 ²¹ - 1) machine cycles, 2.09 s @ 12 MHz
S2	S1	S0	Selected Time-out																																			
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1	1	0	(2 ²⁰ - 1) machine cycles, 1.05 s @ 12 MHz																																			
1	1	1	(2 ²¹ - 1) machine cycles, 2.09 s @ 12 MHz																																			

Reset value XXXX X000

6.10.2. WDT during Power Down and Idle

In Power Down mode the oscillator stops, which means the WDT also stops. While in Power Down mode the user does not need to service the WDT. There are 2 methods of exiting Power Down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power Down mode. When Power Down is exited with hardware reset, servicing the WDT should occur as it normally should whenever the TS80C51Rx2 is reset. Exiting Power Down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service routine.

To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is best to reset the WDT just before entering powerdown.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting the TS80C51Rx2 while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

6.13. Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 27. AUXR Register

AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	EXTRAM	AO

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	EXTRAM	EXTRAM bit See Table 5.
0	AO	ALE Output bit Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = XXXX XX00b

Not bit addressable

9. Signature Bytes

The TS83/87C51RB2/RC2/RD2 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 31. for Read Signature Bytes. Table 31. shows the content of the signature byte for the TS87C51RB2/RC2/RD2.

Table 31. Signature Bytes Content

Location	Contents	Comment
30h	58h	Manufacturer Code: Atmel Wireless & Microcontrollers
31h	57h	Family Code: C51 X2
60h	7Ch	Product name: TS83C51RD2
60h	FCh	Product name: TS87C51RD2
60h	37h	Product name: TS83C51RC2
60h	B7h	Product name: TS87C51RC2
60h	3Bh	Product name: TS83C51RB2
60h	BBh	Product name: TS87C51RB2
61h	FFh	Product revision number

Table 38. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{LHLL}	Min	$2 T - x$	$T - x$	10	8	15	ns
T_{AVLL}	Min	$T - x$	$0.5 T - x$	15	13	20	ns
T_{LLAX}	Min	$T - x$	$0.5 T - x$	15	13	20	ns
T_{LLIV}	Max	$4 T - x$	$2 T - x$	30	22	35	ns
T_{LLPL}	Min	$T - x$	$0.5 T - x$	10	8	15	ns
T_{PLPH}	Min	$3 T - x$	$1.5 T - x$	20	15	25	ns
T_{PLIV}	Max	$3 T - x$	$1.5 T - x$	40	25	45	ns
T_{PXIX}	Min	x	x	0	0	0	ns
T_{PXIZ}	Max	$T - x$	$0.5 T - x$	7	5	15	ns
T_{AVIV}	Max	$5 T - x$	$2.5 T - x$	40	30	45	ns
T_{PLAZ}	Max	x	x	10	10	10	ns

10.5.3. External Program Memory Read Cycle

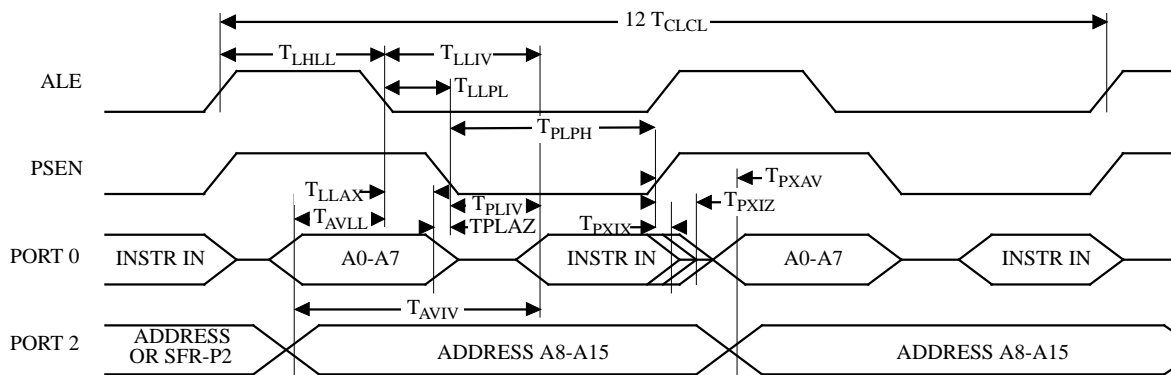


Figure 25. External Program Memory Read Cycle

10.5.4. External Data Memory Characteristics

Table 39. Symbol Description

Symbol	Parameter
T_{RLRH}	\overline{RD} Pulse Width
T_{WLWH}	\overline{WR} Pulse Width
T_{RLDV}	\overline{RD} to Valid Data In
T_{RHDX}	Data Hold After \overline{RD}
T_{RHDZ}	Data Float After \overline{RD}
T_{LLDV}	ALE to Valid Data In
T_{AVDV}	Address to Valid Data In
T_{LLWL}	ALE to \overline{WR} or \overline{RD}
T_{AVWL}	Address to \overline{WR} or \overline{RD}
T_{QVWX}	Data Valid to \overline{WR} Transition
T_{QVWH}	Data set-up to \overline{WR} High
T_{WHQX}	Data Hold After \overline{WR}
T_{RLAZ}	\overline{RD} Low to Address Float
T_{WHLH}	\overline{RD} or \overline{WR} High to ALE high

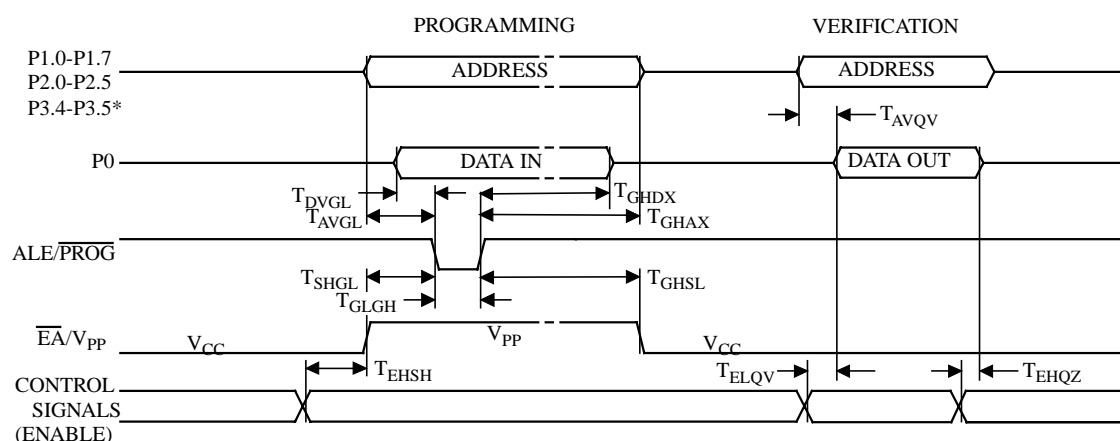
10.5.9. EPROM Programming and Verification Characteristics

$T_A = 21^\circ\text{C}$ to 27°C ; $V_{SS} = 0\text{V}$; $V_{CC} = 5\text{V} \pm 10\%$ while programming. V_{CC} = operating range while verifying

Table 45. EPROM Programming Parameters

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13	V
I_{PP}	Programming Supply Current		75	mA
$1/T_{CLCL}$	Oscillator Frequency	4	6	MHz
T_{AVGL}	Address Setup to $\overline{\text{PROG}}$ Low	$48 T_{CLCL}$		
T_{GHAX}	Adress Hold after $\overline{\text{PROG}}$	$48 T_{CLCL}$		
T_{DVGL}	Data Setup to $\overline{\text{PROG}}$ Low	$48 T_{CLCL}$		
T_{GHDX}	Data Hold after $\overline{\text{PROG}}$	$48 T_{CLCL}$		
T_{EHS}	(Enable) High to V_{PP}	$48 T_{CLCL}$		
T_{SHGL}	V_{PP} Setup to $\overline{\text{PROG}}$ Low	10		μs
T_{GHSL}	V_{PP} Hold after $\overline{\text{PROG}}$	10		μs
T_{GLGH}	$\overline{\text{PROG}}$ Width	90	110	μs
T_{AVQV}	Address to Valid Data		$48 T_{CLCL}$	
T_{ELQV}	ENABLE Low to Data Valid		$48 T_{CLCL}$	
T_{EHQZ}	Data Float after ENABLE	0	$48 T_{CLCL}$	

10.5.10. EPROM Programming and Verification Waveforms



* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

Figure 29. EPROM Programming and Verification Waveforms

11. Ordering Information

TS	87C51RD2	-M	C	B	R
Part Number 80C51RA2 (ROMless, 256 bytes XRAM) 80C51RD2 (ROMless, 768bytes XRAM) 83C51RB2zzz (16k ROM, zzz is the customer code) 83C51RC2zzz (32k ROM, zzz is the customer code) 83C51RD2zzz (64k ROM, zzz is the customer code) 87C51RB2 (16k OTP EPROM) 87C51RC2 (32k OTP EPROM) 87C51RD2 (64k OTP EPROM)					
	-M:	VCC: 5V +/- 10% 40 MHz, X1 mode 20 MHz, X2 mode	Packages: A: PDIL 40 B: PLCC 44 E: VQFP 44 (1.4mm) J: Window CDIL 40* K: Window CQPJ 44* L: PLCC68 (RD devices only)* M: VQFP64, square package, 1.4mm (RD devices only)* N: JLCC68 (RD devices only)*		
	-V:	VCC: 5V +/- 10% 40 MHz, X1 mode 30 MHz, X2 mode			
	-L:	VCC: 2.7 to 5.5 V 30 MHz, X1 mode 20 MHz, X2 mode			
	-E:	Samples			
			Temperature Range C: Commercial 0 to 70°C I: Industrial -40 to 85°C		
					Conditioning R: Tape & Reel D: Dry Pack B: Tape & Reel and Dry Pack

(*) Check with Atmel Wireless & Microcontrollers Sales Office for availability. Ceramic packages (J, K, N) are available for prototyping, not for volume production. Ceramic packages are available for OTP only.

Table 47. Maximum Clock Frequency

Code	-M	-V	-L	Unit
Standard Mode, oscillator frequency	40	40	30	MHz
Standard Mode, internal frequency	40	40	30	
X2 Mode, oscillator frequency	20	30	20	MHz
X2 Mode, internal equivalent frequency	40	60	40	

Table 48. Possible Ordering Entries

	TS80C51RA2/RD2 ROMless	TS83C51RB2/RC2/RD2 ^{zzz} ROM	TS87C51RB2/RC2/RD2 OTP
-MCA	X	X	X
-MCB	X	X	X
-MCE	X	X	X
-MCL	RD2 only	RD2 only	RD2 only
-MCM	RD2 only	RD2 only	RD2 only
-VCA	X	X	X
-VCB	X	X	X
-VCE	X	X	X
-VCL	RD2 only	RD2 only	RD2 only
-VCM	RD2 only	RD2 only	RD2 only
-LCA	X	X	X
-LCB	X	X	X
-LCE	X	X	X
-LCL	RD2 only	RD2 only	RD2 only
-LCM	RD2 only	RD2 only	RD2 only
-MIA	X	X	X
-MIB	X	X	X
-MIE	X	X	X
-MIL	RD2 only	RD2 only	RD2 only
-MIM	RD2 only	RD2 only	RD2 only
-VIA	X	X	X
-VIB	X	X	X
-VIE	X	X	X
-VIL	RD2 only	RD2 only	RD2 only
-VIM	RD2 only	RD2 only	RD2 only
-LIA	X	X	X
-LIB	X	X	X
-LIE	X	X	X
-LIL	RD2 only	RD2 only	RD2 only
-LIM	RD2 only	RD2 only	RD2 only
-EA	X		X
-EB	X		X
-EE	X		X
-EL	RD2 only		RD2 only
-EM	RD2 only		RD2 only
-EJ			RC2 and RD2 only
-EK			RC2 and RD2 only
-EN			RD2 only

- -Ex for samples
- Tape and Reel available for B, E, L and M packages
- Dry pack mandatory for E and M packages