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Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c51rb2-mcb

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Mnemonic	Pin Number			Туре	Name And Function
ALE/PROG	30	33	27	O (I)	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
PSEN	29	32	26	0	Program Store ENable: The read strobe to external program memory. When executing code from the external program memory, \overrightarrow{PSEN} is activated twice each machine cycle, except that two \overrightarrow{PSEN} activations are skipped during each access to external data memory. \overrightarrow{PSEN} is not activated during fetches from internal program memory.
EA/V _{pp}	31	35	29	I	External Access Enable/Programming Supply Voltage: $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH (RB) or 7FFFH (RC), or FFFFH (RD). If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (RB) or 7FFFH (RC) $\overline{\text{EA}}$ must be held low for ROMless devices. This pin also receives the 12.75V programming supply voltage (V _{PP}) during EPROM programming. If security level 1 is programmed, $\overline{\text{EA}}$ will be internally latched on Reset.
XTAL1	19	21	15	Ι	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	0	Crystal 2: Output from the inverting oscillator amplifier



5.1. Pin Description for 64/68 pin Packages

Port 4 and Port 5 are 8-bit bidirectional I/O ports with internal pull-ups. Pins that have 1 written to them are pulled high by the internal pull ups and can be used as inputs.

As inputs, pins that are externally pulled low will source current because of the internal pull-ups.

Refer to the previous pin description for other pins.

	PLCC68	SQUARE VQFP64 1.4
VSS	51	9/40
VCC	17	8
P0.0	15	6
P0.1	14	5
P0.2	12	3
P0.3	11	2
P0.4	9	64
P0.5	6	61
P0.6	5	60
P0.7	3	59
P1.0	19	10
P1.1	21	12
P1.2	22	13
P1.3	23	14
P1.4	25	16
P1.5	27	18
P1.6	28	19
P1.7	29	20
P2.0	54	43
P2.1	55	44
P2.2	56	45
P2.3	58	47
P2.4	59	48
P2.5	61	50
P2.6	64	53
P2.7	65	54
P3.0	34	25
P3.1	39	28

Table	2.	64/68	Pin	Packages	Configuration
I GOIC		0.00		I uchages	Comparation



	PLCC68	SQUARE VQFP64 1.4
P3.2	40	29
P3.3	41	30
P3.4	42	31
P3.5	43	32
P3.6	45	34
P3.7	47	36
RESET	30	21
ALE/PROG	68	56
PSEN	67	55
EA/VPP	2	58
XTAL1	49	38
XTAL2	48	37
P4.0	20	11
P4.1	24	15
P4.2	26	17
P4.3	44	33
P4.4	46	35
P4.5	50	39
P4.6	53	42
P4.7	57	46
P5.0	60	49
P5.1	62	51
P5.2	63	52
P5.3	7	62
P5.4	8	63
P5.5	10	1
P5.6	13	4
P5.7	16	7



ASSEMBLY LANGUAGE

; Block move using dual data pointers ; Destroys DPTR0, DPTR1, A and PSW ; note: DPS exits opposite of entry state ; unless an extra INC AUXR1 is added

00A2	AUXR1 EQU 0A2H	
; 0000 909000 0003 05A2 0005 004000	MOV DPTR,#SOURCE INC AUXR1 MOV DPTR #DEST	; address of SOURCE ; switch data pointers : address of DEST
0003 90A000 0008 0008 05A2	LOOP: INC AUXR1	; switch data pointers
000A E0	MOVX A, @DPTR	; get a byte from SOURCE
000B A3	INC DPTR	; increment SOURCE address
000C 05A2	INC AUXRI	; switch data pointers
000E F0	MOVX @DPTR,A	; write the byte to DEST
000F A3	INC DPTR	: increment DEST address
0010 70F6	JNZ LOOP	; check for 0 terminator
0012 05A2	INC AUXR1	; (optional) restore DPS

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.



6.3. Expanded RAM (XRAM)

The TS80C51Rx2 provide additional Bytes of ramdom access memory (RAM) space for increased data parameter handling and high level language usage.

RA2, RB2 and RC2 devices have 256 bytes of expanded RAM, from 00H to FFH in external data space; RD2 devices have 768 bytes of expanded RAM, from 00H to 2FFH in external data space.

The TS80C51Rx2 has internal data memory that is mapped into four separate segments.

The four segments are:

- 1. The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
- 2. The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
- 3. The Special Function Registers, SFRs, (addresses 80H to FFH) are directly addressable only.
- 4. The expanded RAM bytes are indirectly accessed by MOVX instructions, and with the EXTRAM bit cleared in the AUXR register. (See Table 5.)

The Lower 128 bytes can be accessed by either direct or indirect addressing. The Upper 128 bytes can be accessed by indirect addressing only. The Upper 128 bytes occupy the same address space as the SFR. That means they have the same address, but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 bytes of data RAM or to SFR space by the addressing mode used in the instruction.

- Instructions that use direct addressing access SFR space. For example: MOV 0A0H, # data ,accesses the SFR at location 0A0H (which is P2).
- Instructions that use indirect addressing access the Upper 128 bytes of data RAM. For example: MOV @R0, # data where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).
- The 256 or 768 XRAM bytes can be accessed by indirect addressing, with EXTRAM bit cleared and MOVX instructions. This part of memory which is physically located on-chip, logically occupies the first 256 or 768 bytes of external data memory.
- With <u>EXTRAM = 0</u>, the XRAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. An access to XRAM will not affect ports P0, P2, P3.6 (\overline{WR}) and P3.7 (\overline{RD}). For example, with EXTRAM = 0, MOVX @R0, # data where R0 contains 0A0H, accesses the XRAM at address 0A0H rather than external memory. An access to external data memory locations higher than FFH (i.e. 0100H to FFFFH) (higher than 2FFH (i.e. 0300H to FFFFH for RD devices) will be performed with the MOVX DPTR instructions in the same way as in the standard 80C51, so with P0 and P2 as data/address busses, and P3.6 and P3.7 as write and read timing signals. Refer to Figure . For RD devices, accesses to expanded RAM from 100H to 2FFH can only be done thanks to the use of DPTR.
- With <u>EXTRAM = 1</u>, MOVX @Ri and MOVX @DPTR will be similar to the standard 80C51. MOVX @ Ri will provide an eight-bit address multiplexed with data on Port0 and any output port pins can be used to output higher order address bits. This is to provide the external paging capability. MOVX @DPTR will generate a sixteen-bit address. Port2 outputs the high-order eight address bits (the contents of DPH) while Port0 multiplexes the low-order eight address bits (DPL) with data. MOVX @ Ri and MOVX @DPTR will generate either read or write signals on P3.6 (WR) and P3.7 (RD).

The stack pointer (SP) may be located anywhere in the 256 bytes RAM (lower and upper RAM) internal data memory. The stack may not be located in the XRAM.





Figure 4. Internal and External Data Memory Address

AUXR Iress 08EH		-	-	-	-	-	-	EXTRA M	AO
Reset	value	X	Х	Х	Х	Х	Х	0	0
Symbol					Functior	1			
-	Not imp	Not implemented, reserved for future use. ^a							
AO	Disable/Enable ALE								
	AO	AO Operating Mode							
	0	ALI X2	E is emitte mode is u	ed at a cor sed)	istant rate	of 1/6 the	oscillator	frequency (or	r 1/3 if
	1	AL	E is active	only duri	ng a MOV	X or MO	VC instruc	tion	
EXTRAM	Internal/I	External R	AM (00H-	FFH) acce	ess using N	AOVX @	Ri/ @ DP	TR	
	EXTRAM Operating Mode								
	0	Inte	rnal XRA	M access	using MOV	/X @ Ri/	@ DPTR		
	1	Ext	ernal data	memory a	ccess				

 Table 5. Auxiliary Register AUXR

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.



It is possible to use timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.



Figure 6. Clock-Out Mode $C/\overline{T2} = 0$



Table 7. T2MOD Register

T2MOD - Timer 2 Mode Control Register (C9h)

			,				
7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	DCEN

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	T2OE	Timer 2 Output Enable bit Clear to program P1.0/T2 as clock input or I/O port. Set to program P1.0/T2 as clock output.
0	DCEN	Down Counter Enable bit Clear to disable timer 2 as up/down counter. Set to enable timer 2 as up/down counter.

Reset Value = XXXX XX00b Not bit addressable



The CCON SFR contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (Refer to Table 9).

- Bit CR (CCON.6) must be set by software to run the PCA. The PCA is shut off by clearing this bit.
- Bit CF: The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software.
- Bits 0 through 4 are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software.

CCON Address 0D8H		CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0	
	Rese	et value	0	0	X	0	0	0	0	0
Syı	nbol	Function	l							
CF		PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software can only be cleared by software.								gs tware but
CR		PCA Count by software	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.							
-		Not implen	nented, res	erved for	future use	a				
CCF4		PCA Modu cleared by	ile 4 inter software.	rupt flag.	Set by ha	rdware wh	en a matc	h or captı	ire occurs.	Must be
CCF3		PCA Modu cleared by	ile 3 inter software.	rupt flag.	Set by ha	rdware wh	en a matc	h or captı	ire occurs.	Must be
CCF2		PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must cleared by software.						Must be		
CCF1		PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs cleared by software.						ire occurs.	Must be	
CCF0		PCA Modu cleared by	ile 0 inter software.	rupt flag.	Set by ha	rdware wh	en a matc	h or captu	ire occurs.	Must be

 Table 9. CCON: PCA Counter Control Register

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

The watchdog timer function is implemented in module 4 (See Figure 10).

The PCA interrupt system is shown in Figure 8





Figure 8. PCA Interrupt System

PCA Modules: each one of the five compare/capture modules has six possible functions. It can perform:

- 16-bit Capture, positive-edge triggered,
- 16-bit Capture, negative-edge triggered,
- 16-bit Capture, both positive and negative-edge triggered,
- 16-bit Software Timer,
- 16-bit High Speed Output,
- 8-bit Pulse Width Modulator.

In addition, module 4 can be used as a Watchdog Timer.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. (See Table 10). The registers contain the bits that control the mode that each module will operate in.

- The ECCF bit (CCAPMn.0 where n=0, 1, 2, 3, or 4 depending on the module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module.
- PWM (CCAPMn.1) enables the pulse width modulation mode.
- The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register.
- The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.
- The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition.
- The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function.

Table 11 shows the CCAPMn settings for the various PCA functions.

CCA



Table 10.	CCAPMn:	PCA	Modules	Compare/Capt	ure Control	Registers
-----------	----------------	-----	---------	--------------	-------------	-----------

PMn Address n = 0 - 4 CC CC CC CC		CCAP CCAP CCAP CCAP CCAP	M0=0DAH M1=0DBH M2=0DCH M3=0DDH M4=0DEH								
				-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMm	ECCFn
		Res	et value	Х	0	0	0	0	0	0	0
	Syı	nbol	Function	l							
	-		Not implen	ot implemented, reserved for future use. ^a							
	ECOM	In	Enable Cor	Enable Comparator. ECOMn = 1 enables the comparator function.							
	CAPP	n	Capture Po	Capture Positive, CAPPn = 1 enables positive edge capture.							
	CAPN	n	Capture Ne	ture Negative, CAPNn = 1 enables negative edge capture.							
	MATn	1	Match. Wh register cau	Match. When $MATn = 1$, a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.						re/capture	
	TOGn		Toggle. Wi register cau	ggle. When TOGn = 1, a match of the PCA counter with this module's compare/capture gister causes the CEXn pin to toggle.							
	PWM	1	Pulse Widt modulated	Pulse Width Modulation Mode. PWMn = 1 enables the CEXn pin to be used as a pulse width modulated output.							
	ECCF	n	Enable CC	Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.							

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMm	ECCFn	Module Function
0	0	0	0	0	0	0	No Operation
X	1	0	0	0	0	Х	16-bit capture by a positive-edge trigger on CEXn
X	0	1	0	0	0	Х	16-bit capture by a negative trigger on CEXn
X	1	1	0	0	0	Х	16-bit capture by a transition on CEXn
1	0	0	1	0	0	Х	16-bit Software Timer / Compare mode.
1	0	0	1	1	0	Х	16-bit High Speed Output
1	0	0	0	0	1	0	8-bit PWM
1	0	0	1	Х	0	Х	Watchdog Timer (module 4 only)

Table 11. PCA Module Modes (CCAPMn Registers)

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output (See Table 12 & Table 13)



6.12. Power-Off Flag

The power-off flag allows the user to distinguish between a "cold start" reset and a "warm start" reset.

A cold start reset is the one induced by V_{CC} switch-on. A warm start reset occurs while V_{CC} is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 26.). POF is set by hardware when V_{CC} rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a Vcc range from 4.5V to 5.5V. For lower Vcc value, reading POF bit will return indeterminate value.

Table 26. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3 2 1 0							
SMOD1	SMOD	-	- POF GF1 GF0 PD								
Bit Number	Bit Mnemonic		Description								
7	SMOD1	Serial port Mode bit Set to select dou	erial port Mode bit 1 Set to select double baud rate in mode 1, 2 or 3.								
6	SMOD0	Serial port Mode bit Clear to select SI Set to to select F	0 M0 bit in SCON re E bit in SCON reg	egister. ister.							
5	-	Reserved The value read fr	Reserved The value read from this bit is indeterminate. Do not set this bit.								
4	POF	Power-Off Flag Clear to recogniz Set by hardware	e next reset type. when V _{CC} rises fr	om 0 to its nomina	l voltage. Can also	be set by software	·.				
3	GF1	General purpose Fla Cleared by user f Set by user for g	g or general purpose eneral purpose usa	e usage. ge.							
2	GF0	General purpose Fla Cleared by user f Set by user for g	eneral purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.								
1	PD	Power-Down mode I Cleared by hardw Set to enter powe	Power-Down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.								
0	IDL	Idle mode bit Clear by hardwar Set to enter idle r	e when interrupt on ode.	or reset occurs.							

Reset Value = 00X1 0000b Not bit addressable



8. TS87C51RB2/RC2/RD2 EPROM

8.1. EPROM Structure

The TS87C51RB2/RC2/RD2 EPROM is divided in two different arrays:

•	the code array:
•	the encryption array:
In	addition a third non programmable array is implemented:
•	the signature array:

8.2. EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

8.2.1. Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

8.2.2. Program Lock Bits

The three lock bits, when programmed according to Table 29.8.2.3., will provide different level of protection for the on-chip code and data.

F	Program Lo	ock Bits		Protection description
Security level	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	Р	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, \overline{EA} is sampled and latched on reset, and further programming of the EPROM is disabled.
3	U	Р	U	Same as 2, also verify is disabled.
4	U	U	Р	Same as 3, also external execution is disabled.

Table 29	. Program	Lock	bits
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U: unprogrammed,

P: programmed

WARNING: Security level 2 and 3 should only be programmed after EPROM and Core verification.

8.2.3. Signature bytes

The TS87C51RB2/RC2/RD2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 8.3.



Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
I _{CC} idle	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			0.15 Freq (MHz) + 0.2 @12MHz 2 @16MHz 2.6	mA	$V_{CC} = 3.3 V^{(2)}$

NOTES

1. I_{CC} under reset is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5$ ns (see Figure 24.), $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$ V; XTAL2 N.C.; $\overline{EA} = RST = Port \ 0 = V_{CC}$. I_{CC} would be slightly higher if a crystal oscillator used.

2. Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5$ ns, $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$ V; XTAL2 N.C; Port $0 = V_{CC}$; $\overline{EA} = RST = V_{SS}$ (see Figure 22.).

3. Power Down I_{CC} is measured with all output pins disconnected; $\overline{EA} = V_{SS}$, PORT $0 = V_{CC}$; XTAL2 NC.; RST = V_{SS} (see Figure 23.).

4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the $V_{OL}s$ of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi V_{OL} peak 0.6V. A Schmitt Trigger use is not necessary.

5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.

6. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin: 10 mA Maximum I_{OL} per 8-bit port:

Port 0: 26 mA

Ports 1, 2, 3 and 4 and 5 when available: 15 mA

Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions. 7. For other values, please contact your sales office.

8. Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5$ ns (see Figure 24.), $V_{IL} = V_{SS} + 0.5$ V,

 $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C.; $\overline{EA} = Port 0 = V_{CC}$; RST = V_{SS} . The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.



All other pins are disconnected.

Figure 20. I_{CC} Test Condition, under reset



Symbol	Туре	Standard Clock	X2 Clock	-M	-V	-L	Units
T _{LHLL}	Min	2 T - x	T - x	10	8	15	ns
T _{AVLL}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLAX}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLIV}	Max	4 T - x	2 T - x	30	22	35	ns
T _{LLPL}	Min	T - x	0.5 T - x	10	8	15	ns
T _{PLPH}	Min	3 T - x	1.5 T - x	20	15	25	ns
T _{PLIV}	Max	3 T - x	1.5 T - x	40	25	45	ns
T _{PXIX}	Min	x	x	0	0	0	ns
T _{PXIZ}	Max	T - x	0.5 T - x	7	5	15	ns
T _{AVIV}	Max	5 T - x	2.5 T - x	40	30	45	ns
T _{PLAZ}	Max	x	x	10	10	10	ns

 Table 38. AC Parameters for a Variable Clock: derating formula

10.5.3. External Program Memory Read Cycle



Figure 25. External Program Memory Read Cycle



Symbol	Туре	Standard Clock	X2 Clock	-M	-V	-L	Units
T _{RLRH}	Min	6 T - x	3 T - x	20	15	25	ns
T _{WLWH}	Min	6 T - x	3 T - x	20	15	25	ns
T _{RLDV}	Max	5 T - x	2.5 T - x	25	23	30	ns
T _{RHDX}	Min	x	х	0	0	0	ns
T _{RHDZ}	Max	2 T - x	T - x	20	15	25	ns
T _{LLDV}	Max	8 T - x	4T -x	40	35	45	ns
T _{AVDV}	Max	9 T - x	4.5 T - x	60	50	65	ns
T _{LLWL}	Min	3 T - x	1.5 T - x	25	20	30	ns
T _{LLWL}	Max	3 T + x	1.5 T + x	25	20	30	ns
T _{AVWL}	Min	4 T - x	2 T - x	25	20	30	ns
T _{QVWX}	Min	T - x	0.5 T - x	15	10	20	ns
T _{QVWH}	Min	7 T - x	3.5 T - x	15	10	20	ns
T _{WHQX}	Min	T - x	0.5 T - x	10	8	15	ns
T _{RLAZ}	Max	x	х	0	0	0	ns
T _{WHLH}	Min	T - x	0.5 T - x	15	10	20	ns
T _{WHLH}	Max	T + x	0.5 T + x	15	10	20	ns

Table 41. AC Parameters	for	a	Variable	Clock:	derating	formula
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10.5.5. External Data Memory Write Cycle



Figure 26. External Data Memory Write Cycle



10.5.6. External Data Memory Read Cycle



Figure 27. External Data Memory Read Cycle

10.5.7. Serial Port Timing - Shift Register Mode

Table 42. Symbol Description

Symbol	Parameter
T _{XLXL}	Serial port clock cycle time
T _{QVHX}	Output data set-up to clock rising edge
T _{XHQX}	Output data hold after clock rising edge
T _{XHDX}	Input data hold after clock rising edge
T _{XHDV}	Clock rising edge to input data valid

Table 43. AC Parameters for a Fix Clock

Speed	-M 40 MHz		-M -V -V 40 MHz X2 mode standard mode 30 MHz 40 MHz 60 MHz equiv.		V •d mode ⁄IHz	-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T _{XLXL}	300		200		300		300		400		ns
T _{QVHX}	200		117		200		200		283		ns
T _{XHQX}	30		13		30		30		47		ns
T _{XHDX}	0		0		0		0		0		ns
T _{XHDV}		117		34		117		117		200	ns



Symbol	Туре	Standard Clock	X2 Clock	-М	-V	-L	Units
T _{XLXL}	Min	12 T	6 T				ns
T _{QVHX}	Min	10 T - x	5 T - x	50	50	50	ns
T _{XHQX}	Min	2 T - x	T - x	20	20	20	ns
T _{XHDX}	Min	X	Х	0	0	0	ns
T _{XHDV}	Max	10 T - x	5 T- x	133	133	133	ns

Table 44. AC Parameters	for	a	Variable	Clock:	derating	formula
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10.5.8. Shift Register Timing Waveforms



Figure 28. Shift Register Timing Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \ge \pm 20$ mA.

10.5.15. Clock Waveforms

Valid in normal clock mode. In X2 mode XTAL2 signal must be changed to XTAL2 divided by two.



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though ($T_A=25^{\circ}C$ fully loaded) RD and WR propagation delays are approximately 50ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.



	TS80C51RA2/RD2 ROMless	TS83C51RB2/RC2/RD2zzz ROM	TS87C51RB2/RC2/RD2 OTP	
-MCA	Х	Х	X	
-MCB	Х	Х	X	
-MCE	Х	Х	X	
-MCL	RD2 only	RD2 only	RD2 only	
-MCM	RD2 only	RD2 only	RD2 only	
-VCA	Х	Х	X	
-VCB	Х	Х	X	
-VCE	Х	Х	X	
-VCL	RD2 only	RD2 only	RD2 only	
-VCM	RD2 only	RD2 only	RD2 only	
-LCA	Х	Х	X	
-LCB	Х	Х	X	
-LCE	Х	Х	X	
-LCL	RD2 only	RD2 only	RD2 only	
-LCM	RD2 only	RD2 only	RD2 only	
-MIA	Х	Х	X	
-MIB	X	Х	X	
-MIE	Х	Х	X	
-MIL	RD2 only	RD2 only	RD2 only	
-MIM	RD2 only	RD2 only	RD2 only	
-VIA	Х	Х	X	
-VIB	Х	Х	X	
-VIE	Х	Х	X	
-VIL	RD2 only	RD2 only	RD2 only	
-VIM	RD2 only	RD2 only	RD2 only	
-LIA	Х	Х	X	
-LIB	Х	Х	X	
-LIE	Х	X	X	
-LIL	RD2 only	RD2 only	RD2 only	
-LIM	RD2 only	RD2 only	RD2 only	
-EA	Х		X	
-EB	Х		X	
-EE	Х		X	
-EL	RD2 only		RD2 only	
-EM	RD2 only		RD2 only	
-EJ			RC2 and RD2 only	
-EK			RC2 and RD2 only	
-EN			RD2 only	

Table 48. Possible Ordering Entries

• -Ex for samples

- Tape and Reel available for B, E, L and M packages
- Dry pack mandatory for E and M packages