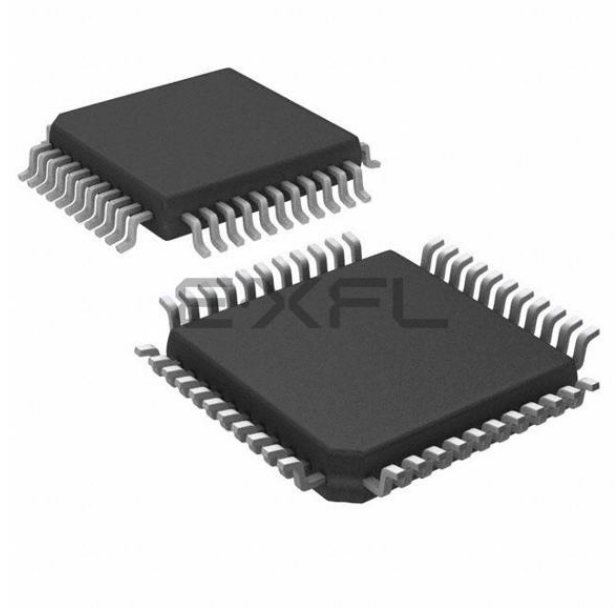

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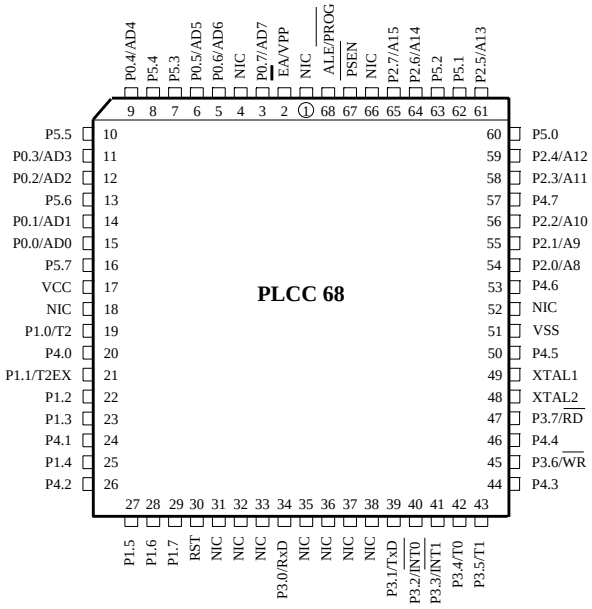
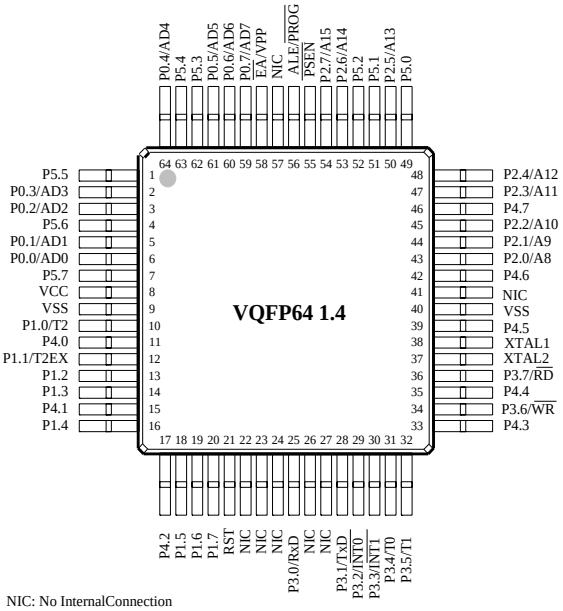
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/30MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-VQFP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c51rb2-vce





NIC: No InternalConnection

	PLCC68	SQUARE VQFP64 1.4
P3.2	40	29
P3.3	41	30
P3.4	42	31
P3.5	43	32
P3.6	45	34
P3.7	47	36
RESET	30	21
ALE/$\overline{PROG}$	68	56
$\overline{PSEN}$	67	55
$\overline{EA}$/VPP	2	58
XTAL1	49	38
XTAL2	48	37
P4.0	20	11
P4.1	24	15
P4.2	26	17
P4.3	44	33
P4.4	46	35
P4.5	50	39
P4.6	53	42
P4.7	57	46
P5.0	60	49
P5.1	62	51
P5.2	63	52
P5.3	7	62
P5.4	8	63
P5.5	10	1
P5.6	13	4
P5.7	16	7

6.3. Expanded RAM (XRAM)

The TS80C51Rx2 provide additional Bytes of ramdom access memory (RAM) space for increased data parameter handling and high level language usage.

RA2, RB2 and RC2 devices have 256 bytes of expanded RAM, from 00H to FFH in external data space; RD2 devices have 768 bytes of expanded RAM, from 00H to 2FFH in external data space.

The TS80C51Rx2 has internal data memory that is mapped into four separate segments.

The four segments are:

- 1. The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
- 2. The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
- 3. The Special Function Registers, SFRs, (addresses 80H to FFH) are directly addressable only.
- 4. The expanded RAM bytes are indirectly accessed by MOVX instructions, and with the EXTRAM bit cleared in the AUXR register. (See Table 5.)

The Lower 128 bytes can be accessed by either direct or indirect addressing. The Upper 128 bytes can be accessed by indirect addressing only. The Upper 128 bytes occupy the same address space as the SFR. That means they have the same address, but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 bytes of data RAM or to SFR space by the addressing mode used in the instruction.

- Instructions that use direct addressing access SFR space. **For example: MOV 0A0H, # data** ,accesses the SFR at location 0A0H (which is P2).
- Instructions that use indirect addressing access the Upper 128 bytes of data RAM. **For example: MOV @R0, # data** where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).
- The 256 or 768 XRAM bytes can be accessed by indirect addressing, with EXTRAM bit cleared and MOVX instructions. This part of memory which is physically located on-chip, logically occupies the first 256 or 768 bytes of external data memory.
- With EXTRAM = 0, the XRAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. **An access to XRAM will not affect ports P0, P2, P3.6 ($\overline{WR}$) and P3.7 ($\overline{RD}$)**. **For example, with EXTRAM = 0, MOVX @R0, # data** where R0 contains 0A0H, accesses the XRAM at address 0A0H rather than external memory. An access to external data memory locations higher than FFH (i.e. 0100H to FFFFH) (higher than 2FFH (i.e. 0300H to FFFFH for RD devices) will be performed with the MOVX DPTR instructions in the same way as in the standard 80C51, so with P0 and P2 as data/address busses, and P3.6 and P3.7 as write and read timing signals. Refer to Figure . For RD devices, accesses to expanded RAM from 100H to 2FFH can only be done thanks to the use of DPTR.
- With EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 80C51. MOVX @ Ri will provide an eight-bit address multiplexed with data on Port0 and any output port pins can be used to output higher order address bits. This is to provide the external paging capability. MOVX @DPTR will generate a sixteen-bit address. Port2 outputs the high-order eight address bits (the contents of DPH) while Port0 multiplexes the low-order eight address bits (DPL) with data. MOVX @ Ri and MOVX @DPTR will generate either read or write signals on P3.6 ($\overline{WR}$) and P3.7 ($\overline{RD}$).

The stack pointer (SP) may be located anywhere in the 256 bytes RAM (lower and upper RAM) internal data memory. The stack may not be located in the XRAM.

6.5. Programmable Counter Array PCA

The PCA provides more timing capabilities with less CPU intervention than the standard timer/counters. Its advantages include reduced software overhead and improved accuracy. The PCA consists of a dedicated timer/counter which serves as the time base for an array of five compare/ capture modules. Its clock input can be programmed to count any one of the following signals:

- Oscillator frequency ÷ 12 (÷ 6 in X2 mode)
- Oscillator frequency ÷ 4 (÷ 2 in X2 mode)
- Timer 0 overflow
- External input on ECI (P1.2)

Each compare/capture modules can be programmed in any one of the following modes:

- rising and/or falling edge capture,
- software timer,
- high-speed output, or
- pulse width modulator.

Module 4 can also be programmed as a watchdog timer (See Section "PCA Watchdog Timer", page 33).

When the compare/capture modules are programmed in the capture mode, software timer, or high speed output mode, an interrupt can be generated when the module executes its function. All five modules plus the PCA timer overflow share one interrupt vector.

The PCA timer/counter and compare/capture modules share Port 1 for external I/O. These pins are listed below. If the port is not used for the PCA, it can still be used for standard I/O.

PCA component	External I/O Pin
16-bit Counter	P1.2 / ECI
16-bit Module 0	P1.3 / CEX0
16-bit Module 1	P1.4 / CEX1
16-bit Module 2	P1.5 / CEX2
16-bit Module 3	P1.6 / CEX3
16-bit Module 4	P1.7 / CEX4

The PCA timer is a common time base for all five modules (See Figure 7). The timer count source is determined from the CPS1 and CPS0 bits in the **CMOD SFR** (See Table 8) and can be programmed to run at:

- 1/12 the oscillator frequency. (Or 1/6 in X2 Mode)
- 1/4 the oscillator frequency. (Or 1/2 in X2 Mode)
- The Timer 0 overflow
- The input on the ECI pin (P1.2)

The CCON SFR contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (Refer to Table 9).

- Bit CR (CCON.6) must be set by software to run the PCA. The PCA is shut off by clearing this bit.
- Bit CF: The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software.
- Bits 0 through 4 are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software.

Table 9. CCON: PCA Counter Control Register

CCON Address 0D8H	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0
Reset value	0	0	X	0	0	0	0	0

Symbol	Function
CF	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.
CR	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
-	Not implemented, reserved for future use.[a]
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

The watchdog timer function is implemented in module 4 (See Figure 10).

The PCA interrupt system is shown in Figure 8

Table 10. CCAPMn: PCA Modules Compare/Capture Control Registers

CCAPMn Address n = 0 - 4	CCAPM0=0DAH CCAPM1=0DBH CCAPM2=0DCH CCAPM3=0DDH CCAPM4=0DEH							
	-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMm	ECCFn
Reset value	X	0	0	0	0	0	0	0

Symbol	Function
-	Not implemented, reserved for future use.[a]
ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.
CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.
CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.
MATn	Match. When MATn = 1, a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.
TOGn	Toggle. When TOGn = 1, a match of the PCA counter with this module's compare/capture register causes the CEXn pin to toggle.
PWMn	Pulse Width Modulation Mode. PWMn = 1 enables the CEXn pin to be used as a pulse width modulated output.
ECCFn	Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

Table 11. PCA Module Modes (CCAPMn Registers)

ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMm	ECCFn	Module Function
0	0	0	0	0	0	0	No Operation
X	1	0	0	0	0	X	16-bit capture by a positive-edge trigger on CEXn
X	0	1	0	0	0	X	16-bit capture by a negative trigger on CEXn
X	1	1	0	0	0	X	16-bit capture by a transition on CEXn
1	0	0	1	0	0	X	16-bit Software Timer / Compare mode.
1	0	0	1	1	0	X	16-bit High Speed Output
1	0	0	0	0	1	0	8-bit PWM
1	0	0	1	X	0	X	Watchdog Timer (module 4 only)

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output (See Table 12 & Table 13)

6.6. TS80C51Rx2 Serial I/O Port

The serial I/O port in the TS80C51Rx2 is compatible with the serial I/O port in the 80C52.
It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

6.6.1. Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 13).

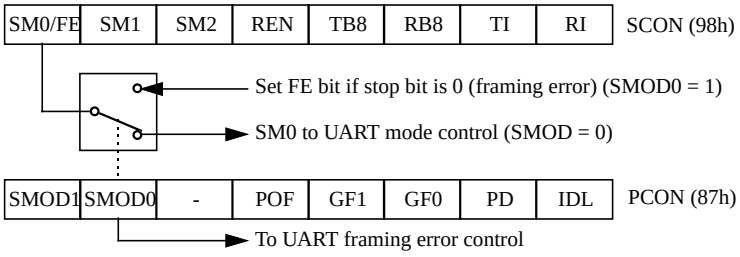


Figure 13. Framing Error Block Diagram

When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 16.) bit is set.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 14. and Figure 15.).

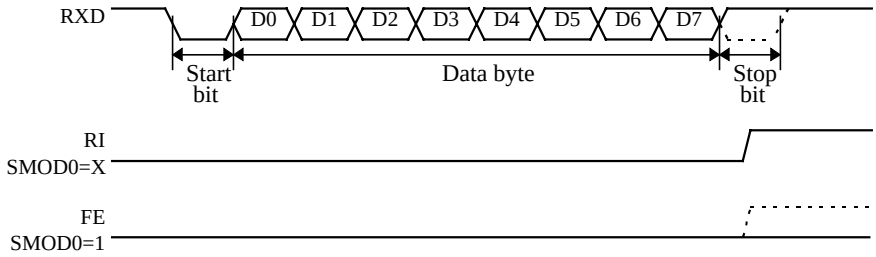


Figure 14. UART Timings in Mode 1

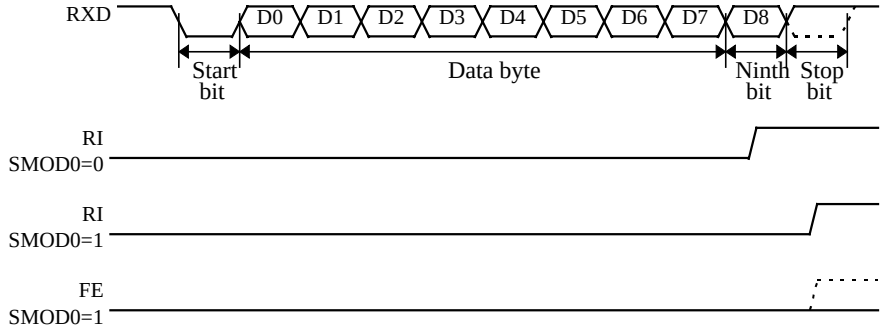


Figure 15. UART Timings in Modes 2 and 3

6.6.2. Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

NOTE: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

Table 16. SCON Register

SCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0
FE/SM0	**SM1**	**SM2**	**REN**	**TB8**	**RB8**	**TI**	**RI**

Bit Number	Bit Mnemonic	Description
7	FE	**Framing Error bit (SMOD0=1)** Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit
	SM0	**Serial port Mode bit 0** Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit
6	SM1	**Serial port Mode bit 1** SM0 SM1 Mode Description Baud Rate 0 0 0 Shift Register F_{XTAL}/12 (/6 in X2 mode) 0 1 1 8-bit UART Variable 1 0 2 9-bit UART F_{XTAL}/64 or F_{XTAL}/32 (/32, /16 in X2 mode) 1 1 3 9-bit UART Variable
5	SM2	**Serial port Mode 2 bit / Multiprocessor Communication Enable bit** Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.
4	REN	**Reception Enable bit** Clear to disable serial reception. Set to enable serial reception.
3	TB8	**Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3.** Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.
2	RB8	**Receiver Bit 8 / Ninth bit received in modes 2 and 3** Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.
1	TI	**Transmit Interrupt flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.
0	RI	**Receive Interrupt flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 14. and Figure 15. in the other modes.

Reset Value = 0000 0000b
Bit addressable

6.8. Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirely : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occured during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

6.9. Power-Down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 17., PCON register).

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. V_{CC} can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts $\overline{INT0}$ and $\overline{INT1}$ are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.
Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 17. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.
Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C51Rx2 into power-down mode.

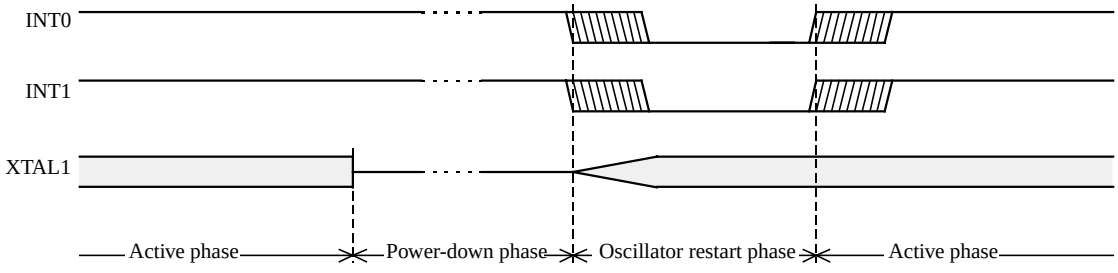


Figure 17. Power-Down Exit Waveform

Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.
NOTE: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

6.10. Hardware Watchdog Timer

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer ReSeT (WDTRST) SFR. The WDT is by default disabled from exiting reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST-pin.

6.10.1. Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST-pin. The RESET pulse duration is 96 x T_{OSC} , where $T_{OSC} = 1/F_{OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

To have a more powerful WDT, a 2^7 counter has been added to extend the Time-out capability, ranking from 16ms to 2s @ F_{OSC} = 12MHz. To manage this feature, refer to WDTPRG register description, Table 24. (SFR0A7h).

Table 23. WDTRST Register

WDTRST Address (0A6h)

	7	6	5	4	3	2	1
Reset value	X	X	X	X	X	X	X

Write only, this SFR is used to reset/enable the WDT by writing 01EH then 0E1H in sequence.

6.13. Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 27. AUXR Register

AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	EXTRAM	AO

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	EXTRAM	**EXTRAM bit** See Table 5.
0	AO	**ALE Output bit** Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = XXXX XX00b
Not bit addressable

7. TS83C51RB2/RC2/RD2 ROM

7.1. ROM Structure

The TS83C51RB2/RC2/RD2 ROM memory is divided in three different arrays:

- the code array: . . . . . 16/32/64 Kbytes.
- the encryption array: . . . . . 64 bytes.
- the signature array:. . . . . 4 bytes.

7.2. ROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

7.2.1. 7.2.1. Encryption Array

Within the ROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

7.2.2. Program Lock Bits

The lock bits when programmed according to Table 28. will provide different level of protection for the on-chip code and data.

Table 28. Program Lock bits

Program Lock Bits				Protection description
Security level	**LB1**	**LB2**	**LB3**	
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	P	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset.
3	U	P	U	Same as level 1+ Verify disable. This security level is only available for 51RDX2 devices.

U: unprogrammed
P: programmed

7.2.3. Signature bytes

The TS83C51RB2/RC2/RD2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 8.3.

7.2.4. Verify Algorithm

Refer to 8.3.4.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{CC} idle	Power Supply Current Maximum values, X1 mode: (7)			0.15 Freq (MHz) + 0.2 @12MHz 2 @16MHz 2.6	mA	V_{CC} = 3.3 V(2)

NOTES

1. I_{CC} under reset is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 24.), V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} - 0.5V; XTAL2 N.C.; $\overline{EA}$ = RST = Port 0 = V_{CC}. I_{CC} would be slightly higher if a crystal oscillator used..

2. Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} - 0.5 V; XTAL2 N.C; Port 0 = V_{CC}; $\overline{EA}$ = RST = V_{SS} (see Figure 22.).

3. Power Down I_{CC} is measured with all output pins disconnected; $\overline{EA}$ = V_{SS}, PORT 0 = V_{CC}; XTAL2 NC.; RST = V_{SS} (see Figure 23.).

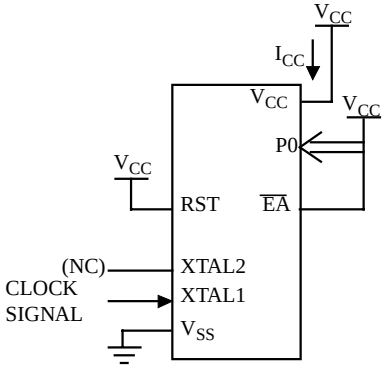
4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi V_{OL} peak 0.6V. A Schmitt Trigger use is not necessary.

5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.

6. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA
Ports 1, 2, 3 and 4 and 5 when available: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

7. For other values, please contact your sales office.

8. Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 24.), V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} - 0.5V; XTAL2 N.C.; $\overline{EA}$ = Port 0 = V_{CC}; RST = V_{SS}. The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.



All other pins are disconnected.

Figure 20. I_{CC} Test Condition, under reset

Table 38. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{LHLL}	Min	2 T - x	T - x	10	8	15	ns
T_{AVLL}	Min	T - x	0.5 T - x	15	13	20	ns
T_{LLAX}	Min	T - x	0.5 T - x	15	13	20	ns
T_{LLIV}	Max	4 T - x	2 T - x	30	22	35	ns
T_{LLPL}	Min	T - x	0.5 T - x	10	8	15	ns
T_{PLPH}	Min	3 T - x	1.5 T - x	20	15	25	ns
T_{PLIV}	Max	3 T - x	1.5 T - x	40	25	45	ns
T_{PXIX}	Min	x	x	0	0	0	ns
T_{PXIZ}	Max	T - x	0.5 T - x	7	5	15	ns
T_{AVIV}	Max	5 T - x	2.5 T - x	40	30	45	ns
T_{PLAZ}	Max	x	x	10	10	10	ns

10.5.3. External Program Memory Read Cycle

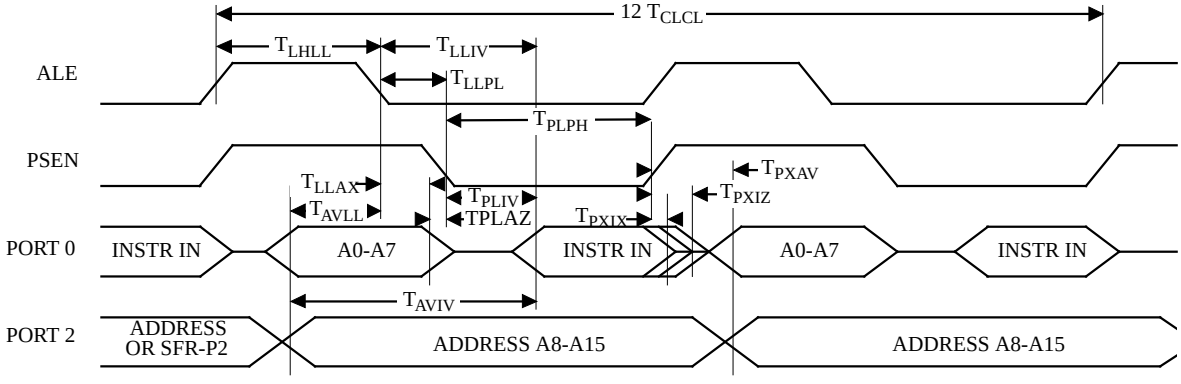


Figure 25. External Program Memory Read Cycle

10.5.4. External Data Memory Characteristics

Table 39. Symbol Description

Symbol	Parameter
T_{RLRH}	$\overline{RD}$ Pulse Width
T_{WLWH}	$\overline{WR}$ Pulse Width
T_{RLDV}	$\overline{RD}$ to Valid Data In
T_{RHDX}	Data Hold After $\overline{RD}$
T_{RHDZ}	Data Float After $\overline{RD}$
T_{LLDV}	ALE to Valid Data In
T_{AVDV}	Address to Valid Data In
T_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$
T_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$
T_{QVWX}	Data Valid to $\overline{WR}$ Transition
T_{QVWH}	Data set-up to $\overline{WR}$ High
T_{WHQX}	Data Hold After $\overline{WR}$
T_{RLAZ}	$\overline{RD}$ Low to Address Float
T_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE high

Table 41. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{RLRH}	Min	6 T - x	3 T - x	20	15	25	ns
T_{WLWH}	Min	6 T - x	3 T - x	20	15	25	ns
T_{RLDV}	Max	5 T - x	2.5 T - x	25	23	30	ns
T_{RHDX}	Min	x	x	0	0	0	ns
T_{RHDZ}	Max	2 T - x	T - x	20	15	25	ns
T_{LLDV}	Max	8 T - x	4T -x	40	35	45	ns
T_{AVDV}	Max	9 T - x	4.5 T - x	60	50	65	ns
T_{LLWL}	Min	3 T - x	1.5 T - x	25	20	30	ns
T_{LLWL}	Max	3 T + x	1.5 T + x	25	20	30	ns
T_{AVWL}	Min	4 T - x	2 T - x	25	20	30	ns
T_{QVWX}	Min	T - x	0.5 T - x	15	10	20	ns
T_{QVWH}	Min	7 T - x	3.5 T - x	15	10	20	ns
T_{WHQX}	Min	T - x	0.5 T - x	10	8	15	ns
T_{RLAZ}	Max	x	x	0	0	0	ns
T_{WHLH}	Min	T - x	0.5 T - x	15	10	20	ns
T_{WHLH}	Max	T + x	0.5 T + x	15	10	20	ns

10.5.5. External Data Memory Write Cycle

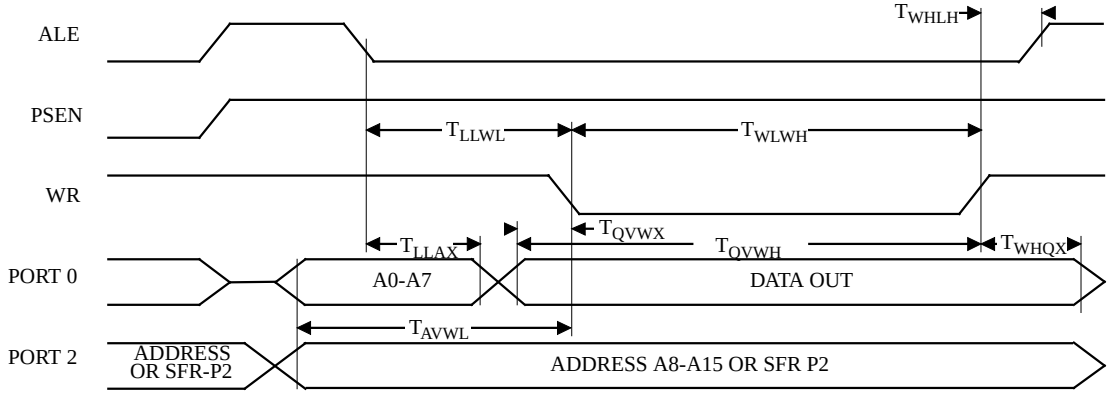


Figure 26. External Data Memory Write Cycle

10.5.11. External Clock Drive Characteristics (XTAL1)

Table 46. AC Parameters

Symbol	Parameter	Min	Max	Units
T_{CLCL}	Oscillator Period	25		ns
T_{CHCX}	High Time	5		ns
T_{CLCX}	Low Time	5		ns
T_{CLCH}	Rise Time		5	ns
T_{CHCL}	Fall Time		5	ns
T_{CHCX}/T_{CLCX}	Cyclic ratio in X2 mode	40	60	%

10.5.12. External Clock Drive Waveforms

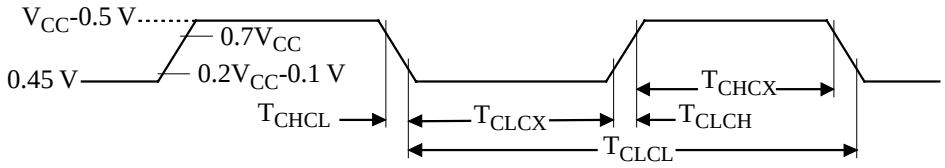


Figure 30. External Clock Drive Waveforms

10.5.13. AC Testing Input/Output Waveforms

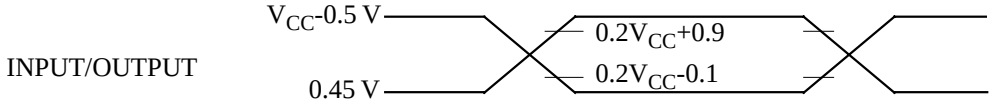


Figure 31. AC Testing Input/Output Waveforms

AC inputs during testing are driven at V_{CC} - 0.5 for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at V_{IH} min for a logic “1” and V_{IL} max for a logic “0”.

10.5.14. Float Waveforms

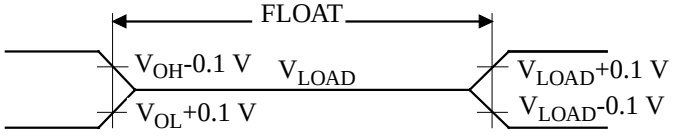


Figure 32. Float Waveforms

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm$ 20mA.

10.5.15. Clock Waveforms

Valid in normal clock mode. In X2 mode XTAL2 signal must be changed to XTAL2 divided by two.

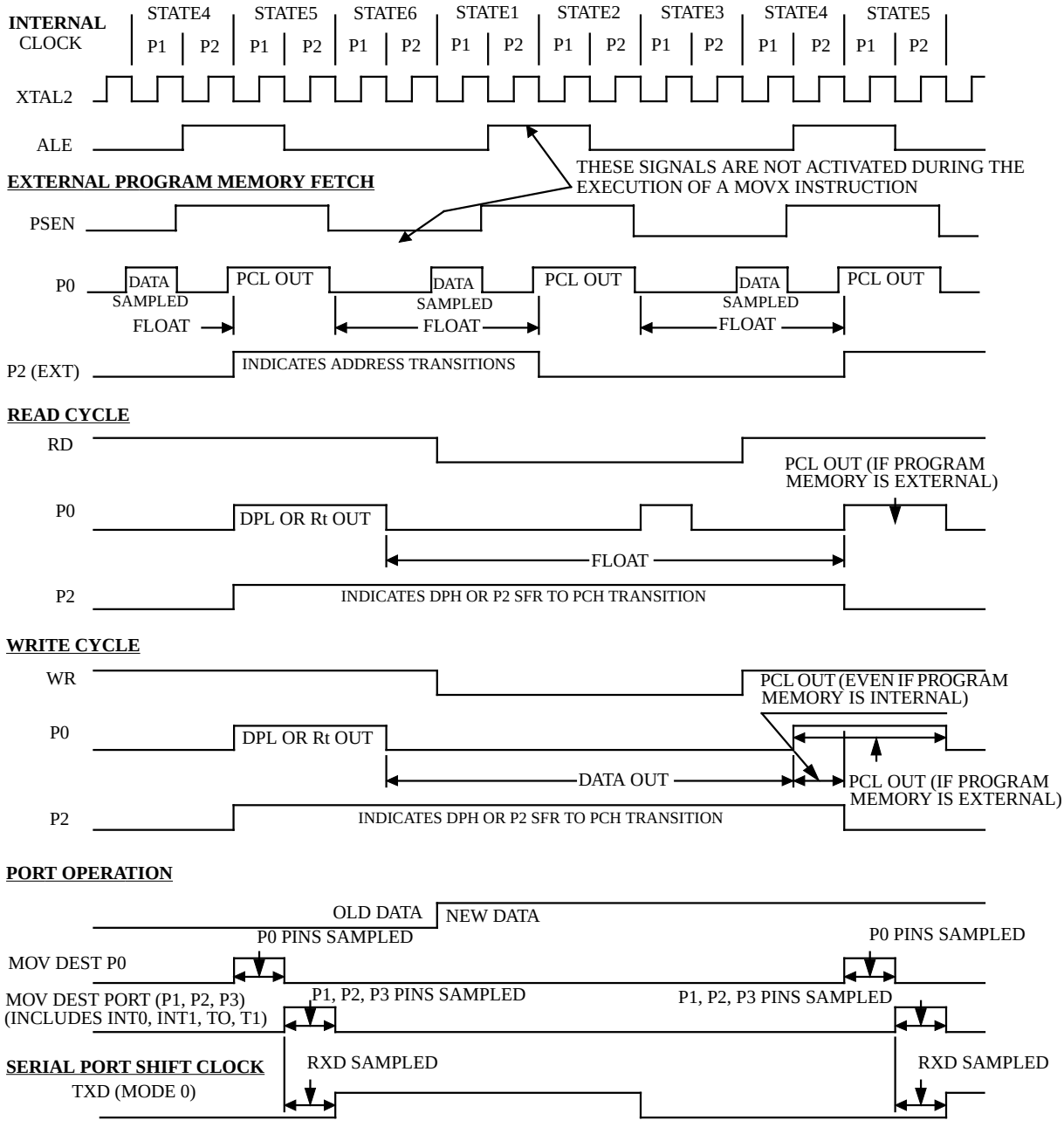


Figure 33. Clock Waveforms

This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (T_A=25°C fully loaded) $\overline{RD}$ and $\overline{WR}$ propagation delays are approximately 50ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

Table 48. Possible Ordering Entries

	TS80C51RA2/RD2 ROMless	TS83C51RB2/RC2/RD2zzz ROM	TS87C51RB2/RC2/RD2 OTP
-MCA	X	X	X
-MCB	X	X	X
-MCE	X	X	X
-MCL	RD2 only	RD2 only	RD2 only
-MCM	RD2 only	RD2 only	RD2 only
-VCA	X	X	X
-VCB	X	X	X
-VCE	X	X	X
-VCL	RD2 only	RD2 only	RD2 only
-VCM	RD2 only	RD2 only	RD2 only
-LCA	X	X	X
-LCB	X	X	X
-LCE	X	X	X
-LCL	RD2 only	RD2 only	RD2 only
-LCM	RD2 only	RD2 only	RD2 only
-MIA	X	X	X
-MIB	X	X	X
-MIE	X	X	X
-MIL	RD2 only	RD2 only	RD2 only
-MIM	RD2 only	RD2 only	RD2 only
-VIA	X	X	X
-VIB	X	X	X
-VIE	X	X	X
-VIL	RD2 only	RD2 only	RD2 only
-VIM	RD2 only	RD2 only	RD2 only
-LIA	X	X	X
-LIB	X	X	X
-LIE	X	X	X
-LIL	RD2 only	RD2 only	RD2 only
-LIM	RD2 only	RD2 only	RD2 only
-EA	X		X
-EB	X		X
-EE	X		X
-EL	RD2 only		RD2 only
-EM	RD2 only		RD2 only
-EJ			RC2 and RD2 only
-EK			RC2 and RD2 only
-EN			RD2 only

- -Ex for samples
- Tape and Reel available for B, E, L and M packages
- Dry pack mandatory for E and M packages