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Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/30MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIL
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c51rb2-via

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



PDIL40 PLCC44 VQFP44 1.4	ROM (bytes)	EPROM (bytes)	XRAM (bytes)	TOTAL RAM (bytes)	I/O
TS80C51RA2	0	0	256	512	32
TS80C51RD2	0	0	768	1024	32
TS83C51RB2	16k	0	256	512	32
TS83C51RC2	32k	0	256	512	32
TS83C51RD2	64k	0	768	1024	32
TS87C51RB2	0	16k	256	512	32
TS87C51RC2	0	32k	256	512	32
TS87C51RD2	0	64k	768	1024	32

PLCC68 VQFP64 1.4	ROM (bytes)	EPROM (bytes)	XRAM (bytes)	TOTAL RAM (bytes)	I/O
TS80C51RD2	0	0	768	1024	48
TS83C51RD2	64k	0	768	1024	48
TS87C51RD2	0	64k	768	1024	48

3. Block Diagram





4. SFR Mapping

The Special Function Registers (SFRs) of the TS80C51Rx2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3, P4, P5
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- HDW Watchdog Timer Reset: WDTRST, WDTPRG
- PCA registers: CL, CH, CCAPiL, CCAPiH, CCON, CMOD, CCAPMi
- Interrupt system registers: IE, IP, IPH
- Others: AUXR, CKCON

Table 1. All SFRs with their address and their reset value

	Bit addressable	Non Bit addressable								
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F		
F8h		CH 0000 0000	CCAP0H XXXX XXXX	CCAP1H XXXX XXXX	CCAPL2H XXXX XXXX	CCAPL3H XXXX XXXX	CCAPL4H XXXX XXXX		F	
F0h	B 0000 0000								F	
E8h	P5 bit addressable 1111 1111	CL 0000 0000	CCAP0L XXXX XXXX	CCAP1L XXXX XXXX	CCAPL2L XXXX XXXX	CCAPL3L XXXX XXXX	CCAPL4L XXXX XXXX		E	
E0h	ACC 0000 0000								E	
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		D	
D0h	PSW 0000 0000								D	
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			C	
C0h	P4 bit addressable 1111 1111							P5 byte addressable 1111 1111	C	
B8h	IP X000 000	SADEN 0000 0000							B	
B0h	P3 1111 1111							IPH X000 0000	В	
A8h	IE 0000 0000	SADDR 0000 0000							A	
A0h	P2 1111 1111		AUXR1 XXXX0XX0				WDTRST XXXX XXXX	WDTPRG XXXX X000	A	
98h	SCON 0000 0000	SBUF XXXX XXXX							91	
90h	P1 1111 1111								9	
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXXXX00	CKCON XXXX XXX0	81	
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	8	
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F		

reserved



		Pin Nu	mber	T		
Mnemonic	DIL	LCC	VQFP 1.4	Туре	Name And Function	
V _{SS}	20	22	16	Ι	Ground: 0V reference	
Vss1		1	39	Ι	Optional Ground: Contact the Sales Office for ground connection.	
V _{CC}	40	44	38	Ι	Power Supply: This is the power supply voltage for normal, idle and power-down operation	
P0.0-P0.7	39-32	43-36	37-30	I/O	Port 0 : Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1 written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to Vcc or Vss in order to prevent any parasitic current consumption Port 0 is also the multiplexed low-order address and data bus during access t external program and data memory. In this application, it uses strong interna pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification durin which P0 outputs the code bytes.	
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-orde address byte during memory programming and verification. Alternate functions for Port 1 include:	
	1	2	40	I/O	T2 (P1.0): Timer/Counter 2 external count input/Clockout	
	2	3	41	I	T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction Control	
	3	4	42	Ι	ECI (P1.2): External Clock for the PCA	
	4	5	43	I/O	CEX0 (P1.3): Capture/Compare External I/O for PCA module 0	
	5	6	44	I/O	CEX1 (P1.4): Capture/Compare External I/O for PCA module 1	
	6	7	45	I/O	CEX0 (P1.5): Capture/Compare External I/O for PCA module 2	
	7	8	46	I/O	CEX0 (P1.6): Capture/Compare External I/O for PCA module 3	
	8	9	47	I/O	CEX0 (P1.7): Capture/Compare External I/O for PCA module 4	
P2.0-P2.7	21-28	24-31	18-25	I/O	CEX0 (P1.7): Capture/Compare External I/O for PCA module 4 Port 2 : Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR).In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR. Some Port 2 pins (P2.0 to P2.5) receive the high order address bits during EPROM programming and verification:	
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port pins that have 1s written to them are pulled high by the internal pull-ups at can be used as inputs. As inputs, Port 3 pins that are externally pulled low w source current because of the internal pull-ups. Some Port 3 pins (P3.4 to P3. receive the high order address bits during EPROM programming and verificatic Port 3 also serves the special features of the 80C51 family, as listed below.	
	10	11	5	I	RXD (P3.0): Serial input port	
	11	13	7	0	TXD (P3.1): Serial output port	
	12	14	8	I	INTO (P3.2): External interrupt 0	
	13	15	9	I	INT1 (P3.3): External interrupt 1	
	14	16	10	I	T0 (P3.4): Timer 0 external input	
	15	17	11	I	T1 (P3.5): Timer 1 external input	
	16	18	12	0	WR (P3.6): External data memory write strobe	
	17	19	13	0	RD (P3.7): External data memory read strobe	



Reset	9	10	4	Ι	Reset: A high on this pin for two machine cycles while the oscillator is running,
					resets the device. An internal diffused resistor to $V_{\mbox{\scriptsize SS}}$ permits a power-on reset
					using only an external capacitor to V_{CC} . If the hardware watchdog reaches its
					time-out, the reset pin becomes an output during the time the internal reset is
					activated.



Mnemonic]	Pin Nu	mber	Туре	Name And Function
ALE/PROG	30	33	27	O (I)	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
PSEN	29	32	26	0	Program Store ENable: The read strobe to external program memory. When executing code from the external program memory, \overrightarrow{PSEN} is activated twice each machine cycle, except that two \overrightarrow{PSEN} activations are skipped during each access to external data memory. \overrightarrow{PSEN} is not activated during fetches from internal program memory.
EA/V _{pp}	31	35	29	I	External Access Enable/Programming Supply Voltage: $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH (RB) or 7FFFH (RC), or FFFFH (RD). If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (RB) or 7FFFH (RC) $\overline{\text{EA}}$ must be held low for ROMless devices. This pin also receives the 12.75V programming supply voltage (V _{PP}) during EPROM programming. If security level 1 is programmed, $\overline{\text{EA}}$ will be internally latched on Reset.
XTAL1	19	21	15	Ι	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	0	Crystal 2: Output from the inverting oscillator amplifier



5.1. Pin Description for 64/68 pin Packages

Port 4 and Port 5 are 8-bit bidirectional I/O ports with internal pull-ups. Pins that have 1 written to them are pulled high by the internal pull ups and can be used as inputs.

As inputs, pins that are externally pulled low will source current because of the internal pull-ups.

Refer to the previous pin description for other pins.

	PLCC68	SQUARE VQFP64 1.4
VSS	51	9/40
VCC	17	8
P0.0	15	6
P0.1	14	5
P0.2	12	3
P0.3	11	2
P0.4	9	64
P0.5	6	61
P0.6	5	60
P0.7	3	59
P1.0	19	10
P1.1	21	12
P1.2	22	13
P1.3	23	14
P1.4	25	16
P1.5	27	18
P1.6	28	19
P1.7	29	20
P2.0	54	43
P2.1	55	44
P2.2	56	45
P2.3	58	47
P2.4	59	48
P2.5	61	50
P2.6	64	53
P2.7	65	54
P3.0	34	25
P3.1	39	28

Table	2.	64/68	Pin	Packages	Configuration
I GOIC		0.00		I uchages	Comparation



Table 3. CKCON Register

CKCON - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	X2

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	X2	CPU and peripheral clock bit Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$).

Reset Value = XXXX XXX0b Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (http://www.atmel-wm.com)



ASSEMBLY LANGUAGE

; Block move using dual data pointers ; Destroys DPTR0, DPTR1, A and PSW ; note: DPS exits opposite of entry state ; unless an extra INC AUXR1 is added

00A2	AUXR1 EQU 0A2H	
; 0000 909000 0003 05A2 0005 004000	MOV DPTR,#SOURCE INC AUXR1 MOV DPTR #DEST	; address of SOURCE ; switch data pointers ; address of DEST
0003 90A000 0008 0008 05A2	LOOP: INC AUXR1	; switch data pointers
000A E0	MOVX A, @DPTR	; get a byte from SOURCE
000B A3	INC DPTR	; increment SOURCE address
000C 05A2	INC AUXRI	; switch data pointers
000E F0	MOVX @DPTR,A	; write the byte to DEST
000F A3	INC DPTR	: increment DEST address
0010 70F6	JNZ LOOP	; check for 0 terminator
0012 05A2	INC AUXR1	; (optional) restore DPS

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.



6.4. Timer 2

The timer 2 in the TS80C51RX2 is compatible with the timer 2 in the 80C52.

It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 6) and T2MOD register (See Table 7). Timer 2 operation is similar to Timer 0 and Timer 1. C/T2 selects $F_{OSC}/12$ (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and $CP/\overline{RL2}$ (T2CON), as described in the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description.

Refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C51RX2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

6.4.1. Auto-Reload Mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 5. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.





Figure 5. Auto-Reload Mode Up/Down Counter (DCEN = 1)

6.4.2. Programmable Clock-Output

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 6) . The input clock increments TL2 at frequency $F_{OSC}/2$. The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers :

$$Clock - OutFrequency = \frac{F_{osc}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, timer 2 has a programmable frequency range of 61 Hz $(F_{OSC}/2^{16})$ to 4 MHz $(F_{OSC}/4)$. The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear C/T2 bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.
- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or a different one depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.



It is possible to use timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.



Figure 6. Clock-Out Mode $C/\overline{T2} = 0$



Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 14. and Figure 15.).







Figure 15. UART Timings in Modes 2 and 3

6.6.2. Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

NOTE: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).



Table 16. SCON Register

SCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0	
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI	
Bit Number	Bit Mnemonic			Descrip	tion			
7	FE	Framing Error bit Clear to reset the Set by hardware SMOD0 must be	Framing Error bit (SMOD0=1) Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit					
	SM0	Serial port Mode bi Refer to SM1 fo SMOD0 must be	Serial port Mode bit 0 Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit					
		Serial port Mode bi	t 1 [1]Mode	Descriptio	on Baud Rate	2		
6	SMI	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	1 2 3	8-bit UAI 9-bit UAI 9-bit UAI	Ister F _{XTAL} /I RT Variable RT F _{XTAL} /6 RT Variable	2 (/6 in X2 mode) 4 or F _{XTAL} /32 (/32	2,/16 in X2 mode)	
5	SM2	Serial port Mode 2 bit / Multiprocessor Communication Enable bit Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.						
4	REN	Reception Enable bit Clear to disable serial reception. Set to enable serial reception.						
3	TB8	Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3. Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.						
2	RB8	Receiver Bit 8 / Ninth bit received in modes 2 and 3 Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.						
1	TI	Transmit Interrupt flag Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.						
0	RI	Receive Interrupt fl Clear to acknow Set by hardware	ag ledge interrupt. at the end of the 8	th bit time in mode	0, see Figure 14.	and Figure 15. in	the other modes.	

Reset Value = 0000 0000b Bit addressable



Table 17. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0		
SMOD1	SMOD) -	POF	GF1	GF0	PD	IDL		
Bit Number	Bit Mnemonic		Description						
7	SMOD1	Serial port Mode bi Set to select dou	t 1 ble baud rate in m	ode 1, 2 or 3.					
6	SMOD0	Serial port Mode bi Clear to select S Set to to select F	Serial port Mode bit 0 Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.						
5	-	Reserved The value read fr	Reserved The value read from this bit is indeterminate. Do not set this bit.						
4	POF	Power-Off Flag Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.							
3	GF1	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.							
2	GF0	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.							
1	PD	Power-Down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.							
0	IDL	Idle mode bit Clear by hardwar Set to enter idle	Idle mode bit Clear by hardware when interrupt or reset occurs. Set to enter idle mode.						

Reset Value = 00X1 0000b Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.



6.8. Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirely : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occured during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

6.9. Power-Down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 17., PCON register).

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. V_{CC} can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts $\overline{INT0}$ and $\overline{INT1}$ are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.

Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 17. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C51Rx2 into power-down mode.



Figure 17. Power-Down Exit Waveform

Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content. NOTE: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.



8. TS87C51RB2/RC2/RD2 EPROM

8.1. EPROM Structure

The TS87C51RB2/RC2/RD2 EPROM is divided in two different arrays:

•	the code array:
•	the encryption array:
In	addition a third non programmable array is implemented:
•	the signature array:

8.2. EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

8.2.1. Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

8.2.2. Program Lock Bits

The three lock bits, when programmed according to Table 29.8.2.3., will provide different level of protection for the on-chip code and data.

Program Lock Bits				Protection description				
Security level	LB1	LB2	LB3					
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.				
2	Р	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, \overline{EA} is sampled and latched on reset, and further programming of the EPROM is disabled.				
3	U	Р	U	Same as 2, also verify is disabled.				
4	U	U	Р	Same as 3, also external execution is disabled.				

Table 29	. Program	Lock	bits
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U: unprogrammed,

P: programmed

WARNING: Security level 2 and 3 should only be programmed after EPROM and Core verification.

8.2.3. Signature bytes

The TS87C51RB2/RC2/RD2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 8.3.





All other pins are disconnected.





All other pins are disconnected.

Figure 22. I_{CC} Test Condition, Idle Mode



Figure 23. I_{CC} Test Condition, Power-Down Mode



Figure 24. Clock Signal Waveform for $I_{\mbox{\scriptsize CC}}$ Tests in Active and Idle Modes



Symbol	Туре	Standard Clock	X2 Clock	-M	-V	-L	Units
T _{LHLL}	Min	2 T - x	T - x	10	8	15	ns
T _{AVLL}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLAX}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLIV}	Max	4 T - x	2 T - x	30	22	35	ns
T _{LLPL}	Min	T - x	0.5 T - x	10	8	15	ns
T _{PLPH}	Min	3 T - x	1.5 T - x	20	15	25	ns
T _{PLIV}	Max	3 T - x	1.5 T - x	40	25	45	ns
T _{PXIX}	Min	x	x	0	0	0	ns
T _{PXIZ}	Max	T - x	0.5 T - x	7	5	15	ns
T _{AVIV}	Max	5 T - x	2.5 T - x	40	30	45	ns
T _{PLAZ}	Max	x	x	10	10	10	ns

 Table 38. AC Parameters for a Variable Clock: derating formula

10.5.3. External Program Memory Read Cycle



Figure 25. External Program Memory Read Cycle



10.5.11. External Clock Drive Characteristics (XTAL1)

Table	46.	AC	Parameters
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Symbol	Parameter	Min	Max	Units
T _{CLCL}	Oscillator Period	25		ns
T _{CHCX}	High Time	5		ns
T _{CLCX}	Low Time	5		ns
T _{CLCH}	Rise Time		5	ns
T _{CHCL}	Fall Time		5	ns
T _{CHCX} /T _{CLCX}	Cyclic ratio in X2 mode	40	60	%

10.5.12. External Clock Drive Waveforms



Figure 30. External Clock Drive Waveforms

10.5.13. AC Testing Input/Output Waveforms



Figure 31. AC Testing Input/Output Waveforms

AC inputs during testing are driven at V_{CC} - 0.5 for a logic "1" and 0.45V for a logic "0". Timing measurement are made at V_{IH} min for a logic "1" and V_{IL} max for a logic "0".

10.5.14. Float Waveforms



Figure 32. Float Waveforms



11. Ordering Information



(*) Check with Atmel Wireless & Microcontrollers Sales Office for availability. Ceramic packages (J, K, N) are available for proto typing, not for volume production. Ceramic packages are available for OTP only.

Table	47.	Maximum	Clock	Frequency
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Code	-M	-V	-L	Unit
Standard Mode, oscillator frequency	40	40	30	MHz
Standard Mode, internal frequency	40	40	30	
X2 Mode, oscillator frequency	20	30	20	MHz
X2 Mode, internal equivalent frequency	40	60	40	