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#### Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/30MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/ts87c51rb2-vib">https://www.e-xfl.com/product-detail/microchip-technology/ts87c51rb2-vib</a>

## 4. SFR Mapping

The Special Function Registers (SFRs) of the TS80C51Rx2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3, P4, P5
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- HDW Watchdog Timer Reset: WDTRST, WDTPRG
- PCA registers: CL, CH, CCAPiL, CCAPiH, CCON, CMOD, CCAPMi
- Interrupt system registers: IE, IP, IPH
- Others: AUXR, CKCON

**Table 1. All SFRs with their address and their reset value**

	Bit addressable	Non Bit addressable							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h		CH 0000 0000	CCAP0H XXXX XXXX	CCAP1H XXXX XXXX	CCAPL2H XXXX XXXX	CCAPL3H XXXX XXXX	CCAPL4H XXXX XXXX		FFh
F0h	B 0000 0000								F7h
E8h	P5 bit addressable 1111 1111	CL 0000 0000	CCAP0L XXXX XXXX	CCAP1L XXXX XXXX	CCAPL2L XXXX XXXX	CCAPL3L XXXX XXXX	CCAPL4L XXXX XXXX		EFh
E0h	ACC 0000 0000								E7h
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		DFh
D0h	PSW 0000 0000								D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0h	P4 bit addressable 1111 1111							P5 byte addressable 1111 1111	C7h
B8h	IP X000 000	SADEN 0000 0000							BFh
B0h	P3 1111 1111							IPH X000 0000	B7h
A8h	IE 0000 0000	SADDR 0000 0000							AFh
A0h	P2 1111 1111		AUXR1 XXXX0XX0				WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh
90h	P1 1111 1111								97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXXXX00	CKCON XXXX XXX0	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

reserved

Reset	9	10	4	I	<b>Reset:</b> A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to $V_{SS}$ permits a power-on reset using only an external capacitor to $V_{CC}$ . If the hardware watchdog reaches its time-out, the reset pin becomes an output during the time the internal reset is activated.
-------	---	----	---	---	---

Mnemonic	Pin Number			Type	Name And Function
ALE/ $\overline{\text{PROG}}$	30	33	27	O (I)	<b>Address Latch Enable/Program Pulse:</b> Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
$\overline{\text{PSEN}}$	29	32	26	O	<b>Program Store ENable:</b> The read strobe to external program memory. When executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
$\overline{\text{EA}}/\text{V}_{\text{PP}}$	31	35	29	I	<b>External Access Enable/Programming Supply Voltage:</b> $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH (RB) or 7FFFH (RC), or FFFFH (RD). If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (RB) or 7FFFH (RC). $\overline{\text{EA}}$ must be held low for ROMless devices. This pin also receives the 12.75V programming supply voltage ( $\text{V}_{\text{PP}}$ ) during EPROM programming. If security level 1 is programmed, $\overline{\text{EA}}$ will be internally latched on Reset.
XTAL1	19	21	15	I	<b>Crystal 1:</b> Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	<b>Crystal 2:</b> Output from the inverting oscillator amplifier

## 5.1. Pin Description for 64/68 pin Packages

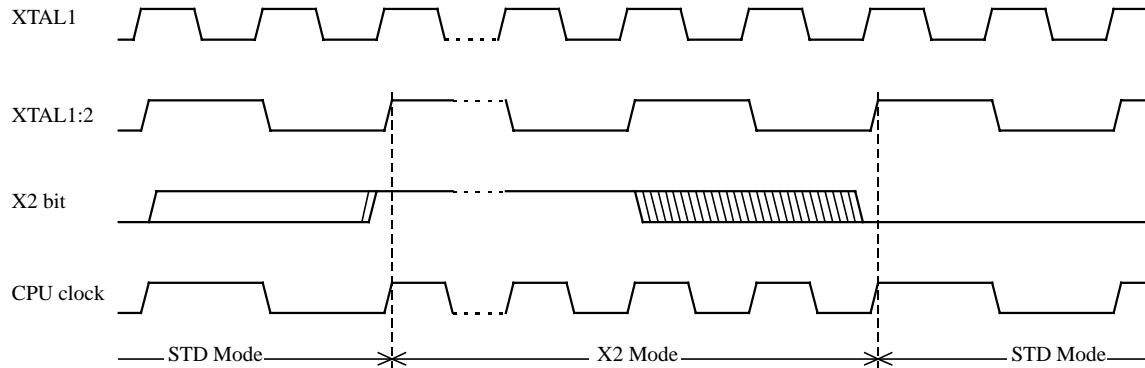
Port 4 and Port 5 are 8-bit bidirectional I/O ports with internal pull-ups. Pins that have 1 written to them are pulled high by the internal pull ups and can be used as inputs.

As inputs, pins that are externally pulled low will source current because of the internal pull-ups.

Refer to the previous pin description for other pins.

**Table 2. 64/68 Pin Packages Configuration**

	<b>PLCC68</b>	<b>SQUARE VQFP64 1.4</b>
VSS	51	9/40
VCC	17	8
P0.0	15	6
P0.1	14	5
P0.2	12	3
P0.3	11	2
P0.4	9	64
P0.5	6	61
P0.6	5	60
P0.7	3	59
P1.0	19	10
P1.1	21	12
P1.2	22	13
P1.3	23	14
P1.4	25	16
P1.5	27	18
P1.6	28	19
P1.7	29	20
P2.0	54	43
P2.1	55	44
P2.2	56	45
P2.3	58	47
P2.4	59	48
P2.5	61	50
P2.6	64	53
P2.7	65	54
P3.0	34	25
P3.1	39	28



**Figure 2. Mode Switching Waveforms**

The X2 bit in the CKCON register (See Table 3.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

#### **CAUTION**

In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers, PCA...) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.

**Table 3. CKCON Register**

**CKCON - Clock Control Register (8Fh)**

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	<b>X2</b>

Bit Number	Bit Mnemonic	Description
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
3	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
2	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
1	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
0	X2	<b>CPU and peripheral clock bit</b> Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$ ). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$ ).

Reset Value = XXXX XXX0b

Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (<http://www.atmel-wm.com>)

## ASSEMBLY LANGUAGE

```

; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2          AUXR1 EQU 0A2H
;
0000 909000    MOV DPTR,#SOURCE      ; address of SOURCE
0003 05A2      INC  AUXR1             ; switch data pointers
0005 90A000    MOV DPTR,#DEST        ; address of DEST
0008          LOOP:
0008 05A2      INC  AUXR1             ; switch data pointers
000A E0        MOVX A,@DPTR          ; get a byte from SOURCE
000B A3        INC  DPTR             ; increment SOURCE address
000C 05A2      INC  AUXR1             ; switch data pointers
000E F0        MOVX @DPTR,A          ; write the byte to DEST
000F A3        INC  DPTR             ; increment DEST address
0010 70F6      JNZ  LOOP             ; check for 0 terminator
0012 05A2      INC  AUXR1            ; (optional) restore DPS

```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.



Table 10. CCAPMn: PCA Modules Compare/Capture Control Registers

CCAPMn Address

n = 0 - 4

CCAPM0=0DAH

CCAPM1=0DBH

CCAPM2=0DCH

CCAPM3=0DDH

CCAPM4=0DEH

	-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn
Reset value	X	0	0	0	0	0	0	0

Symbol	Function
-	Not implemented, reserved for future use. <sup>a</sup>
ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.
CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.
CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.
MATn	Match. When MATn = 1, a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.
TOGn	Toggle. When TOGn = 1, a match of the PCA counter with this module's compare/capture register causes the CEXn pin to toggle.
PWMn	Pulse Width Modulation Mode. PWMn = 1 enables the CEXn pin to be used as a pulse width modulated output.
ECCFn	Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.

- a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

Table 11. PCA Module Modes (CCAPMn Registers)

ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	Module Function
0	0	0	0	0	0	0	No Operation
X	1	0	0	0	0	X	16-bit capture by a positive-edge trigger on CEXn
X	0	1	0	0	0	X	16-bit capture by a negative trigger on CEXn
X	1	1	0	0	0	X	16-bit capture by a transition on CEXn
1	0	0	1	0	0	X	16-bit Software Timer / Compare mode.
1	0	0	1	1	0	X	16-bit High Speed Output
1	0	0	0	0	1	0	8-bit PWM
1	0	0	1	X	0	X	Watchdog Timer (module 4 only)

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output (See Table 12 & Table 13)

**Table 12. CCAPnH: PCA Modules Capture/Compare Registers High**

CCAPnH Address n = 0 - 4	CCAP0H=0FAH CCAP1H=0FBH CCAP2H=0FCH CCAP3H=0FDH CCAP4H=0FEH								
		7	6	5	4	3	2	1	0
	Reset value	0	0	0	0	0	0	0	0

**Table 13. CCAPnL: PCA Modules Capture/Compare Registers Low**

CCAPnL Address n = 0 - 4	CCAP0L=0EAH CCAP1L=0EBH CCAP2L=0ECH CCAP3L=0EDH CCAP4L=0EEH								
		7	6	5	4	3	2	1	0
	Reset value	0	0	0	0	0	0	0	0

**Table 14. CH: PCA Counter High**

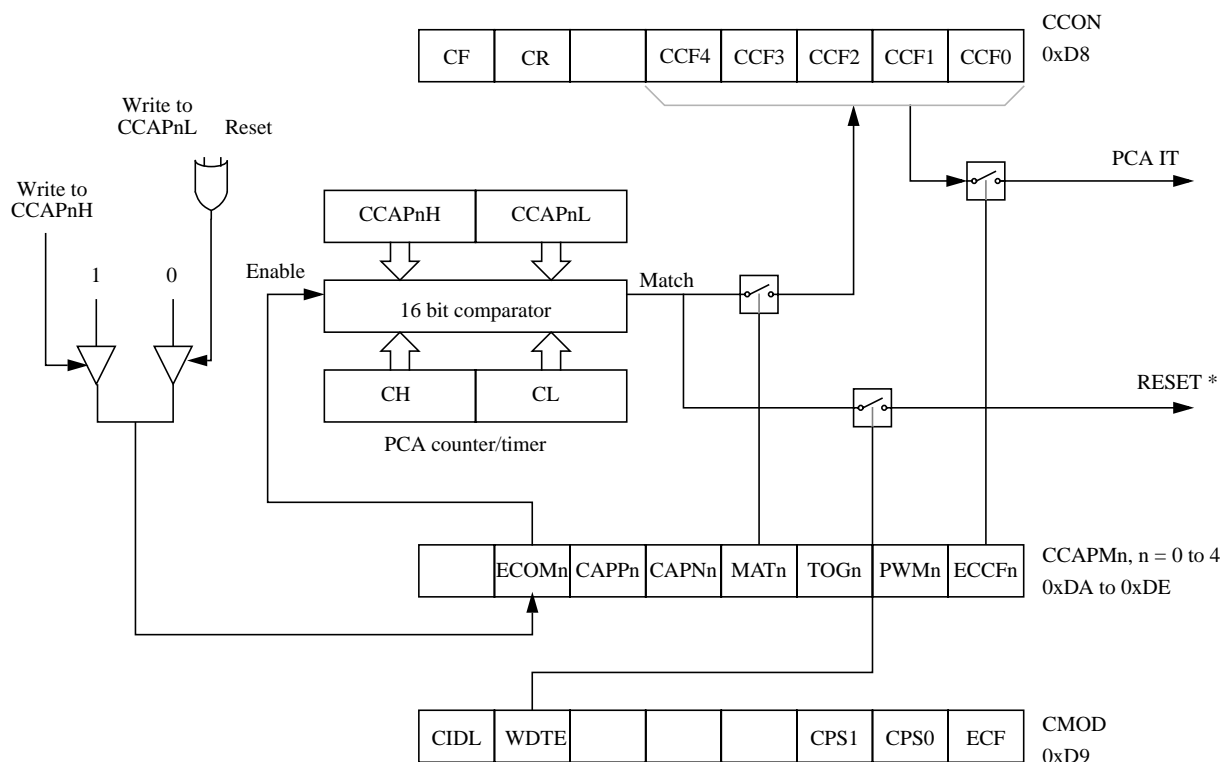
CH Address 0F9H								
	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0

**Table 15. CL: PCA Counter Low**

CL Address 0E9H								
	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0

## 6.5.2. 16-bit Software Timer / Compare Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set (See Figure 10).



\* Only for Module 4

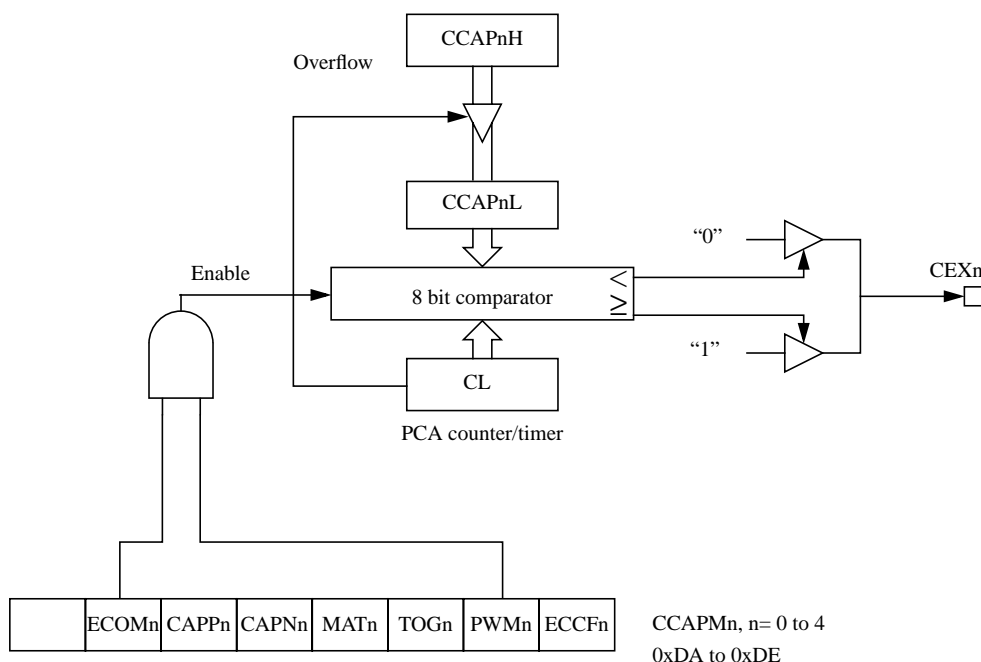
**Figure 10. PCA Compare Mode and PCA Watchdog Timer**

Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen. Writing to CCAPnH will set the ECOM bit.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.

### 6.5.4. Pulse Width Modulator Mode

All of the PCA modules can be used as PWM outputs. Figure 12 shows the PWM function. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in the module's CCAPLn SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn. This allows updating the PWM without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.



**Figure 12. PCA PWM Mode**

### 6.5.5. PCA Watchdog Timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed. Figure 10 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

- 1. periodically change the compare value so it will never match the PCA timer,
- 2. periodically change the PCA timer value so it will never match the compare values, or
- 3. disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for all modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

This watchdog timer won't generate a reset out on the reset pin.

### 6.6.5. Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXXb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

#### SADEN - Slave Address Mask Register (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Not bit addressable

#### SADDR - Slave Address Register (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Not bit addressable

Table 17. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL

Bit Number	Bit Mnemonic	Description
7	SMOD1	<b>Serial port Mode bit 1</b> Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	<b>Serial port Mode bit 0</b> Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	POF	<b>Power-Off Flag</b> Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	<b>Power-Down mode bit</b> Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	<b>Idle mode bit</b> Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b

Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

**Table 22. The state of ports during idle and power-down mode**

Mode	Program Memory	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data*	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data*	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

\* Port 0 can force a "zero" level. A "one" will leave port floating.

## 6.12. Power-Off Flag

The power-off flag allows the user to distinguish between a “cold start” reset and a “warm start” reset.

A cold start reset is the one induced by  $V_{CC}$  switch-on. A warm start reset occurs while  $V_{CC}$  is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 26.). POF is set by hardware when  $V_{CC}$  rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a  $V_{CC}$  range from 4.5V to 5.5V. For lower  $V_{CC}$  value, reading POF bit will return indeterminate value.

**Table 26. PCON Register**

**PCON - Power Control Register (87h)**

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL

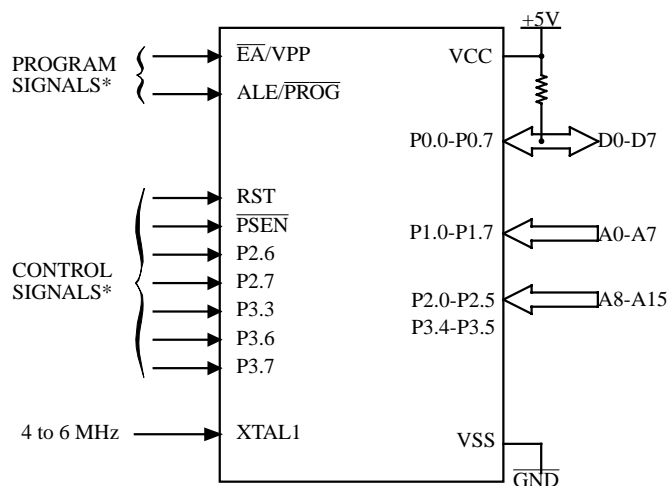
  

Bit Number	Bit Mnemonic	Description
7	SMOD1	<b>Serial port Mode bit 1</b> Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	<b>Serial port Mode bit 0</b> Clear to select SM0 bit in SCON register. Set to select FE bit in SCON register.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	POF	<b>Power-Off Flag</b> Clear to recognize next reset type. Set by hardware when $V_{CC}$ rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	<b>Power-Down mode bit</b> Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	<b>Idle mode bit</b> Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b

Not bit addressable





\* See Table 31. for proper value on these inputs

**Figure 18. Set-Up Modes Configuration**

### 8.3.3. Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the TS87C51RB2/RC2/RD2 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise  $\overline{EA}/VPP$  from VCC to VPP (typical 12.75V).
- Step 5: Pulse  $ALE/\overline{PROG}$  once.
- Step 6: Lower  $\overline{EA}/VPP$  from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 19.).

### 8.3.4. Verify algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C51RB2/RC2/RD2.

P 2.7 is used to enable data output.

To verify the TS87C51RB2/RC2/RD2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 19.)

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.

### 10.3. DC Parameters for Standard Voltage

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ;  $V_{SS} = 0\text{ V}$ ;  $V_{CC} = 5\text{ V} \pm 10\%$ ;  $F = 0$  to  $40\text{ MHz}$ .

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ;  $V_{SS} = 0\text{ V}$ ;  $V_{CC} = 5\text{ V} \pm 10\%$ ;  $F = 0$  to  $40\text{ MHz}$ .

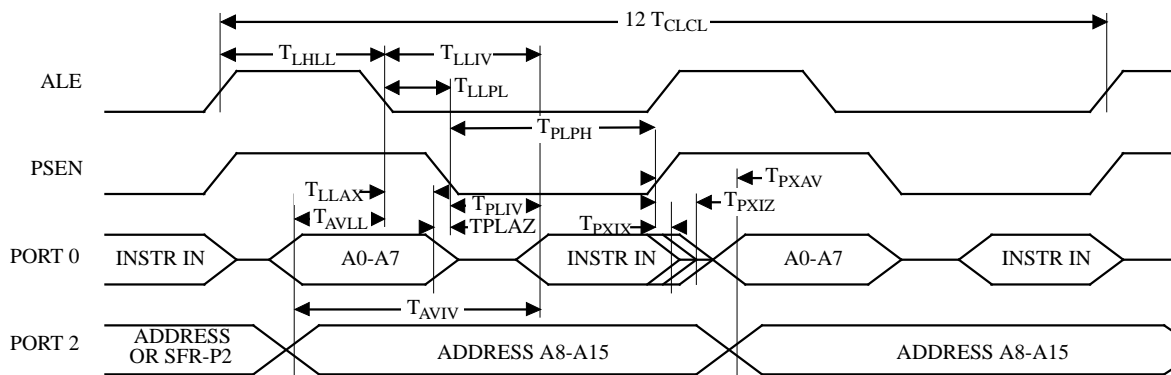
**Table 32. DC Parameters in Standard Voltage**

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$V_{IL}$	Input Low Voltage	-0.5		$0.2 V_{CC} - 0.1$	V	
$V_{IH}$	Input High Voltage except XTAL1, RST	$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
$V_{IH1}$	Input High Voltage, XTAL1, RST	$0.7 V_{CC}$		$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage, ports 1, 2, 3, 4, 5 <sup>(6)</sup>			0.3 0.45 1.0	V V V	$I_{OL} = 100\text{ }\mu\text{A}$ <sup>(4)</sup> $I_{OL} = 1.6\text{ mA}$ <sup>(4)</sup> $I_{OL} = 3.5\text{ mA}$ <sup>(4)</sup>
$V_{OL1}$	Output Low Voltage, port 0 <sup>(6)</sup>			0.3 0.45 1.0	V V V	$I_{OL} = 200\text{ }\mu\text{A}$ <sup>(4)</sup> $I_{OL} = 3.2\text{ mA}$ <sup>(4)</sup> $I_{OL} = 7.0\text{ mA}$ <sup>(4)</sup>
$V_{OL2}$	Output Low Voltage, ALE, $\overline{\text{PSEN}}$			0.3 0.45 1.0	V V V	$I_{OL} = 100\text{ }\mu\text{A}$ <sup>(4)</sup> $I_{OL} = 1.6\text{ mA}$ <sup>(4)</sup> $I_{OL} = 3.5\text{ mA}$ <sup>(4)</sup>
$V_{OH}$	Output High Voltage, ports 1, 2, 3, 4, 5	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V V V	$I_{OH} = -10\text{ }\mu\text{A}$ $I_{OH} = -30\text{ }\mu\text{A}$ $I_{OH} = -60\text{ }\mu\text{A}$ $V_{CC} = 5\text{ V} \pm 10\%$
$V_{OH1}$	Output High Voltage, port 0	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V V V	$I_{OH} = -200\text{ }\mu\text{A}$ $I_{OH} = -3.2\text{ mA}$ $I_{OH} = -7.0\text{ mA}$ $V_{CC} = 5\text{ V} \pm 10\%$
$V_{OH2}$	Output High Voltage, ALE, $\overline{\text{PSEN}}$	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V V V	$I_{OH} = -100\text{ }\mu\text{A}$ $I_{OH} = -1.6\text{ mA}$ $I_{OH} = -3.5\text{ mA}$ $V_{CC} = 5\text{ V} \pm 10\%$
$R_{RST}$	RST Pulldown Resistor	50	90 <sup>(5)</sup>	200	k $\Omega$	
$I_{IL}$	Logical 0 Input Current ports 1, 2, 3, 4, 5			-50	$\mu\text{A}$	$V_{in} = 0.45\text{ V}$
$I_{LI}$	Input Leakage Current			$\pm 10$	$\mu\text{A}$	$0.45\text{ V} < V_{in} < V_{CC}$
$I_{TL}$	Logical 1 to 0 Transition Current, ports 1, 2, 3, 4, 5			-650	$\mu\text{A}$	$V_{in} = 2.0\text{ V}$
$C_{IO}$	Capacitance of I/O Buffer			10	pF	$F_c = 1\text{ MHz}$ $T_A = 25^\circ\text{C}$
$I_{PD}$	Power Down Current		20 <sup>(5)</sup>	50	$\mu\text{A}$	$2.0\text{ V} < V_{CC} < 5.5\text{ V}$ <sup>(3)</sup>
$I_{CC}$ under RESET	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			1 + 0.4 Freq (MHz) @12MHz 5.8 @16MHz 7.4	mA	$V_{CC} = 5.5\text{ V}$ <sup>(1)</sup>

**Table 38. AC Parameters for a Variable Clock: derating formula**

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
$T_{LHLL}$	Min	$2 T - x$	$T - x$	10	8	15	ns
$T_{AVLL}$	Min	$T - x$	$0.5 T - x$	15	13	20	ns
$T_{LLAX}$	Min	$T - x$	$0.5 T - x$	15	13	20	ns
$T_{LLIV}$	Max	$4 T - x$	$2 T - x$	30	22	35	ns
$T_{LLPL}$	Min	$T - x$	$0.5 T - x$	10	8	15	ns
$T_{PLPH}$	Min	$3 T - x$	$1.5 T - x$	20	15	25	ns
$T_{PLIV}$	Max	$3 T - x$	$1.5 T - x$	40	25	45	ns
$T_{PXIX}$	Min	x	x	0	0	0	ns
$T_{PXIZ}$	Max	$T - x$	$0.5 T - x$	7	5	15	ns
$T_{AVIV}$	Max	$5 T - x$	$2.5 T - x$	40	30	45	ns
$T_{PLAZ}$	Max	x	x	10	10	10	ns

### 10.5.3. External Program Memory Read Cycle



**Figure 25. External Program Memory Read Cycle**

#### 10.5.4. External Data Memory Characteristics

**Table 39. Symbol Description**

Symbol	Parameter
$T_{RLRH}$	$\overline{RD}$ Pulse Width
$T_{WLWH}$	$\overline{WR}$ Pulse Width
$T_{RLDV}$	$\overline{RD}$ to Valid Data In
$T_{RHDX}$	Data Hold After $\overline{RD}$
$T_{RHDZ}$	Data Float After $\overline{RD}$
$T_{LLDV}$	ALE to Valid Data In
$T_{AVDV}$	Address to Valid Data In
$T_{LLWL}$	ALE to $\overline{WR}$ or $\overline{RD}$
$T_{AVWL}$	Address to $\overline{WR}$ or $\overline{RD}$
$T_{QVWX}$	Data Valid to $\overline{WR}$ Transition
$T_{QVWH}$	Data set-up to $\overline{WR}$ High
$T_{WHQX}$	Data Hold After $\overline{WR}$
$T_{RLAZ}$	$\overline{RD}$ Low to Address Float
$T_{WHLH}$	$\overline{RD}$ or $\overline{WR}$ High to ALE high

## 11. Ordering Information

TS	87C51RD2	-M	C	B	R
	-M: VCC: 5V +/- 10% 40 MHz, X1 mode 20 MHz, X2 mode -V: VCC: 5V +/- 10% 40 MHz, X1 mode 30 MHz, X2 mode -L: VCC: 2.7 to 5.5 V 30 MHz, X1 mode 20 MHz, X2 mode -E: Samples		Packages: A: PDIL 40 B: PLCC 44 E: VQFP 44 (1.4mm)  J: Window CDIL 40* K: Window CQPJ 44* L: PLCC68 (RD devices only)* M: VQFP64, square package, 1.4mm (RD devices only)* N: JLCC68 (RD devices only)*		Conditioning R: Tape & Reel D: Dry Pack B: Tape & Reel and Dry Pack
Part Number 80C51RA2 (ROMless, 256 bytes XRAM) 80C51RD2 (ROMless, 768bytes XRAM) 83C51RB2zzz (16k ROM, zzz is the customer code) 83C51RC2zzz (32k ROM, zzz is the customer code) 83C51RD2zzz (64k ROM, zzz is the customer code) 87C51RB2 (16k OTP EPROM) 87C51RC2 (32k OTP EPROM) 87C51RD2 (64k OTP EPROM)					
Temperature Range C: Commercial 0 to 70°C I: Industrial -40 to 85°C					

(\*) Check with Atmel Wireless & Microcontrollers Sales Office for availability. Ceramic packages (J, K, N) are available for prototyping, not for volume production. Ceramic packages are available for OTP only.

**Table 47. Maximum Clock Frequency**

Code	-M	-V	-L	Unit
Standard Mode, oscillator frequency	40	40	30	MHz
Standard Mode, internal frequency	40	40	30	
X2 Mode, oscillator frequency	20	30	20	MHz
X2 Mode, internal equivalent frequency	40	<b>60</b>	<b>40</b>	