



Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIL
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c51rc2-lca

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



PDIL40 PLCC44 VQFP44 1.4	ROM (bytes)	EPROM (bytes)	XRAM (bytes)	TOTAL RAM (bytes)	I/O
TS80C51RA2	0	0	256	512	32
TS80C51RD2	0	0	768	1024	32
TS83C51RB2	16k	0	256	512	32
TS83C51RC2	32k	0	256	512	32
TS83C51RD2	64k	0	768	1024	32
TS87C51RB2	0	16k	256	512	32
TS87C51RC2	0	32k	256	512	32
TS87C51RD2	0	64k	768	1024	32

PLCC68 VQFP64 1.4	ROM (bytes)	EPROM (bytes)	XRAM (bytes)	TOTAL RAM (bytes)	I/O
TS80C51RD2	0	0	768	1024	48
TS83C51RD2	64k	0	768	1024	48
TS87C51RD2	0	64k	768	1024	48

# 3. Block Diagram





# 4. SFR Mapping

The Special Function Registers (SFRs) of the TS80C51Rx2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3, P4, P5
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- HDW Watchdog Timer Reset: WDTRST, WDTPRG
- PCA registers: CL, CH, CCAPiL, CCAPiH, CCON, CMOD, CCAPMi
- Interrupt system registers: IE, IP, IPH
- Others: AUXR, CKCON

#### Table 1. All SFRs with their address and their reset value

	Bit addressable			Noi	n Bit address	able			
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h		CH 0000 0000	CCAP0H XXXX XXXX	CCAP1H XXXX XXXX	CCAPL2H XXXX XXXX	CCAPL3H XXXX XXXX	CCAPL4H XXXX XXXX		F
F0h	B 0000 0000								F
E8h	P5 bit addressable 1111 1111	CL 0000 0000	CCAP0L XXXX XXXX	CCAP1L XXXX XXXX	CCAPL2L XXXX XXXX	CCAPL3L XXXX XXXX	CCAPL4L XXXX XXXX		E
E0h	ACC 0000 0000								E
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		D
D0h	PSW 0000 0000								D
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			C
C0h	P4 bit addressable 1111 1111							P5 byte addressable 1111 1111	C
B8h	IP X000 000	SADEN 0000 0000							B
B0h	P3 1111 1111							IPH X000 0000	В
A8h	IE 0000 0000	SADDR 0000 0000							A
A0h	P2 1111 1111		AUXR1 XXXX0XX0				WDTRST XXXX XXXX	WDTPRG XXXX X000	A
98h	SCON 0000 0000	SBUF XXXX XXXX							91
90h	P1 1111 1111								9
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXXXX00	CKCON XXXX XXX0	81
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	8
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

reserved



## **5. Pin Configuration**



\*NIC: No Internal Connection







The X2 bit in the CKCON register (See Table 3.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

### CAUTION

In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers, PCA...) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.



### 6.4. Timer 2

The timer 2 in the TS80C51RX2 is compatible with the timer 2 in the 80C52.

It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 6) and T2MOD register (See Table 7). Timer 2 operation is similar to Timer 0 and Timer 1. C/T2 selects  $F_{OSC}/12$  (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and  $CP/\overline{RL2}$  (T2CON), as described in the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description.

Refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C51RX2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

### 6.4.1. Auto-Reload Mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 5. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.



It is possible to use timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.



Figure 6. Clock-Out Mode  $C/\overline{T2} = 0$ 

CCA



Table 10.	<b>CCAPMn:</b>	PCA	Modules	Compare/Capt	ure Control	Registers
-----------	----------------	-----	---------	--------------	-------------	-----------

.PMn A n = 0 -	PMn Address n = 0 - 4 CCAPN CCAPN CCAPN CCAPN		M0=0DAH M1=0DBH M2=0DCH M3=0DDH M4=0DEH									
				-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMm	ECCFn	
		Res	et value	Х	0	0	0	0	0	0	0	
	Syı	nbol	Function	l								
	-		Not implen	ot implemented, reserved for future use. <sup>a</sup>								
	ECOM	In	Enable Cor	Enable Comparator. ECOMn = 1 enables the comparator function.								
	CAPP	n	Capture Po	Capture Positive, CAPPn = 1 enables positive edge capture.								
	CAPN	n	Capture Ne	apture Negative, CAPNn = 1 enables negative edge capture.								
	MATn	1	Match. Wh register cau	Match. When MATn = 1, a match of the PCA counter with this module's compare/capture egister causes the CCFn bit in CCON to be set, flagging an interrupt.								
	TOGn		Toggle. Wi register cau	loggle. When $TOGn = 1$ , a match of the PCA counter with this module's compare/capture egister causes the CEXn pin to toggle.								
	PWM	1	Pulse Widt modulated	ulse Width Modulation Mode. PWMn = 1 enables the CEXn pin to be used as a pulse width nodulated output.								
	ECCF	n	Enable CC	F interrupt	. Enables o	compare/ca	apture flag	CCFn in t	the CCON	register to	generate	

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMm	ECCFn	Module Function
0	0	0	0	0	0	0	No Operation
X	1	0	0	0	0	Х	16-bit capture by a positive-edge trigger on CEXn
X	0	1	0	0	0	Х	16-bit capture by a negative trigger on CEXn
X	1	1	0	0	0	Х	16-bit capture by a transition on CEXn
1	0	0	1	0	0	Х	16-bit Software Timer / Compare mode.
1	0	0	1	1	0	Х	16-bit High Speed Output
1	0	0	0	0	1	0	8-bit PWM
1	0	0	1	Х	0	Х	Watchdog Timer (module 4 only)

Table 11. PCA Module Modes (CCAPMn Registers)

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output (See Table 12 & Table 13)



## 6.5.1. PCA Capture Mode

To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated (Refer to Figure 9).



Figure 9. PCA Capture Mode



### 6.5.4. Pulse Width Modulator Mode

All of the PCA modules can be used as PWM outputs. Figure 12 shows the PWM function. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in the module's CCAPLn SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn. This allows updating the PWM without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.



Figure 12. PCA PWM Mode

## 6.5.5. PCA Watchdog Timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed. Figure 10 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

- 1. periodically change the compare value so it will never match the PCA timer,
- 2. periodically change the PCA timer value so it will never match the compare values, or
- 3. disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for all modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

This watchdog timer won't generate a reset out on the reset pin.



### 6.6.5. Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

### SADEN - Slave Address Mask Register (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b Not bit addressable

#### SADDR - Slave Address Register (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b Not bit addressable



### 6.7. Interrupt System

The TS80C51Rx2 has a total of 7 interrupt vectors: two external interrupts ( $\overline{INT0}$  and  $\overline{INT1}$ ), three timer interrupts (timers 0, 1 and 2), the serial port interrupt and the PCA global interrupt. These interrupts are shown in Figure 16.

WARNING: Note that in the first version of RC devices, the PCA interrupt is in the lowest priority. Thus the order in INTO, TF0, INT1, TF1, RI or TI, TF2 or EXF2, PCA.



#### Figure 16. Interrupt Control System

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 19.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 20.) and in the Interrupt Priority High register (See Table 21.). shows the bit values and priority levels associated with each combination.

The PCA interrupt vector is located at address 0033H. All other vector addresses are the same as standard C52 devices.



Table	22.	The	state	of	ports	during	idle	and	power-down	mode
-------	-----	-----	-------	----	-------	--------	------	-----	------------	------

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data*	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data*	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

\* Port 0 can force a "zero" level. A "one" will leave port floating.



### 6.12. Power-Off Flag

The power-off flag allows the user to distinguish between a "cold start" reset and a "warm start" reset.

A cold start reset is the one induced by  $V_{CC}$  switch-on. A warm start reset occurs while  $V_{CC}$  is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 26.). POF is set by hardware when  $V_{CC}$  rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a Vcc range from 4.5V to 5.5V. For lower Vcc value, reading POF bit will return indeterminate value.

#### Table 26. PCON Register

#### PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0			
SMOD1	SMOD	-	PD	IDL						
Bit Number	Bit Mnemonic		Description							
7	SMOD1	Serial port Mode bit Set to select dou	1 ble baud rate in m	ode 1, 2 or 3.						
6	SMOD0	Serial port Mode bit Clear to select SI Set to to select F	0 M0 bit in SCON re E bit in SCON reg	egister. ister.						
5	-	<b>Reserved</b> The value read fr	om this bit is inde	terminate. Do not s	et this bit.					
4	POF	Power-Off Flag Clear to recogniz Set by hardware	e next reset type. when V <sub>CC</sub> rises fr	om 0 to its nomina	l voltage. Can also	be set by software	·.			
3	GF1	General purpose Fla Cleared by user f Set by user for g	<b>g</b> or general purpose eneral purpose usa	e usage. ge.						
2	GF0	General purpose Fla Cleared by user f Set by user for g	<b>g</b> or general purpose eneral purpose usa	e usage. ge.						
1	PD	Power-Down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.								
0	IDL	Idle mode bit Clear by hardwar Set to enter idle r	e when interrupt on ode.	or reset occurs.						

Reset Value = 00X1 0000b Not bit addressable



# **10. Electrical Characteristics**

## 10.1. Absolute Maximum Ratings <sup>(1)</sup>

Ambiant Temperature Under Bias:	
C = commercial	0°C to 70°C
I = industrial	-40°C to 85°C
Storage Temperature	-65°C to + 150°C
Voltage on V <sub>CC</sub> to V <sub>SS</sub>	-0.5 V to + 7 V
Voltage on V <sub>PP</sub> to V <sub>SS</sub>	-0.5 V to + 13 V
Voltage on Any Pin to V <sub>SS</sub>	-0.5 V to $V_{CC}$ + 0.5 V
Power Dissipation	$1 W^{(2)}$

NOTES

1. Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

### 10.2. Power consumption measurement

Since the introduction of the first C51 devices, every manufacturer made operating Icc measurements under reset, which made sense for the designs were the CPU was running under reset. In Atmel Wireless & Microcontrollers new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That's why, while keeping measurements under Reset, Atmel Wireless & Microcontrollers presents a new way to measure the operating Icc:

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA = Vcc, RST = Vss, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating Icc.



Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
I <sub>CC</sub> idle	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			0.15 Freq (MHz) + 0.2 @12MHz 2 @16MHz 2.6	mA	$V_{CC} = 3.3 V^{(2)}$

NOTES

1.  $I_{CC}$  under reset is measured with all output pins disconnected; XTAL1 driven with  $T_{CLCH}$ ,  $T_{CHCL} = 5$  ns (see Figure 24.),  $V_{IL} = V_{SS} + 0.5$  V,  $V_{IH} = V_{CC} - 0.5$ V; XTAL2 N.C.;  $\overline{EA} = RST = Port \ 0 = V_{CC}$ .  $I_{CC}$  would be slightly higher if a crystal oscillator used.

2. Idle  $I_{CC}$  is measured with all output pins disconnected; XTAL1 driven with  $T_{CLCH}$ ,  $T_{CHCL} = 5$  ns,  $V_{IL} = V_{SS} + 0.5$  V,  $V_{IH} = V_{CC} - 0.5$  V; XTAL2 N.C; Port  $0 = V_{CC}$ ;  $\overline{EA} = RST = V_{SS}$  (see Figure 22.).

3. Power Down  $I_{CC}$  is measured with all output pins disconnected;  $\overline{EA} = V_{SS}$ , PORT  $0 = V_{CC}$ ; XTAL2 NC.; RST =  $V_{SS}$  (see Figure 23.).

4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the  $V_{OL}s$  of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi  $V_{OL}$  peak 0.6V. A Schmitt Trigger use is not necessary.

5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.

6. Under steady state (non-transient) conditions, I<sub>OL</sub> must be externally limited as follows:

Maximum I<sub>OL</sub> per port pin: 10 mA Maximum I<sub>OL</sub> per 8-bit port:

Port 0: 26 mA

Ports 1, 2, 3 and 4 and 5 when available: 15 mA

Maximum total I<sub>OL</sub> for all output pins: 71 mA

If  $I_{OL}$  exceeds the test condition,  $V_{OL}$  may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions. 7. For other values, please contact your sales office.

8. Operating  $I_{CC}$  is measured with all output pins disconnected; XTAL1 driven with  $T_{CLCH}$ ,  $T_{CHCL} = 5$  ns (see Figure 24.),  $V_{IL} = V_{SS} + 0.5$  V,

 $V_{IH} = V_{CC} - 0.5V$ ; XTAL2 N.C.;  $\overline{EA} = Port 0 = V_{CC}$ ; RST =  $V_{SS}$ . The internal ROM runs the code 80 FE (label: SJMP label).  $I_{CC}$  would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.



All other pins are disconnected.

Figure 20. I<sub>CC</sub> Test Condition, under reset





All other pins are disconnected.





All other pins are disconnected.

Figure 22. I<sub>CC</sub> Test Condition, Idle Mode



Figure 23. I<sub>CC</sub> Test Condition, Power-Down Mode



Figure 24. Clock Signal Waveform for  $I_{\mbox{\scriptsize CC}}$  Tests in Active and Idle Modes



## **10.5.2. External Program Memory Characteristics**

Table 36. Symbol Description	Table 3	36.	Symbol	Description
------------------------------	---------	-----	--------	-------------

Symbol	Parameter
Т	Oscillator clock period
T <sub>LHLL</sub>	ALE pulse width
T <sub>AVLL</sub>	Address Valid to ALE
T <sub>LLAX</sub>	Address Hold After ALE
T <sub>LLIV</sub>	ALE to Valid Instruction In
T <sub>LLPL</sub>	ALE to PSEN
T <sub>PLPH</sub>	PSEN Pulse Width
T <sub>PLIV</sub>	PSEN to Valid Instruction In
T <sub>PXIX</sub>	Input Instruction Hold After PSEN
T <sub>PXIZ</sub>	Input Instruction FloatAfter PSEN
T <sub>PXAV</sub>	PSEN to Address Valid
T <sub>AVIV</sub>	Address to Valid Instruction In
T <sub>PLAZ</sub>	PSEN Low to Address Float

### Table 37. AC Parameters for Fix Clock

Speed	-1 40 N	М ЛНz	X2 r 30 M 60 MH	V node MHz z equiv.	standar 40 N	V rd mode MHz	X2 r 20 N 40 MH	L node MHz z equiv.	standar 30 N	L <sup>.</sup> d mode ⁄IHz	Units
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Т	25		33		25		50		33		ns
T <sub>LHLL</sub>	40		25		42		35		52		ns
T <sub>AVLL</sub>	10		4		12		5		13		ns
T <sub>LLAX</sub>	10		4		12		5		13		ns
T <sub>LLIV</sub>		70		45		78		65		98	ns
T <sub>LLPL</sub>	15		9		17		10		18		ns
T <sub>PLPH</sub>	55		35		60		50		75		ns
T <sub>PLIV</sub>		35		25		50		30		55	ns
T <sub>PXIX</sub>	0		0		0		0		0		ns
T <sub>PXIZ</sub>		18		12		20		10		18	ns
T <sub>AVIV</sub>		85		53		95		80		122	ns
T <sub>PLAZ</sub>		10		10		10		10		10	ns



### **10.5.9. EPROM Programming and Verification Characteristics**

TA = 21°C to 27°C;  $V_{SS} = 0V$ ;  $V_{CC} = 5V \pm 10\%$  while programming.  $V_{CC}$  = operating range while verifying

Symbol	Parameter	Min	Max	Units
V <sub>PP</sub>	Programming Supply Voltage	12.5	13	V
I <sub>PP</sub>	Programming Supply Current		75	mA
1/T <sub>CLCL</sub>	Oscillator Frquency	4	6	MHz
T <sub>AVGL</sub>	Address Setup to PROG Low	48 T <sub>CLCL</sub>		
T <sub>GHAX</sub>	Adress Hold after PROG	48 T <sub>CLCL</sub>		
T <sub>DVGL</sub>	Data Setup to PROG Low	48 T <sub>CLCL</sub>		
T <sub>GHDX</sub>	Data Hold after PROG	48 T <sub>CLCL</sub>		
T <sub>EHSH</sub>	(Enable) High to V <sub>PP</sub>	48 T <sub>CLCL</sub>		
T <sub>SHGL</sub>	V <sub>PP</sub> Setup to PROG Low	10		μs
T <sub>GHSL</sub>	V <sub>PP</sub> Hold after PROG	10		μs
T <sub>GLGH</sub>	PROG Width	90	110	μs
T <sub>AVQV</sub>	Address to Valid Data		48 T <sub>CLCL</sub>	
T <sub>ELQV</sub>	ENABLE Low to Data Valid		48 T <sub>CLCL</sub>	
T <sub>EHQZ</sub>	Data Float after ENABLE	0	48 T <sub>CLCL</sub>	

### Table 45. EPROM Programming Parameters

### 10.5.10. EPROM Programming and Verification Waveforms



\* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

#### Figure 29. EPROM Programming and Verification Waveforms



# 11. Ordering Information



(\*) Check with Atmel Wireless & Microcontrollers Sales Office for availability. Ceramic packages (J, K, N) are available for proto typing, not for volume production. Ceramic packages are available for OTP only.

Table	47.	Maximum	Clock	Frequency
-------	-----	---------	-------	-----------

Code	-M	-V	-L	Unit
Standard Mode, oscillator frequency	40	40	30	MHz
Standard Mode, internal frequency	40	40	30	
X2 Mode, oscillator frequency	20	30	20	MHz
X2 Mode, internal equivalent frequency	40	<b>60</b>	<b>40</b>	



	TS80C51RA2/RD2 ROMless	TS83C51RB2/RC2/RD2zzz ROM	TS87C51RB2/RC2/RD2 OTP
-MCA	Х	Х	X
-MCB	X	Х	X
-MCE	X	X	X
-MCL	RD2 only	RD2 only	RD2 only
-MCM	RD2 only	RD2 only	RD2 only
-VCA	Х	Х	X
-VCB	X	X	X
-VCE	X	Х	X
-VCL	RD2 only	RD2 only	RD2 only
-VCM	RD2 only	RD2 only	RD2 only
-LCA	Х	Х	X
-LCB	X	Х	X
-LCE	X	Х	X
-LCL	RD2 only	RD2 only	RD2 only
-LCM	RD2 only	RD2 only	RD2 only
-MIA	Х	Х	X
-MIB	X	X	X
-MIE	Х	Х	X
-MIL	RD2 only	RD2 only	RD2 only
-MIM	RD2 only	RD2 only	RD2 only
-VIA	Х	Х	X
-VIB	X	X	X
-VIE	X	X	X
-VIL	RD2 only	RD2 only	RD2 only
-VIM	RD2 only	RD2 only	RD2 only
-LIA	Х	Х	X
-LIB	X	X	X
-LIE	X	Х	X
-LIL	RD2 only	RD2 only	RD2 only
-LIM	RD2 only	RD2 only	RD2 only
-EA	Х		X
-EB	X		X
-EE	X		X
-EL	RD2 only		RD2 only
-EM	RD2 only		RD2 only
-EJ			RC2 and RD2 only
-EK			RC2 and RD2 only
-EN			RD2 only

### Table 48. Possible Ordering Entries

• -Ex for samples

- Tape and Reel available for B, E, L and M packages
- Dry pack mandatory for E and M packages